For 100% TTL or ECL/TTL mixed mode circuits;
Single +5V power supply
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT22 2-INPUT NOR, TTL 8mA OUTPUT

LUMPED CAPACITIVE LOAD LIMIT:	FREQUENCY (MHz)	CAP (pF)
	10	100
	20	71
	30	47
	40	39
	45	36

FOR DISTRIBUTED CAPACITIVE LOADS THAT EXCEED THESE LIMITS REFER TO APPENDIX 2-A IN SECTION 2.

$PO = \overline{A + B}$

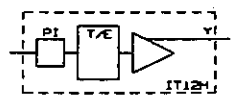
AMCC Q20000 SERIES - TTL LIB MIL5 (210)

For 100% TTL or ECL/TTL mixed mode circuits;
Single +5V power supply
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

IT12 TTL INPUT BUFFER

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	PI->Y	++			457/754	ps
		−−			274/506	ps
k_{fo}, k_{net}	rising Y				1.20/3.72	ps/LU
	falling				2.00/6.20	ps/LU
MIL4 ADJ. FACTOR					1.09/1.00	
ICC I/P	LOW				1.33	mA
	HIGH				1.22	mA
FAN-IN	PI				1	load
FAN-OUT	Y				18	loads
PW					4200	ps min
f_{max}					100	MHz
SIZE					1	I/O cell

Y = PI

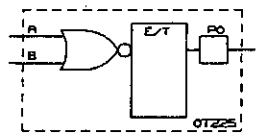


For 100% TTL or ECL/TTL mixed mode circuits;
Single +5V power supply
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT22 2-INPUT NOR, TTL 8mA OUTPUT

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A, B->PO	+−		958/1820		ps
		−+		3137/5210		ps
k_{cap}	rising PO			13/41		ps/pF
	falling			34/106		ps/pF
MIL4 ADJ. FACTOR:				1.09/1.00		
ICC	I/Ps LOW			3.76		mA
	HIGH			3.76		mA
FAN-IN	A, B			1		load
PW				9.0		ns min
f_{max}				45		MHz
SIZE				1		I/O cell

A, B - AT LEAST ONE MUST BE DRIVEN BY A MACRO



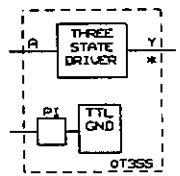
For 100% TTL or ECL/TTL mixed mode circuits;
Single +5V power supply
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT35 3-STATE DRIVER; EXTERNAL TTL GROUND PAD

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->Y	++		554/875		ps
		−−		441/686		ps
k_{fo}, k_{net}	rising Y			1.03/1.65		ps/LU
	falling			3.72/6.20		ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00		
ICC	I/P LOW			4.75		mA
	HIGH			5.17		mA
FAN-IN	A			1		load
FAN-OUT	Y			8		loads
PW				7000		ps min
f_{max}				60		MHz
SIZE				1		I/O cell

3-STATE DRIVER OUTPUT Y TO ENABLE INPUT, ON 3-STATE OR BIDIRECTIONAL MACROS.

Y = A



For 100% TTL or ECL/TTL mixed mode circuits;
Single +5V power supply
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT36 2-INPUT NOR, TTL 8mA 3-STATE OUTPUT

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A, B->PO	+−		866/1696		ps
		−+		3234/5359		ps
	EN->PO	LZ		2647/7037		ps
		HZ		2219/4089		ps
		ZH		2754/4379		ps
		ZL		3373/6100		ps
k_{cap}	rising PO			6/21		ps/pF
	falling			29/90		ps/pF
MIL4 ADJ. FACTOR:				1.09/1.00		
ENABLED:						
ICC	I/Ps LOW			4.46		mA
	HIGH			3.95		mA
DISABLED:						
ICC	I/Ps LOW			4.77		mA
	HIGH			5.12		mA
FAN-IN	A, B, EN			1		load
PW				9.0		ns min
f_{max}				45		MHz
SIZE				1		I/O cell

For 100% TTL or ECL/TTL mixed mode circuits;
Single +5V power supply
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

UT31 2-INPUT NOR, TTL 8mA BIDIRECTIONAL OUTPUT

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A, B->PB	+−		940/1814		ps
		−+		3223/5538		ps
	PB->Y	++		352/627		ps
		−−		315/575		ps
	EN->PB	LZ		2738/6927		ps
		HZ		2310/4215		ps
		ZH		2818/4609		ps
		ZL		3483/6238		ps
k_{to}, k_{net}	rising Y			1.20/3.72		ps/LU
	falling			2.00/6.20		ps/LU
k_{cap}	rising PB			27/86		ps/pF
	falling			45/140		ps/pF
MIL4 ADJ. FACTOR:				1.09/1.00		

For 100% TTL or ECL/TTL mixed mode circuits;
Single +5V power supply
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT36 2-INPUT NOR, TTL 8mA 3-STATE OUTPUT

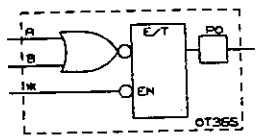
LUMPED CAPACITIVE LOAD LIMIT:	FREQUENCY (MHz)	CAP (pF)
	10	100
	20	71
	30	50
	40	40
	45	35

FOR DISTRIBUTED CAPACITIVE LOADS THAT EXCEED THESE LIMITS REFER TO APPENDIX 2-A IN SECTION 2.

A, B - AT LEAST ONE MUST BE DRIVEN BY A MACRO
EN MUST BE DRIVEN BY A MACRO
USE WHEN CONSTRUCTING BIDIRECTIONAL TTL FUNCTIONS
EN FROM TTL 3-STATE ENABLE DRIVER (OT35)
SIGNAL NAME FOR ENABLE INPUT MUST APPEAR IN THE SIMULATION FORMAT.

EN	A+B	PO
0	0	1
0	1	0
1	X	HiZ

X = DON'T CARE



For 100% TTL or ECL mixed mode circuits;
Single +5V power supply
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

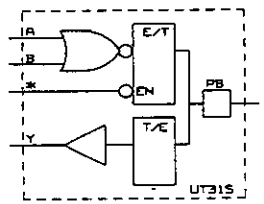
UT31 2-INPUT NOR, TTL 8mA BIDIRECTIONAL OUTPUT

ENABLED:			
ICC	I/PsLOW	5.68	mA
	HIGH	5.88	mA
DISABLED:			
ICC	I/PsLOW	5.98	mA
	HIGH	5.87	mA
FAN-IN	A, B, EN	1	load
FAN-OUT	Y	18	loads
PW	(INPUT MODE)	4.2	ns min
PW	(OUTPUT MODE)	9.0	ns min
f_{max}	(INPUT MODE)	100	MHz
f_{max}	(OUTPUT MODE)	45	MHz
SIZE		2	I/O cells

A, B - AT LEAST ONE MUST BE DRIVEN BY A MACRO
EN MUST BE DRIVEN BY A MACRO
* EN FROM TTL 3-STATE ENABLE DRIVER (OT35)
SIGNAL NAME FOR ENABLE INPUT MUST APPEAR IN THE SIMULATION FORMAT.

EN	A+B	PB	Y	
0	0	1	1	OUTPUT MODE
0	1	0	0	OUTPUT MODE
1	X	0	0	INPUT MODE
1	X	1	1	INPUT MODE

X = DON'T CARE

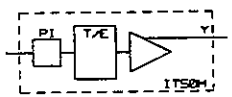


For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

IT50 TTLMIX INPUT BUFFER

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} PI->Y	++			65/336	ps
	--			126/602	ps
k_{fo}, k_{net} rising Y				1.20/3.72	ps/LU
falling				2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00	
ICC I/P LOW				0.697	mA
HIGH				0.588	mA
IEE				1.40	mA
FAN-IN PI				1	load
FAN-OUT Y				18	loads
PW				4.2	ns min
f_{max}				100	MHz
SIZE				1	I/O cell

Y = PI



For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

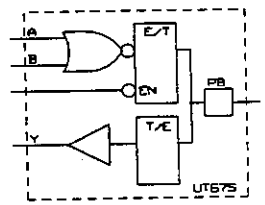
UT67 2-INPUT NOR, TTLMIX 20mA BIDIRECTIONAL OUTPUT

ENABLED:		
ICC I/Ps LOW	3.14	mA
HIGH	1.54	mA
IEE	1.71	mA
DISABLED:		
ICC	2.74	mA
IEE	1.71	mA
FAN-IN A, B, EN	1	load
FAN-OUT Y	9	loads
PW (INPUT MODE)	4200	ps min
PW (OUTPUT MODE)	6700	ps min
f_{max} (INPUT MODE)	100	MHz
f_{max} (OUTPUT MODE)	60	MHz
SIZE	1	I/O cell

EN MUST BE DRIVEN BY A MACRO.
EN CAN BE DRIVEN BY ANY INTERNAL SIGNAL.
(NO PIN RESTRICTION)
SIGNAL NAME FOR ENABLE INPUT MUST APPEAR IN THE SIMULATION FORMAT.

A	B	EN	I	PB	Y	
0	0	0	I	1	1	OUTPUT
1	X	0	I	0	0	OUTPUT
X	1	0	I	0	0	OUTPUT
X	X	1	I	0	0	INPUT
X	X	1	I	1	1	INPUT

X = DON'T CARE

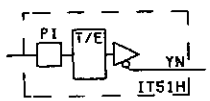


For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

IT51 TTLMIX INVERTING INPUT BUFFER

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} PI->YN	+−			8/11	ps
	−+			808/1578	ps
k_{fo}, k_{net} rising YN				1.20/3.72	ps/LU
falling				2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00	
ICC I/P LOW				0.650	mA
HIGH				0.550	mA
IEE				1.92	mA
FAN-IN PI				1	load
FAN-OUT YN				10	loads
PW				4200	ps min
f_{max}				100	MHz
SIZE				1	I/O cell

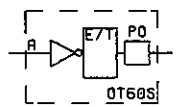
YN = $\overline{PI}$



For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or 5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT60 TTLMIX 8mA OUTPUT INVERTER

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} A->PO	+−		1722/2660		ps
	−+		755/1161		ps
k_{cap} rising PO			38/121		ps/pF
falling			30/94		ps/pF
MIL4 ADJ. FACTOR:			1.09/1.00		
ICC			2.24		mA
IEE			1.35		mA
FAN-IN A			3		loads
PW			5000		ps min
f_{max}			80		MHz
SIZE			1		I/O cell



For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or 5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT60 TTLMIX 8mA OUTPUT INVERTER

LUMPED CAPACITIVE LOAD LIMIT:

FREQUENCY (MHz)	CAP (pF)
10	100
20	100
30	70
40	52
50	42
60	35
70	30
80	27

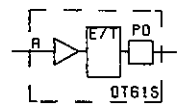
FOR DISTRIBUTED CAPACITIVE LOADS THAT EXCEED THESE LIMITS REFER TO APPENDIX 2-A IN SECTION 2.

PO = $\overline{A}$

For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT61 TTLMIX 8mA OUTPUT BUFFER

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->PO	++		757/1155		ps
		--		1702/2636		ps
k_{cap}	risingPO			38/121		ps/LU
	falling			30/94		ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00		
ICC				2.24		mA
IEE				1.35		mA
FAN-IN	A			3		loads
PW				5000		ps min
f_{max}				80		MHz
SIZE				1		I/O cell



For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT61 TTLMIX 8mA OUTPUT BUFFER

LUMPED CAPACITIVE LOAD LIMIT:

FREQUENCY (MHz)	CAP (pF)
10	100
20	100
30	70
40	52
50	42
60	35
70	30
80	27

FOR DISTRIBUTED CAPACITIVE LOADS THAT EXCEED THESE LIMITS REFER TO APPENDIX 2-A IN SECTION 2.

PO = A

For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT67 2-INPUT NOR, TTLMIX 20mA 3-STATE OUTPUT W/EN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A, B->PO	+-		2800/4920		ps
		-+		2250/4300		ps
	EN->PO	LZ		2957/5124		ps
		HZ		2718/4478		ps
		ZH		3272/5876		ps
		ZL		4059/7043		ps
k_{cap}	rising PO			27/86		ps/pF
	falling			27/86		ps/pF
MIL4 ADJ. FACTOR:				1.09/1.00		
ENABLED:						
ICC I/Ps LOW				2.34		mA
	HIGH			2.34		mA
IEE				1.37		mA
DISABLED:						
ICC				2.63		mA
IEE				1.37		mA
FAN-IN	A, B, EN			1		load
PW				6700		ps min
f_{max}				60		MHz
SIZE				1		I/O cell

For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT67 2-INPUT NOR, TTLMIX 20mA 3-STATE OUTPUT W/EN

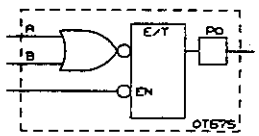
EITHER A OR B MUST BE DRIVEN BY A MACRO.
EN MUST BE DRIVEN BY A MACRO.
EN CAN BE DRIVEN BY ANY INTERNAL SIGNAL.
(NO PIN RESTRICTION)
USE WHEN CONSTRUCTING BIDIRECTIONAL TTLMIX FUNCTIONS.
SIGNAL NAME FOR ENABLE INPUT MUST APPEAR IN THE SIMULATION FORMAT.

LUMPED CAPACITIVE LOAD LIMIT:	FREQUENCY (MHz)	CAP (pF)
	10	100
	20	100
	30	72
	40	52
	50	40
	60	29

FOR DISTRIBUTED CAPACITIVE LOADS THAT EXCEED THESE LIMITS REFER TO APPENDIX 2-A IN SECTION 2.

A	B	EN	I	PO
0	0	0	I	1
1	0	0	I	0
0	1	0	I	0
1	1	0	I	0
X	X	1	I	HiZ

X = DON'T CARE



For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT68 2-INPUT OR, TTLMIX 20mA 3-STATE OUTPUT W/EN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A, B->PO	++		3350/5300		ps
		--		4801/7895		ps
	EN->PO	LZ		3258/6831		ps
		HZ		2883/4504		ps
		ZH		3543/7587		ps
		ZL		3288/6337		ps
k_{cap}	rising PO			27/86		ps/pF
	falling			27/86		ps/pF
MIL4 ADJ. FACTOR:				1.09/1.00		
ENABLED:						
ICC I/Ps LOW				2.63		mA
HIGH				0.893		mA
IEE				0.812		mA
DISABLED:						
ICC				2.34		mA
IEE				0.812		mA
FAN-IN	A, B, EN			1		load
PW				6700		ps min
f_{max}				60		MHz
SIZE				1		I/O cell

For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT68 2-INPUT OR, TTLMIX 20mA 3-STATE OUTPUT W/EN

LUMPED CAPACITIVE LOAD LIMIT:

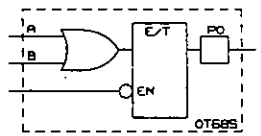
FREQUENCY (MHz)	CAP (pF)
10	100
20	100
30	76
40	55
50	43
60	32

FOR DISTRIBUTED CAPACITIVE LOADS THAT EXCEED THESE LIMITS REFER TO APPENDIX 2-A IN SECTION 2.

EITHER A OR B MUST BE DRIVEN BY A MACRO.
EN MUST BE DRIVEN BY A MACRO.
EN CAN BE DRIVEN BY ANY INTERNAL SIGNAL.
(NO PIN RESTRICTION)
USE WHEN CONSTRUCTING BIDIRECTIONAL TTLMIX FUNCTIONS.
SIGNAL NAME FOR ENABLE INPUT MUST APPEAR IN THE SIMULATION FORMAT.

A	B	EN	I	PO
0	0	0	I	0
1	0	0	I	1
0	1	0	I	1
1	1	0	I	1
X	X	1	I	HiZ

X = DON'T CARE

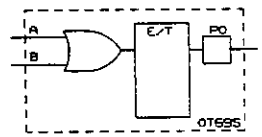


For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT69 2-INPUT OR, TTLMIX 20mA OUTPUT

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A, B->PO	++		2700/5000		ps
		--		2780/4800		ps
k_{cap}	rising PO			27/86		ps/pF
	falling			27/86		ps/pF
MIL4 ADJ. FACTOR:				1.09/1.00		
ICC				2.48		mA
IEE				0.887		mA
FAN-IN	A, B			1		load
PW				6700		ps min
f_{max}				60		MHz
SIZE				1		I/O cell

EITHER A OR B MUST BE DRIVEN BY A MACRO.



For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT69 2-INPUT OR, TTLMIX 20mA OUTPUT

LUMPED CAPACITIVE LOAD LIMIT:

FREQUENCY (MHz)	CAP (pF)
10	100
20	96
30	55
40	30
50	23
60	20

FOR DISTRIBUTED CAPACITIVE LOADS THAT EXCEED THESE LIMITS REFER TO APPENDIX 2-A IN SECTION 2.

PO = A + B

For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT71 TTLMIX 8mA 3-STATE OUTPUT BUFFER WITH EN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->PO	++		922/1408		ps
		−−		1758/2742		ps
	EN->PO	LZ		822/2681		ps
		HZ		1589/2601		ps
		ZH		1269/2054		ps
		ZL		2390/3940		ps
k_{cap}	risingPO			26/82		ps/pF
	falling			36/112		ps/pF
MIL4 ADJ. FACTOR:				1.09/1.00		
ENABLED:						
ICC I/Ps LOW				2.24		mA
	HIGH			1.76		mA
IEE				3.49		mA
DISABLED:						
ICC I/Ps LOW				2.92		mA
	HIGH			2.92		mA
IEE				3.49		mA
FAN-IN	A,EN			1		load
PW				5000		ps min
f_{max}				80		MHz
SIZE				1		I/O cell

EN MUST BE DRIVEN BY A MACRO.

For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OT71 TTLMIX 8mA 3-STATE OUTPUT BUFFER WITH EN

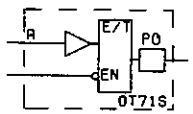
LUMPED CAPACITIVE LOAD LIMIT:

FREQUENCY (MHz)	CAP (pF)
10	100
20	100
30	70
40	52
50	42
60	35
70	30
80	27

FOR DISTRIBUTED CAPACITIVE LOADS THAT EXCEED THESE LIMITS REFER TO APPENDIX 2-A IN SECTION 2.

A	EN	I	PO
1	0	I	1
0	0	I	0
X	1	I	HiZ

X = DON'T CARE

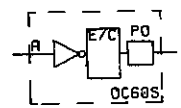


For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or 5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OC60 CMOS OUTPUT

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->PO	+−		1382/2165		ps
		−+		1241/1943		ps
k_{cap}	rising PO			38/121		ps/LU
	falling			30/94		ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00		
ICC				2.24		mA
IEE				1.35		mA
FAN-IN	A			3		loads
FAN-OUT	PO			1		load
PW				5000		ps min
f_{max}				80		MHz
SIZE				1		I/O cell

OC60 SOURCES 1mA WITH VOH min = 0.7 x IOVCC AND SINKS 8mA WITH VOL max = 0.5 VOLT.



For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or 5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OC60 CMOS OUTPUT

LUMPED CAPACITIVE LOAD LIMIT:	FREQUENCY (MHz)	CAP (pF)
	10	100
	20	100
	30	70
	40	52
	50	42
	60	35
	70	30
	80	27

FOR DISTRIBUTED CAPACITIVE LOADS THAT EXCEED THESE LIMITS REFER TO APPENDIX 2-A IN SECTION 2.

TEST REQUIREMENTS:

1 /VOH min = 0.7 × IOVCC @ -1mA./

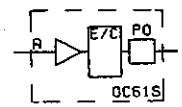
PO = $\overline{A}$

For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OC61 CMOS OUTPUT BUFFER

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->PO	+ +		1243/1950		ps
		– –		1266/2021		ps
k_{cap}	risingPO			38/121		ps/pF
	falling			30/94		ps/pF
MIL4 ADJ. FACTOR:				1.09/1.00		
ICC				2.24		mA
IEE				1.35		mA
FAN-IN	A			3		loads
PW				5000		ps min
f_{max}				80		MHz
SIZE				1		I/O cell

OC61 SOURCES 1mA WITH VOH MIN = 0.7 × IOVCC AND SINKS 8mA WITH VOL MAX = 0.5V.



For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OC61 CMOS OUTPUT BUFFER

LUMPED CAPACITIVE LOAD LIMIT:	FREQUENCY (MHz)	CAP (pF)
	10	100
	20	100
	30	70
	40	52
	50	42
	60	35
	70	30
	80	27

FOR DISTRIBUTED CAPACITIVE LOADS THAT EXCEED THESE LIMITS REFER TO APPENDIX 2-A IN SECTION 2.

TEST REQUIREMENTS:
==========
1 /VOH MIN = 0.7 × IOVCC @ -1mA./

PO = A

For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OC71 CMOS 3-STATE OUTPUT BUFFER WITH EN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->PO	++		1483/2292		ps
		−−		1397/2146		ps
	EN->PO	LZ		822/2681		ps
		HZ		1589/2601		ps
		ZH		1269/2054		ps
		ZL		2390/3940		ps
k_{cap}	risingPO			30/121		ps/pF
	falling			30/94		ps/pF
MIL4 ADJ. FACTOR:				1.09/1.00		
ENABLED:						
ICC I/Ps LOW				2.24		mA
HIGH				1.76		mA
IEE				3.49		mA
DISABLED:						
ICC I/Ps LOW				2.92		mA
HIGH				2.92		mA
IEE				3.49		mA
FAN-IN	A,EN			1		load
PW				5000		ps min
f_{max}				80		MHz
SIZE				1		I/O cell

EN MUST BE DRIVEN BY A MACRO.
OC71 SOURCES 1mA WITH VOH MIN = 0.7 × IOVCC AND SINKS 8mA WITH VOL MAX = 0.5V.

For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OC71 CMOS 3-STATE OUTPUT BUFFER WITH EN

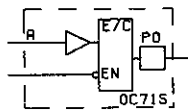
LUMPED CAPACITIVE LOAD LIMIT:	FREQUENCY (MHz)	CAP (pF)
	10	100
	20	100
	30	70
	40	52
	50	42
	60	35
	70	30
	80	27

FOR DISTRIBUTED CAPACITIVE LOADS THAT EXCEED THESE LIMITS REFER TO APPENDIX 2-A IN SECTION 2.

TEST REQUIREMENTS:

1 /VOH MIN = 0.7 x IOVCC @ -1mA./

PO = A



For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

UT67 2-INPUT NOR, TTLMIX 20mA BIDIRECTIONAL OUTPUT

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A, B->PB	+-		2800/4920		ps
		-+		2250/4300		ps
	PB->Y	++		8/430		ps
		--		8/387		ps
	EN->PB	LZ		2228/4780		ps
		HZ		3008/4780		ps
		ZH		3679/6860		ps
		ZL		4108/8322		ps
k_{fo}, k_{net}	rising Y			2.50/7.75		ps/LU
	falling			5.00/15.50		ps/LU
k_{cap}	rising PB			27/86		ps/pF
	falling			27/86		ps/pF

MIL4 ADJ. FACTOR: 1.09/1.00

LUMPED CAPACITIVE LOAD LIMIT:	FREQUENCY (MHz)	CAP (pF)
	10	100
	20	100
	30	74
	40	53
	50	39
	60	25

FOR DISTRIBUTED CAPACITIVE LOADS THAT EXCEED THESE LIMITS REFER TO APPENDIX 2-A IN SECTION 2.

For mixed ECL/TTL mixed mode circuits;
Dual +5V/-5.2V or +5V/-4.5V power supplies
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

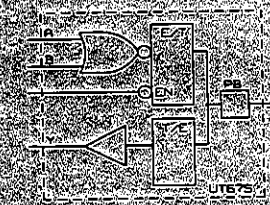
UT67 2-INPUT NOR, TTLMIX 20mA BIDIRECTIONAL OUTPUT

ENABLED:		
ICC I/Ps LOW	3.14	mA
HIGH	1.54	mA
IEE	1.71	mA
DISABLED:		
ICC	2.74	mA
IEE	1.71	mA
FAN-IN A, B, EN	1	load
FAN-OUT Y	9	loads
PW (INPUT MODE)	4200	ps min
PW (OUTPUT MODE)	6700	ps min
f_{max} (INPUT MODE)	100	MHz
f_{max} (OUTPUT MODE)	60	MHz
SIZE	1	I/O cell

EN MUST BE DRIVEN BY A MACRO
EN CAN BE DRIVEN BY ANY INTERNAL SIGNAL
(NO PIN RESTRICTION)
SIGNAL NAME FOR ENABLE INPUT MUST APPEAR IN THE SIMULATION FORMAT

A	B	EN	I	PB	Y	
0	0	0	I	1	1	OUTPUT
1	X	0	I	0	0	OUTPUT
X	1	0	I	0	0	OUTPUT
X	X	1	I	0	0	INPUT
X	X	1	I	1	1	INPUT

X = DON'T CARE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

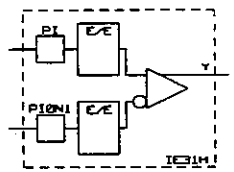
IE31 CML COMPATIBLE DIFFERENTIAL BUFFERED INPUT

	L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} PI,PI0N1->Y (+ –) +			155/294	ps
(– +) –			135/211	ps
k_{fo}, k_{net} rising Y			1.20/3.72	ps/LU
falling			2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	
IEE			2.19	mA
FAN-IN PI, PI0N1			1	load
FAN-OUT Y			18	loads
PW			500	ps min
f_{max}			800	MHz
SIZE			2	I/O cells

VIN(MAX) = (CORE GND)
VIN(MIN) = (CORE V -) + 2.25V
WHERE VALUES FOR (CORE GND) AND (CORE V -) ARE DEFINED IN TABLE 2-3
VDIFF(MIN) = 0.25V
WHERE VDIFF(MIN) IS THE MINIMUM DIFFERENTIAL INPUT REQUIRED TO OBTAIN A FULL LOGIC SWING ON THE OUTPUT

PI	PI0N1	I	Y	
0	0	I	UKN	ILLEGAL
0	1	I	0	
1	0	I	1	
1	1	I	UKN	ILLEGAL

UKN = UNKNOWN



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

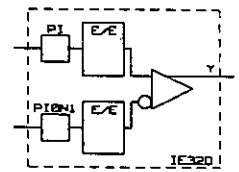
IE32D DIFFERENTIAL INPUT BUFFER, SUPER-DRIVER

	D MIN/MAX	
T_{pd} PI,PI0N1->Y (+ –) +	71/242	ps
(– +) –	62/95	ps
k_{fo}, k_{net} rising Y	0.90/2.79	ps/LU
falling	1.25/3.88	ps/LU
MIL4 ADJ. FACTOR:	1.09/1.00	
IEE	1.69	mA
FAN-IN PI, PI0N1	1	load
FAN-OUT Y	32	loads
PW	560	ps min
f_{max}	800	MHz
SIZE	2	I/O cells

VIN(MAX) = (CORE GND) - 0.5V
VIN(MIN) = (CORE V -) + 2.25V
WHERE VALUES FOR (CORE GND) AND (CORE V -) ARE DEFINED IN TABLE 2-3.
VDIFF(MIN) = 0.25V
WHERE VDIFF(MIN) IS THE MINIMUM DIFFERENTIAL INPUT REQUIRED TO OBTAIN A FULL LOGIC SWING ON THE OUTPUT.

PI	PI0N1	I	Y	
0	0	I	UKN	ILLEGAL
0	1	I	0	
1	0	I	1	
1	1	I	UKN	ILLEGAL

UKN = UNKNOWN



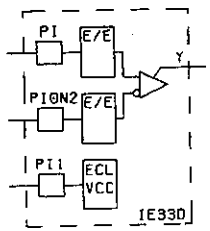
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

IE33D DIFFERENTIAL INPUT BUFFER, SUPER-DRIVER WITH EXTRA ECL VCC (IEVCC)

		D MIN/MAX	
T_{pd}	PI,PI0N2->Y (+ –) +	47/150	ps
	(– +) –	59/90	ps
k_{fo}, k_{net}	rising Y	0.90/2.79	ps/LU
	falling	1.25/3.88	ps/LU
MIL4 ADJ. FACTOR:		1.09/1.00	
IEE		1.94	mA
FAN-IN	PI, PI0N2	1	load
FAN-OUT	Y	32	loads
PW		310	ps min
f_{max}		1.3	GHz
SIZE		3	I/O cells

VIN(MAX) = (CORE GND) - 0.5V
VIN(MIN) = (CORE V -) + 2.25V
WHERE VALUES FOR (CORE GND) AND (CORE V -) ARE DEFINED IN TABLE 2-3.
VDIFF(MIN) = 0.25V
WHERE VDIFF(MIN) IS THE MINIMUM DIFFERENTIAL INPUT REQUIRED TO OBTAIN A FULL LOGIC SWING ON THE OUTPUT.

PI	PI0N2	Y	
0	0	UKN	ILLEGAL
0	1	0	
1	0	1	
1	1	UKN	ILLEGAL



UKN = UNKNOWN

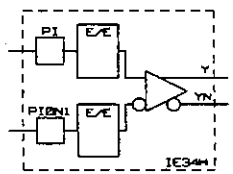
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

IE34 DIFFERENTIAL INPUT BUFFER; Y, YN

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	PI,PI0N1->Y (+ –) +			133/285	ps
	(– +) –			95/149	ps
	PI,PI0N1->YN (– +) +			129/278	ps
	(+ –) –			95/149	ps
k_{fo}, k_{net}	rising Y, YN			1.20/3.72	ps/LU
	falling			2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00	
IEE				1.69	mA
FAN-IN	PI, PI0N1			1	load
FAN-OUT	Y, YN			18	loads
PW				500	ps min
f_{max}				800	MHz
SIZE				2	I/O cells

VIN(MAX) = (CORE GND) - 0.5V
VIN(MIN) = (CORE V -) + 2.25V
WHERE VALUES FOR (CORE GND) AND (CORE V -) ARE DEFINED IN TABLE 2-3
VDIFF(MIN) = 0.25V
WHERE VDIFF(MIN) IS THE MINIMUM DIFFERENTIAL INPUT REQUIRED TO OBTAIN A FULL LOGIC SWING ON THE OUTPUT

PI	PI0N1	Y	YN	
0	0	UKN	UKN	ILLEGAL
0	1	0	1	
1	0	1	0	
1	1	UKN	UKN	ILLEGAL



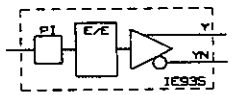
UKN = UNKNOWN

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

IE93 INPUT BUFFER, COMPLIMENTARY OUTPUTS; Y, YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	PI->Y	++		174/438		ps
		−−		71/121		ps
	PI->YN	+−		86/132		ps
		−+		151/410		ps
k_{fo}, k_{net}	rising Y, YN			1.50/4.65		ps/LU
	falling			2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00		
IEE				1.12		mA
FAN-IN PI				1		load
FAN-OUT Y, YN				18		loads
PW				650		ps min
f_{max}				600		MHz
SIZE				1		I/O cell

Y = PI YN = $\overline{PI}$

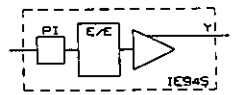


Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

IE94 INPUT BUFFER

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	PI->Y	++		113/281		ps
		−−		57/92		ps
k_{fo}, k_{net}	rising Y			1.50/4.65		ps/LU
	falling			2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00		
IEE				1.01		mA
FAN-IN PI				1		load
FAN-OUT Y				18		loads
PW				650		ps min
f_{max}				600		MHz
SIZE				1		I/O cell

Y = PI

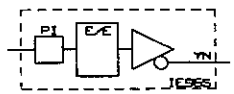


Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

IE96 INPUT BUFFER, INVERTING

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	PI->YN	+−		69/107		ps
		−+		76/208		ps
k_{fo}, k_{net}	rising YN			1.50/4.65		ps/LU
	falling			2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00		
IEE				1.01		mA
FAN-IN	PI			1		load
FAN-OUT	YN			18		loads
PW				650		ps min
f_{max}				600		MHz
SIZE				1		I/O cell

$YN = \overline{PI}$



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

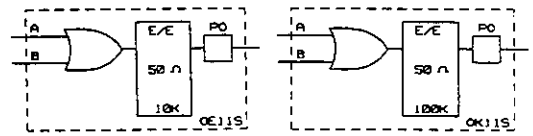
Ox11 2-INPUT OR, 50 OHM TERMINATION

			OE11 S MIN/MAX	OK11 S MIN/MAX	
T_{pd}	A, B->PO	++	182/439	206/346	ps
		−−	252/459	278/550	ps
k_{cap}	rising PO		14/44	14/44	ps/pF
	falling		17/53	17/53	ps/pF
MIL4 ADJ. FACTOR:			1.09./1.00	1.09./1.00	
IEE			5.88	5.63	mA
FAN-IN	A,B		2	2	loads
PW			1150	1150	ps min
f_{max}			350	350	MHz
SIZE			1	1	I/O cell

A, B - AT LEAST ONE MUST BE DRIVEN BY A MACRO

PO = A + B

OE11: ECL10K
OK11: ECL100K



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OE14 3-INPUT NOR, 50 OHM TERMINATION; DIFF.

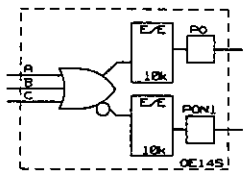
			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A, B, C->PO	++		174/396		ps
		−−		223/454		ps
	A, B, C->PON1	+−		174/396		ps
		−+		223/454		ps
k_{cap}	rising PO,PON1			14/44		ps/pF
	falling			17/53		ps/pF
MIL4 ADJ. FACTOR:				1.09/1.00		
IEE				5.88		mA
FAN-IN	A,B,C			2		loads
PW				800		ps min
f_{max}				500		MHz
SIZE				2		I/O cells

A, B, C MUST BE DRIVEN BY A MACRO

PO = A + B + C

PON1 = $\overline{A + B + C}$

OE14: ECL10K



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

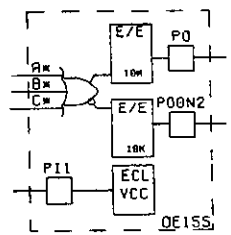
OE15 3-INPUT OR/NOR, 50 OHM TERMINATION; DIFF., WITH EXTRA ECL VCC (IEVCC)

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A, B, C->PO,PO0N2				
	+ (+ −)		176/399		ps
	− (− +)		228/466		ps
k_{cap}	rising PO,PO0N2		14/44		ps/pF
	falling		17/53		ps/pF
MIL4 ADJ. FACTOR:			1.09/1.00		
IEE			5.88		mA
FAN-IN	A,B,C		2		loads
PW			800		ps min
f_{max}			500		GHz
SIZE			3		I/O cells

A, B, C - AT LEAST ONE MUST BE DRIVEN BY A MACRO.
PI1 IS EXTRA ECL VCC (IEVCC).
IEVCC is a GROUND pad in a STD-REF ECL circuit.
IEVCC is a POWER pad in a +5V REF ECL circuit.

A	B	C	I	PO	PO0N2
0	0	0	I	0	1
1	X	X	I	1	0
X	1	X	I	1	0
X	X	1	I	1	0

UKN = UNKNOWN



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

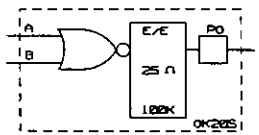
OK20 2-INPUT NOR, 25 OHM TERMINATION; DARLINGTON

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A, B->PO	+−		166/394		ps
		−+		244/380		ps
k_{cap}	rising PO			11/36		ps/pF
	falling			15/34		ps/pF
MIL4 ADJ. FACTOR:				1.09/1.00		
ICC				3.78		mA
IEE				5.11		mA
FAN-IN	A, B			2		loads
PW				650		ps min
f_{max}				600		MHz
SIZE				1		I/O cell

A, B - AT LEAST ONE MUST BE DRIVEN BY A MACRO
DARLINGTONS CAN ONLY BE USED IN A DUAL-SUPPLY CIRCUIT.

$PO = \overline{A + B}$

OK20: ECL100K



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

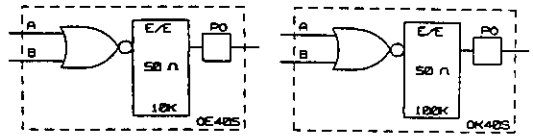
Ox40 2-INPUT NOR, 50 OHM TERMINATION; DARLINGTON

			OE40 S MIN/MAX	OK40 S MIN/MAX	
T_{pd}	A, B->PO	+−	138/291	157/356	ps
		−+	198/397	224/347	ps
k_{cap}	rising PO		11/36	11/36	ps/pF
	falling		17/55	17/55	ps/pF
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	
ICC			3.57	3.65	mA
IEE			5.11	5.10	mA
FAN-IN	A, B		2	2	loads
PW			650	650	ps min
f_{max}			600	600	MHz
SIZE			1	1	I/O cell

A, B - AT LEAST ONE MUST BE DRIVEN BY A MACRO
DARLINGTONS CAN ONLY BE USED IN A DUAL-SUPPLY CIRCUIT.

$PO = \overline{A + B}$

OE40: ECL10K
OK40: ECL100K



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

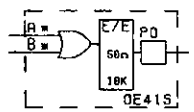
OE41 2-INPUT OR, 50 OHM TERMINATION; DARLINGTON

			S MIN/MAX	
T_{pd}	A, B->PO	++	167/389	ps
		−−	184/317	ps
k_{cap}	rising PO		11/36	ps/pF
	falling		17/55	ps/pF
MIL4 ADJ. FACTOR:			1.09/1.00	
ICC			3.46	mA
IEE			4.74	mA
FAN-IN	A,B		2	loads
PW			650	ps min
f_{max}			600	MHz
SIZE			1	I/O cell

A, B - AT LEAST ONE MUST BE DRIVEN BY A MACRO.
DARLINGTONS CAN ONLY BE USED IN A DUAL-SUPPLY CIRCUIT.

PO = A + B

OE41: ECL10K



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

Ox42 2-INPUT NOR, 50 OHM TERMINATION; CUT-OFF

			OE42 S MIN/MAX	OK42 S MIN/MAX	
T_{pd}	A, B->PO	+−	195/398	206/480	ps
		−+	244/513	267/410	ps
	EN->PO	+−	164/334	171/372	ps
		−+	289/711	312/611	ps
k_{cap}	rising PO		14/44	14/44	ps/pF
	falling		17/53	17/53	ps/pF
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	
IEE			7.76	7.76	mA
FAN-IN	A,B		2	2	loads
	EN		4	4	loads
PW			1150	1150	ps min
f_{max}			350	350	MHz
SIZE			1	1	I/O cell

EN MUST BE DRIVEN BY A MACRO.
USE WHEN CONSTRUCTING BIDIRECTIONAL ECL FUNCTION.
THE CUTOFF VOLTAGE SPEC. IS VCC - 1.9V OR LESS.

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

Ox42 2-INPUT NOR, 50 OHM TERMINATION; CUT-OFF

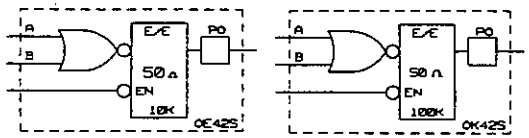
TEST REQUIREMENTS

1 /THE VOC MAX TEST LIMIT FOR THIS MACRO IS VCC -1.9V./

A	B	EN	I	PO
0	0	0	I	1
0	1	0	I	0
1	0	0	I	0
1	1	0	I	0
X	X	1	I	0 (HiZ)

X = DON'T CARE

OE42: ECL10K
OK42: ECL100K



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

OE60 CML; DIFF. OPEN COLLECTOR OUTPUTS, 50 OHMS TO GND EXTERNAL TERMINATION

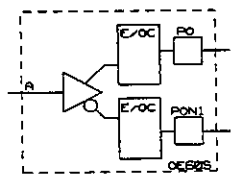
		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->PO,PON1 + (+ –)		64/127		ps
	– (– +)		47/109		ps
k_{cap}	rising PO,PON1		17/55		ps/pF
	falling		17/55		ps/pF
MIL4 ADJ. FACTOR:			1.09/1.00		
IEE			15.53		mA
FAN-IN	A		5		loads
PW			350		ps min
f_{max}			1.2		GHz
SIZE			2		I/O cells

A MUST BE DRIVEN BY A MACRO.
50 OHM TERMINATION
NO STATIC ECL OUTPUT POWER COMPUTATION FOR THIS MACRO.
I (OUT) = 10mA (TYP) THROUGH A 50 OHM RESISTOR FOR A 500mV TYPICAL SWING.

PO = A

PON1 = $\overline{A}$

OE60: ECL10K



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

Ux54 3-INPUT NOR, 50 OHM TERMINATION; BIDIRECTIONAL; SECOND PAD TIED TO ECL VCC

			UE54 S MIN/MAX	UK54 S MIN/MAX	
T_{pd}	A, B, C->PB	+−	194/444	207/363	ps
		−+	239/487	258/529	ps
	PB->YN	+−	170/384	179/312	ps
		−+	285/595	306/638	ps
	EN->PB	+−	135/219	135/219	ps
		−+	20/203	20/203	ps
k_{fo}, k_{net}	rising YN		1.50/4.65	1.50/4.65	ps/LU
	falling		2.50/7.75	2.50/7.75	ps/LU
k_{cap}	rising PB		14/44	14/44	ps/pF
	falling		17/53	17/53	ps/pF
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	
IEE			8.30	8.30	mA
FAN-IN	A,B C		2	2	loads
	EN		4	4	loads
FAN-OUT	YN		18	18	loads
PW	(INPUT MODE)		650	650	ps min
PW	(OUTPUT MODE)		1150	1150	ps min
f_{max}	(INPUT MODE)		600	600	MHz
f_{max}	(OUTPUT MODE)		350	350	MHz
SIZE			2	2	I/O cells

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

Ux54 3-INPUT NOR, 50 OHM TERMINATION; BIDIRECTIONAL; SECOND PAD TIED TO ECL VCC

DRIVE EN BY ANY INTERNAL LEVEL SIGNAL
NO PIN RESTRICTION ON EN
EN MUST BE DRIVEN BY A MACRO
PI1 IS AN EXTRA ECL VCC (IEVCC)
THE CUTOFF VOLTAGE SPEC. IS VCC - 1.9V OR LESS

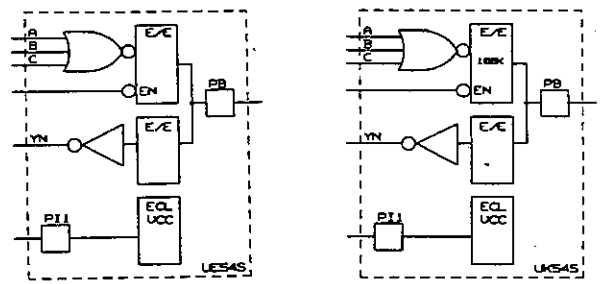
TEST REQUIREMENTS

1 /THE V_{oc} MAX TEST LIMIT FOR THIS MACRO IS VCC -1.9V./

A	B	C	EN	I	PB	YN	
0	0	0	0	I	1	0	OUTPUT
1	X	X	0	I	0	1	OUTPUT
X	1	X	0	I	0	1	OUTPUT
X	X	1	0	I	0	1	OUTPUT
X	X	X	1	I	1	0	INPUT
X	X	X	1	I	0	1	INPUT

X = DON'T CARE

UE54: ECL10K
UK54: ECL100K



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

AD05 ONE BIT FULL ADDER

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->S	++	179/304	148/265		ps
		−−	120/222	101/179		ps
		+−	153/293	118/231		ps
		−+	140/223	126/198		ps
	B->S	++	234/440	192/373		ps
		−−	140/238	120/188		ps
		+−	210/438	160/341		ps
		−+	157/245	124/201		ps
	CI->S	++	120/197	111/188		ps
		−−	79/143	61/114		ps
		+−	93/159	76/130		ps
		−+	87/142	79/127		ps
	A->CO	++	216/348	150/289		ps
		−−	130/237	102/183		ps
	B->CO	++	269/468	195/377		ps
		−−	149/243	118/187		ps
	CI->CO	++	147/255	115/187		ps
		−−	95/156	67/118		ps
k_{fo}, k_{net}	rising S, CO		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range .

AD05 ONE BIT FULL ADDER

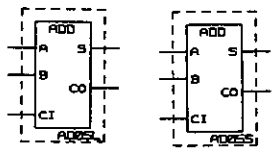
		L	S	H	
IEE		1.11	1.46		mA
FAN-IN	A, B	1	1		load
	CI	2	2		loads
FAN-OUT	S, CO	18	18		loads
PW		650	500		ps min
f_{max}		600	800		MHz
SIZE		2	3		L cells

A, B - EACH MUST BE DRIVEN BY A MACRO.

$S = A \oplus B \oplus CI$

$CO = A * B + (A \oplus B) * CI$

A	B	CI	I	S	CO
0	0	0	I	0	0
0	0	1	I	1	0
0	1	0	I	1	0
0	1	1	I	0	1
1	0	0	I	1	0
1	0	1	I	0	1
1	1	0	I	0	1
1	1	1	I	1	1



* = AND

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

ADD00 4-BIT CARRY LOOK-AHEAD ADDER W/CARRY OUTPUT

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	Ai, Bi->Si	++	506/986	326/653	267/576	ps
		−−	372/863	258/644	201/494	ps
		+−	379/987	236/667	199/572	ps
		−+	356/906	248/638	210/697	ps
	Ai, Bi->CO	++	534/1035	354/654	184/570	ps
		−−	343/752	328/603	145/536	ps
	CI->CO	++	339/565	214/380	178/323	ps
		−−	253/415	214/324	197/312	ps
	CI->Si	++	130/577	74/386	69/331	ps
		−−	131/530	95/363	81/487	ps
		+−	79/527	60/396	52/326	ps
		−+	178/606	111/394	96/531	ps
	i = 0, 1, 2, 3					
k_{fo}, k_{net}	rising Si, CO		1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
	falling		3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
	i = 0, 1, 2, 3					
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	1.09/1.00	

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

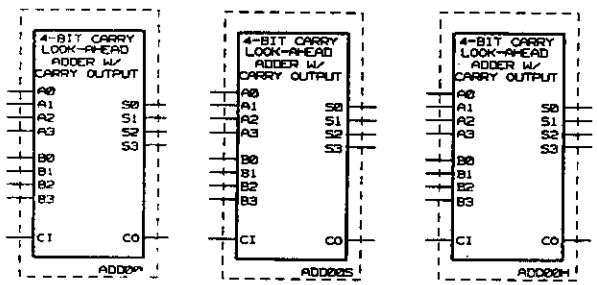
ADD00 4-BIT CARRY LOOK-AHEAD ADDER W/CARRY OUTPUT

		L	S	H	
IEE		6.95	10.70	15.73	mA
FAN-IN	Ai	2	2	2	loads
	Bi	1	1	1	load
	CI	5	5	5	loads
	i = 0, 1, 2, 3				
FAN-OUT	Si, CO	18	18	18	loads
ROUTABLE PINS		54	54	54	
PW		650	500	350	ps min
f_{max}		600	800	1200	MHz
SIZE		24	24	28	L cells

Bi MUST BE DRIVEN BY A MACRO.

i = 0, 1, 2, 3

The ADD00 macro is a four-bit semi-fast carry look-ahead adder with carry output. These macros can be cascaded by attaching the CO output of one stage to the CI input of the next stage. The main advantage of this adder over the ADD02 macro is hardware savings, if speed is not the critical parameter.



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

ADD00 4-BIT CARRY LOOK-AHEAD ADDER W/CARRY OUTPUT

$$S0 = \overline{P0} \oplus \overline{CI}$$

$$S1 = \overline{P1} \oplus \overline{C1}$$

$$S2 = \overline{P2} \oplus \overline{C2}$$

$$S3 = \overline{P3} \oplus \overline{C3}$$

$$C1 = G0 + \overline{(\overline{P0} + \overline{CI})}$$

$$C2 = G1 + \overline{(\overline{P1} + \overline{G0})} + \overline{(\overline{P1} + \overline{P0} + \overline{CI})}$$

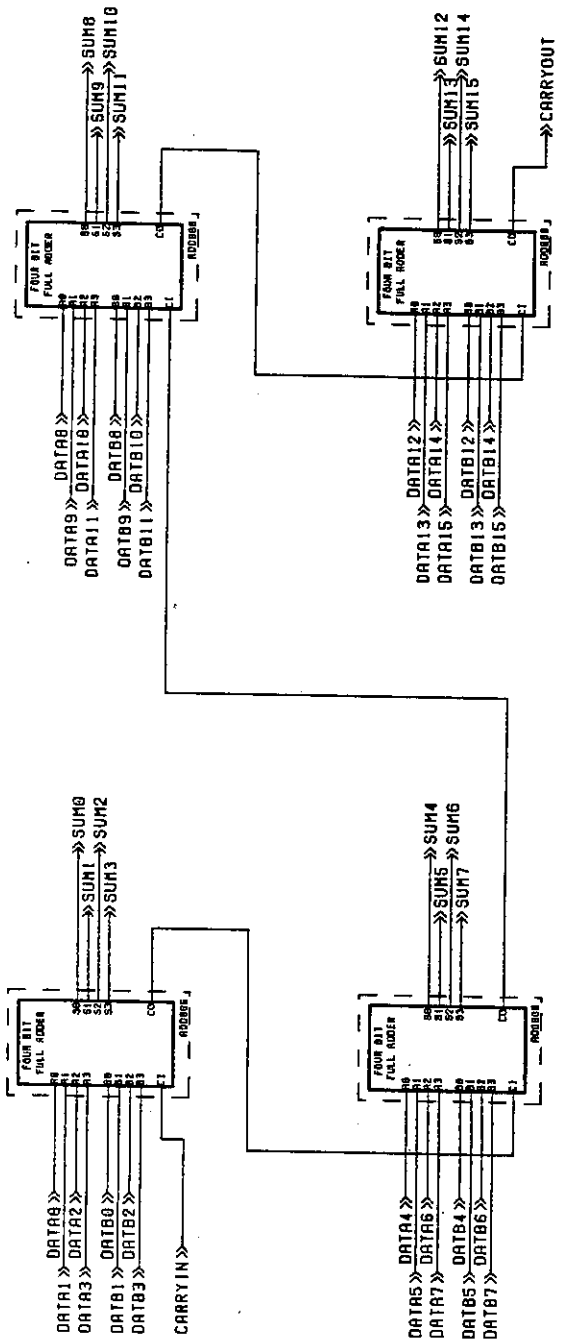
$$C3 = G2 + \overline{(\overline{P2} + \overline{G1})} + \overline{(\overline{P2} + \overline{P1} + \overline{G0})} + \overline{(\overline{P2} + \overline{P1} + \overline{P0} + \overline{CI})}$$

$$CO = G3 + \overline{(\overline{P3} + \overline{G2})} + \overline{(\overline{P3} + \overline{P2} + \overline{G1})} + \overline{(\overline{P3} + \overline{P2} + \overline{P1} + \overline{G0})} + \overline{(\overline{P3} + \overline{P2} + \overline{P1} + \overline{P0} + \overline{CI})}$$

where:

P0 = A0 ⊕ B0
P1 = A1 ⊕ B1
P2 = A2 ⊕ B2
P3 = A3 ⊕ B3
G0 = A0 * B0
G1 = A1 * B1
G2 = A2 * B2
G3 = A3 * B3

* = AND



16-BIT RIPPLE ADDER USING ADD00

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

ADD02 4-BIT CARRY LOOK-AHEAD ADDER W/PN & G OUTPUTS

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	Ai, Bi->Si	++	516/963	333/640	278/570	ps
		−−	387/824	268/616	216/489	ps
		+−	379/1012	232/686	203/586	ps
		−+	362/953	250/673	226/714	ps
	Ai, Bi->PN	++	468/818	306/538	261/488	ps
		−−	360/699	248/524	203/418	ps
		+−	388/765	271/575	222/451	ps
		−+	423/736	275/485	236/440	ps
	Ai, Bi->G	++	517/1027	346/657	184/569	ps
		−−	330/805	298/610	143/595	ps
	CI->Si	++	132/574	75/383	71/331	ps
		−−	122/552	87/388	76/492	ps
		+−	79/521	61/392	55/326	ps
		−+	167/628	103/420	90/534	ps
	i = 0, 1, 2, 3					
k_{fo}, k_{net}	rising Si, PN, G		1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
	falling		3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
	i = 0, 1, 2, 3					
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	1.09/1.00	

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

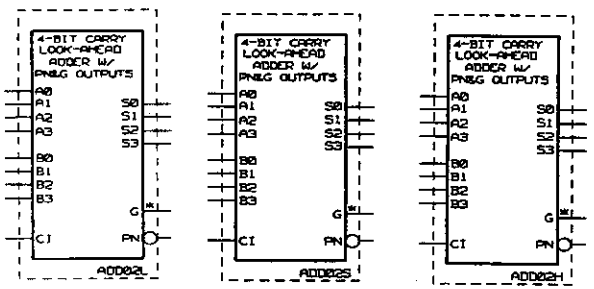
ADD02 4-BIT CARRY LOOK-AHEAD ADDER W/PN & G OUTPUTS

		L	S	H	
IEE		6.95	10.70	15.81	mA
FAN-IN	Ai	2	2	2	loads
	Bi	1	1	1	load
	CI	4	4	4	loads
	i = 0, 1, 2, 3				
FAN-OUT	Si, G,PN	18	18	18	loads
ROUTABLE PINS		67	67	67	
PW		650	500	350	ps min
f_{max}		600	800	1200	MHz
SIZE		24	24	28	L cells

Bi MUST BE DRIVEN BY A MACRO.

i = 0, 1, 2, 3

The ADD02 macro is a four-bit fast carry look-ahead adder with negated propagate (PN) and generate (G) outputs. The PN and G outputs feed carry look-ahead generator CPG02, which can build a 16-bit fast adder. Consult AMCC on methodology for implementing larger fast adders.



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

ADD02 4-BIT CARRY LOOK-AHEAD ADDER W/PN & G OUTPUTS

$$S0 = \overline{P0} \oplus \overline{CI}$$

$$S1 = \overline{P1} \oplus \overline{C1}$$

$$S2 = \overline{P2} \oplus \overline{C2}$$

$$S3 = \overline{P3} \oplus \overline{C3}$$

$$C1 = G0 + \overline{(P0 + CI)}$$

$$C2 = G1 + \overline{(P1 + G0)} + \overline{(P1 + P0 + CI)}$$

$$C3 = G2 + \overline{(P2 + G1)} + \overline{(P2 + P1 + G0)} + \overline{(P2 + P1 + P0 + CI)}$$

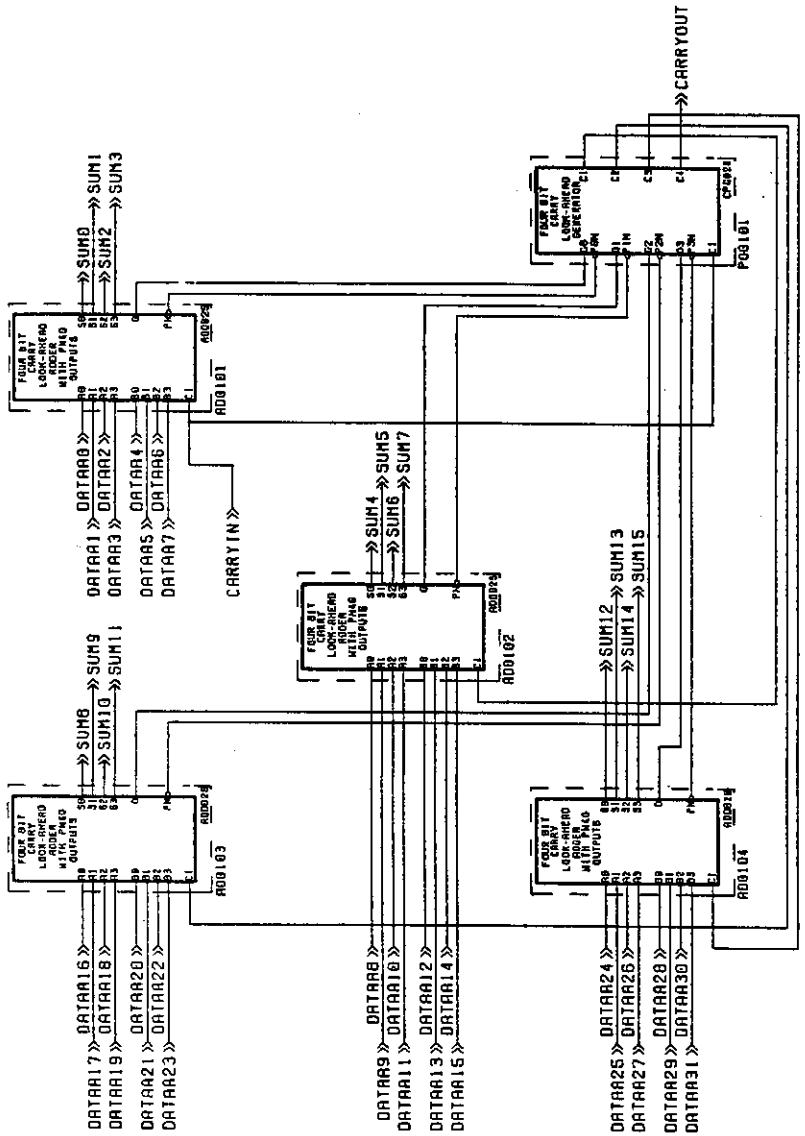
$$G = G3 + \overline{(P3 + G2)} + \overline{(P3 + P2 + G1)} + \overline{(P3 + P2 + P1 + G0)}$$

$$PN = \overline{P0} + \overline{P1} + \overline{P2} + \overline{P3}$$

where:

$P0 = A0 \oplus B0$
$P1 = A1 \oplus B1$
$P2 = A2 \oplus B2$
$P3 = A3 \oplus B3$
$G0 = A0 * B0$
$G1 = A1 * B1$
$G2 = A2 * B2$
$G3 = A3 * B3$

* = AND



16-BIT CARRY-LOOK AHEAD ADDER USING ADD02

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

CMP00 8-BIT COMPARATOR

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	Ai->AEB	++		425/818		ps
		−−		399/736		ps
		+−		420/761		ps
		−+		413/800		ps
	Ai->AGB	++		441/783		ps
		−−		372/751		ps
	Ai->ALB	+−		290/577		ps
		−+		433/725		ps
	Bi->AEB	++		457/899		ps
		−−		414/780		ps
		+−		448/848		ps
		−+		429/845		ps
	Bi->AGB	+−		416/849		ps
		−+		435/803		ps
	Bi->ALB	++		412/677		ps
		−−		248/466		ps
	EN->AEB	+−		103/200		ps
		−+		107/170		ps
	EN->AGB	+−		68/117		ps
		−+		81/128		ps
	EN->ALB	+−		103/201		ps
		−+		107/171		ps
	i = 0,1,2,3,4,5,6,7					
k_{fo}, k_{net}	rising AEB,AGB,ALB			1.50/4.65		ps/LU
	falling			2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00		

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

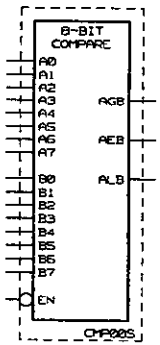
CMP00 8-BIT COMPARATOR

		L	S	H	
IEE			20.00		mA
FAN-IN	Ai,Bi		2		loads
	EN		3		loads
	i = 0,1,2,3,4,5,6,7				
FAN-OUT	AEB,AGB,ALB		18		loads
PW			400		ps min
f_{max}			1000		MHz
SIZE			40		L cells

Bi - EACH MUST BE DRIVEN BY A MACRO
EN MUST BE DRIVEN BY A MACRO

EN	COMPARE	AGB	AEB	ALB
1	X	0	0	0
0	A>B	1	0	0
0	A=B	0	1	0
0	A<B	0	0	1

X = DON'T CARE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

CPG02 4-BIT CARRY LOOK-AHEAD GENERATOR

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	PiN->Cj	+−	523/1101	372/760	389/751	ps
		−+	476/1058	314/736	257/612	ps
	Gi->Cj	++	260/568	202/375	62/325	ps
		−−	199/451	193/376	60/408	ps
	CI->Cj	++	312/568	197/379	164/328	ps
		−−	215/452	167/347	196/416	ps
	i = 0, 1, 2, 3					
	j = 1, 2, 3, 4					
k_{fo}, k_{net}	rising Cj		1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
	falling		3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
	j = 1, 2, 3, 4					
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	1.09/1.00	
IEE			6.46	9.22	12.00	mA
FAN-IN	G0, CI		4	4	4	loads
	G1		3	3	3	loads
	G2		2	2	2	loads
	G3,PiN		1	1	1	load
	i = 0,1,2,3					
FAN-OUT	Cj		18	18	18	loads
	j = 1, 2, 3, 4					
ROUTABLE PINS			48	48	48	
PW			650	500	350	ps min
f_{max}			600	800	1200	MHz
SIZE			20	20	24	L cells

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

CPG02 4-BIT CARRY LOOK-AHEAD GENERATOR

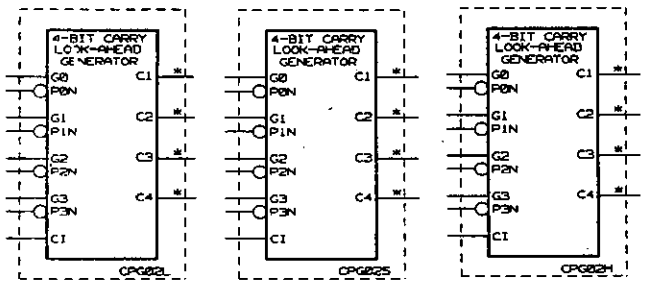
CPG02 is a carry look-ahead generator for use with ADD02. The inputs are negated propagate (PN) and generate (G) from up to four ADD02s, to permit a 16-bit fast addition to be performed. Consult AMCC on methodology for implementing larger fast adders.

$$C1 = G0 + \overline{(P0N + \overline{CI})}$$

$$C2 = G1 + \overline{(P1N + \overline{G0})} + \overline{(P1N + P0N + \overline{CI})}$$

$$C3 = G2 + \overline{(P2N + \overline{G1})} + \overline{(P2N + P1N + \overline{G0})} + \overline{(P2N + P1N + P0N + \overline{CI})}$$

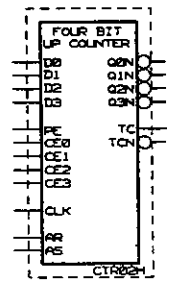
$$C4 = G3 + \overline{(P3N + \overline{G2})} + \overline{(P3N + P2N + \overline{G1})} + \overline{(P3N + P2N + P1N + \overline{G0})} + \overline{(P3N + P2N + P1N + P0N + \overline{CI})}$$



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

CTR02 4-BIT UP-COUNTER, RISING-EDGE LATCHED, WITH ASYNCHRONOUS SET, RESET

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	CLK->ALL QiN	++			211/452	ps
		+−			189/514	ps
	CLK->TC	++			271/448	ps
		+−			165/362	ps
	CLK->TCN	++			260/416	ps
		+−			173/387	ps
	AR->ALL QiN	++			196/382	ps
	AS->ALL QiN	+−			183/503	ps
	i = 0, 1, 2, 3					
k_{fo}, k_{net}	rising QiN, TC, TCN				1.20/3.72	ps/LU
	falling				2.00/6.20	ps/LU
	i = 0, 1, 2, 3					
MIL4 ADJ. FACTOR:					1.09/1.00	



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

CTR02 4-BIT UP-COUNTER, RISING-EDGE LATCHED, WITH ASYNCHRONOUS SET, RESET

	L	S	H	
IEE			15.4	mA
FAN-IN Di, CEi, PE, CLK, AR, AS i = 0, 1, 2, 3			1	load
FAN-OUT QiN			14	loads
TC, TCN i = 0, 1, 2, 3			18	loads
ROUTABLE PINS			134	
T_{su}(PE)			525	ps min
T_{su} (CEi)			795	ps min
T_{su} (Di)			355	ps min
T_h (PE, CEi, Di)			0	ps min
T_{rec} (AR)			300	ps min
T_{rec} (AS) i = 0, 1, 2, 3			300	ps min
PW(CLK,AR,AS)			430	ps min
f_{max}			950	MHz
SIZE			26	L cells

PE, CLK, AR, AS - EACH MUST BE DRIVEN BY A MACRO.

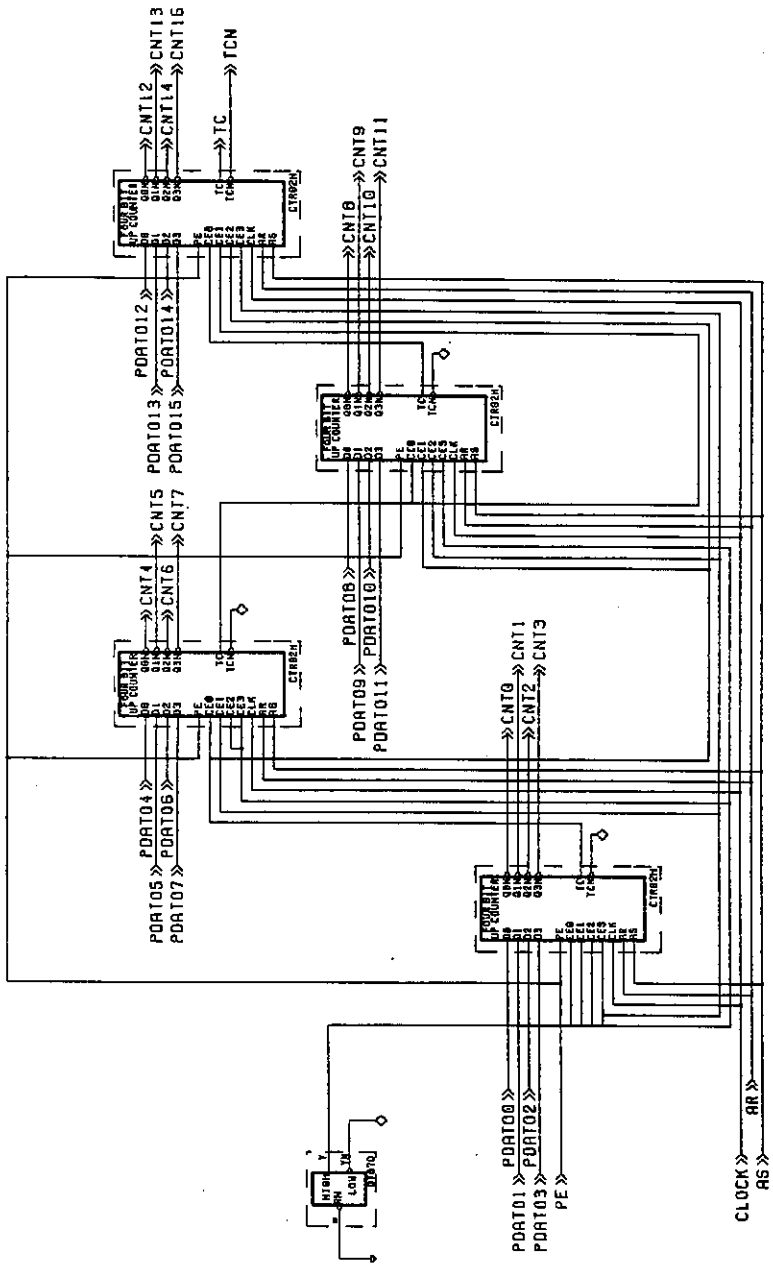
CTR02 is a positive edge triggered, resettable four-bit up-counter with active low outputs. TC and TCN are synchronous with the CLK and are in phase with the QiN outputs. AS and AR asynchronously set and reset the QiN outputs, but do not work asynchronously on the TC and TCN outputs. This macro may be cascaded with itself to form up to a 16-bit counter by connecting TC outputs to CEi inputs. Any unused CEi input, i ≤ 3, must be tied high.

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

CTR02 4-BIT UP-COUNTER, RISING-EDGE LATCHED, WITH ASYNCHRONOUS SET, RESET

AR	AS	PE	CE0	CE1	CE2	CE3	CLK	MODE
0	0	1	X	X	X	X	R	LOAD
0	0	0	0	X	X	X	R	HOLD
0	0	0	X	0	X	X	R	HOLD
0	0	0	X	X	0	X	R	HOLD
0	0	0	X	X	X	0	R	HOLD
0	0	0	1	1	1	1	R	COUNT
1	0	X	X	X	X	X	X	RESET
0	1	X	X	X	X	X	X	SET
1	1	X	X	X	X	X	X	UKN

R = RISING EDGE
UKN = UNKNOWN
X = DON'T CARE



16-BIT COUNTER USING CTR02

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

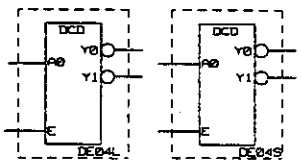
DE04 1:2 DECODER, HI-ENABLE, LOW ACTIVE OUTPUTS

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A0->Y0	++	165/263	105/167		ps
		−−	97/165	71/132		ps
	A0->Y1	+−	110/181	83/144		ps
		−+	143/219	89/135		ps
	E->Y0	+−	151/281	114/222		ps
		−+	232/360	184/281		ps
	E->Y1	+−	147/277	114/222		ps
		−+	238/371	186/284		ps
k_{fo}, k_{net}	rising Y0, Y1		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.629	0.936		mA
FAN-IN	A0		2	2		loads
	E		1	1		load
FAN-OUT	Y0, Y1		18	18		loads
PW			650	500		ps min
f_{max}			600	800		MHz
SIZE			2	2		L cells

E MUST BE DRIVEN BY A MACRO

E	A0	Y0	Y1
0	X	1	1
1	0	0	1
1	1	1	0

X = DON'T CARE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

DE25 2:4 DECODER, HI-ENABLE, LOW ACTIVE OUTPUTS

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->Y0	++	166/273	95/162		ps
		−−	115/187	73/140		ps
	A->Y1	+−	112/187	82/147		ps
		−+	122/187	76/121		ps
	A->Y2	++	178/301	98/169		ps
		−−	122/197	76/146		ps
	A->Y3	+−	108/182	78/143		ps
		−+	126/192	73/118		ps
	B->Y0	++	243/385	149/246		ps
		−−	207/342	142/252		ps
	B->Y1	++	214/360	140/240		ps
		−−	186/319	137/245		ps
	B->Y2	+−	193/351	130/265		ps
		−+	257/394	150/241		ps
	B->Y3	+−	165/312	121/250		ps
		−+	223/346	142/221		ps
	E->Y0	+−	327/591	213/434		ps
		−+	290/447	175/284		ps
	E->Y1	+−	319/584	215/438		ps
		−+	272/420	175/277		ps
	E->Y2	+−	303/566	203/427		ps
		−+	306/477	180/293		ps
	E->Y3	+−	280/531	195/412		ps
		−+	281/424	175/277		ps
k_{fo}, k_{net}	rising Yi		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
	i = 0, 1, 2, 3					
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		

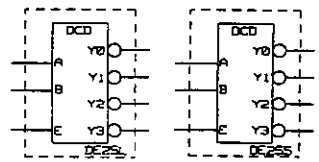
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

DE25 2:4 DECODER, HI-ENABLE, LOW ACTIVE OUTPUTS

		L	S	H	
IEE		1.43	1.88		mA
FAN-IN	A	4	4		loads
	B, E	1	1		load
FAN-OUT	Yi	18	18		loads
	i = 0, 1, 2, 3				
PW		650	500		ps min
f_{max}		600	800		MHz
SIZE		4	4		L cells

B, E - EACH MUST BE DRIVEN BY A MACRO.

E	B	A	I	Y0	Y1	Y2	Y3
1	0	0	I	0	1	1	1
1	0	1	I	1	0	1	1
1	1	0	I	1	1	0	1
1	1	1	I	1	1	1	0
0	X	X	I	1	1	1	1



X = DON'T CARE

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

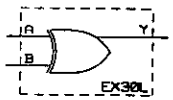
EX30 2-INPUT EXOR; Y

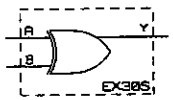
			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->Y	++	207/367	119/208		ps
		−−	117/180	76/136		ps
		+−	125/195	87/149		ps
		−+	178/303	101/165		ps
	B->Y	++	273/418	163/252		ps
		−−	181/299	144/245		ps
		+−	169/300	119/226		ps
		−+	257/397	168/259		ps
k_{fo}, k_{net}	rising Y		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.361	0.515		mA
FAN-IN	A,B		1	1		load
FAN-OUT	Y		18	18		loads
PW			650	500		ps min
f_{max}			600	800		MHz
SIZE			1	1		L cell

B MUST BE DRIVEN BY A MACRO

$Y = A \oplus B$

A	B	I	Y
0	0	I	0
0	1	I	1
1	0	I	1
1	1	I	0





Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

EX31 2-INPUT EXOR/EXNOR; Y, YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->Y	++	376/763	191/395		ps
		−−	198/348	135/211		ps
		+−	206/356	141/221		ps
		−+	336/673	168/341		ps
	B->Y	++	432/787	236/421		ps
		−−	277/445	207/312		ps
		+−	275/418	177/287		ps
		−+	419/771	238/437		ps
	A->YN	++	414/868	204/432		ps
		−−	204/368	137/222		ps
		+−	216/385	146/236		ps
		−+	372/777	181/380		ps
	B->YN	++	467/891	246/458		ps
		−−	283/466	208/321		ps
		+−	286/444	187/296		ps
		−+	455/875	252/477		ps
k_{fo}, k_{net}	rising Y, YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		

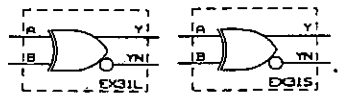
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

EX31 2-INPUT EXOR/EXNOR; Y, YN

	L	S	H	
IEE	0.450	0.604		mA
FAN-IN A,B	1	1		load
FAN-OUT Y,YN	18	18		loads
PW	1150	620		ps min
f_{max}	350	650		MHz
SIZE	2	2		L cells

B MUST BE DRIVEN BY A MACRO

A	B	Y	YN
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF02 D FLIP FLOP, ORed-DATA, ANDed-CLOCK; Q

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C1->Q	--	266/422	230/361		ps
		-+	325/518	239/387		ps
	C2->Q	--	339/526	294/452		ps
		-+	404/623	303/479		ps
k_{fo}, k_{net}	rising Q		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.730	0.883		mA
FAN-IN	C1,C2,D1,D2		1	1		load
FAN-OUT	Q		18	18		loads
T_{su}(D1, D2)			400	400		ps min
T_h (D1, D2)			150	150		ps min
PW (C1, C2)			650	500		ps min
f_{max}			600	800		MHz
SIZE			3	3		L cells

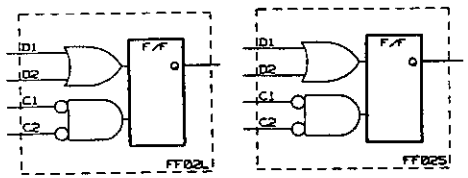
C1, C2 - EACH MUST BE DRIVEN BY A MACRO

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF02 D FLIP FLOP, ORed-DATA, ANDed-CLOCK; Q

D1	D2	C1	C2		Qn+1
X	X	0	0	I	Qn
X	X	1	X	I	Qn
X	X	X	1	I	Qn
1	X	F	0	I	1
X	1	F	0	I	1
1	X	0	F	I	1
X	1	0	F	I	1
0	0	F	0	I	0
0	0	0	F	I	0
X	X	R	0	I	Qn
X	X	0	R	I	Qn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF06 D FLIP FLOP, ORed DATA, ORed CLOCK; Q

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} C1, C2->Q	++	248/426	148/266	144/269	ps
	+-	169/351	122/263	112/248	ps
k_{fo}, k_{net} rising Q		1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
falling		3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:		1.09/1.00	1.09/1.00	1.09/1.00	
IEE		0.636	0.789	1.36	mA
FAN-IN C1,C2,D1,D2,		1	1	1	load
FAN-OUT Q		18	18	18	loads
T_{su}(D1, D2)		300	300	300	ps min
T_h (D1, D2)		50	0	60	ps min
PW (C1, C2)		650	500	310	ps min
f_{max}		600	800	1300	MHz
SIZE		2	2	3	L cells

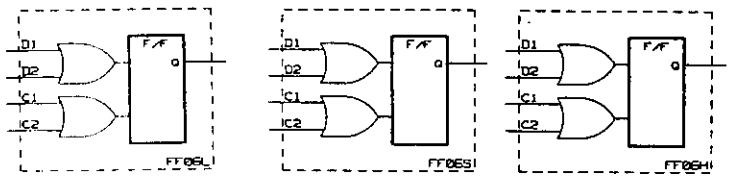
EITHER C1 OR C2 MUST BE DRIVEN BY A MACRO.

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF06 D FLIP FLOP, ORed DATA, ORed CLOCK; Q

D1	D2	C1	C2		Qn+1
X	X	0	0		Qn
X	X	X	1		Qn
X	X	1	X		Qn
1	X	R	0		1
X	1	R	0		1
1	X	0	R		1
X	1	0	R		1
0	0	R	0		0
0	0	0	R		0
X	X	F	0		Qn
X	X	0	F		Qn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF08 D FLIP FLOP, ORed CLOCK, ASYNC. RESET; Q

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C1,C2->Q	++	301/500	177/305		ps
		+−	190/361	131/274		ps
	AR->Q	+−	253/495	171/364		ps
k_{fo}, k_{net}	rising Q		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.729	0.883		mA
FAN-IN	AR,C1,C2,D		1	1		load
FAN-OUT	Q		18	18		loads
T_{su}(D)			350	350		ps min
T_h(D)			0	0		ps min
T_{rec}(AR)			515	515		ps min
PW (AR,C1,C2)			650	500		ps min
f_{max}			600	800		MHz
SIZE			3	3		L cells

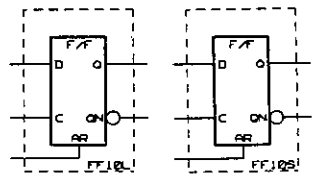
EITHER C1 OR C2 MUST BE DRIVEN BY A MACRO
AR MUST BE DRIVEN BY A MACRO

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF10 D FLIP FLOP, ASYNC. RESET; Q, QN

AR	D	C	I	Qn+1	QNn+1
0	X	0	I	Qn	QNn
0	X	1	I	Qn	QNn
0	0	R	I	0	1
0	1	R	I	1	0
1	X	X	I	0	1
0	X	F	I	Qn	QNn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF08 D FLIP FLOP, ORed CLOCK, ASYNC. RESET; Q

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C1,C2->Q	++	301/500	177/305		ps
		+−	190/361	131/274		ps
	AR->Q	+−	253/495	171/364		ps
k_{fo}, k_{net}	rising Q		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.729	0.883		mA
FAN-IN	AR,C1,C2,D		1	1		load
FAN-OUT	Q		18	18		loads
T_{su}(D)			350	350		ps min
T_h(D)			0	0		ps min
T_{rec}(AR)			515	515		ps min
PW (AR,C1,C2)			650	500		ps min
f_{max}			600	800		MHz
SIZE			3	3		L cells

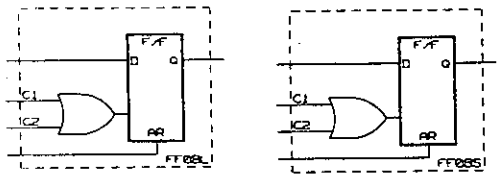
EITHER C1 OR C2 MUST BE DRIVEN BY A MACRO
AR MUST BE DRIVEN BY A MACRO

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF08 D FLIP FLOP, ORed CLOCK, ASYNC. RESET; Q

D	C1	C2	AR	I	Qn+1
X	0	0	0	I	Qn
X	X	1	0	I	Qn
X	1	X	0	I	Qn
1	0	R	0	I	1
1	R	0	0	I	1
0	0	R	0	I	0
0	R	0	0	I	0
X	0	F	0	I	Qn
X	F	0	0	I	Qn
X	X	X	1	I	0

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF10 D FLIP FLOP, ASYNC. RESET; Q, QN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C->Q	++	450/827	249/431		ps
		+−	286/450	180/319		ps
	C->QN	++	451/834	252/434		ps
		+−	297/471	182/333		ps
	AR->Q	+−	345/583	218/409		ps
	AR->QN	++	525/891	311/485		ps
k_{fo}, k_{net}	rising Q, QN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.723	0.876		mA
FAN-IN	AR, C,D		1	1		load
FAN-OUT	Q,QN		18	18		loads
T_{su}(D)			300	300		ps min
T_h (D)			50	50		ps min
T_{rec}(AR)			250	250		ps min
PW (AR,C)			650	500		ps min
f_{max}			600	800		MHz
SIZE			3	3		L cells

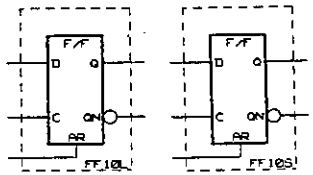
AR, C - EACH MUST BE DRIVEN BY A MACRO

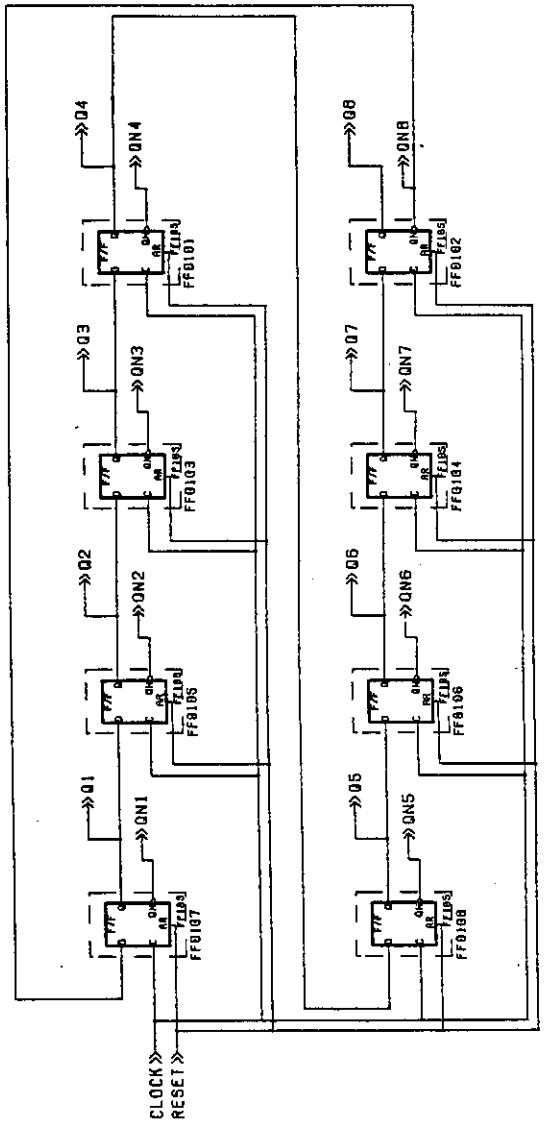
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF10 D FLIP FLOP, ASYNC. RESET; Q, QN

AR	D	C		Qn+1	QNn+1
0	X	0	I	Qn	QNn
0	X	1	I	Qn	QNn
0	0	R	I	0	1
0	1	R	I	1	0
1	X	X	I	0	1
0	X	F	I	Qn	QNn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE





8-BIT COUNTER

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF12 HIGH DENSITY D FLIP FLOP, ASYNC. RESET; Q, QN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C->Q	++		308/529		ps
		+-		199/328		ps
	C->QN	++		276/466		ps
		+-		188/320		ps
	AR->Q	+-		189/341		ps
	AR->QN	++		314/499		ps
k_{fo}, k_{net}	rising Q, QN			1.50/4.65		ps/LU
	falling			2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00		
IEE				0.912		mA
FAN-IN	AR,C,D			1		load
FAN-OUT	Q,QN			18		loads
T_{su}(D)				300		ps min
T_h(D)				50		ps min
T_{rec}				250		ps min
PW (AR,C)				500		ps min
f_{max}				800		MHz
SIZE				2		L cells

AR, C - EACH MUST BE DRIVEN BY A MACRO

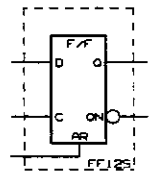
AMCC Q20000 SERIES - FFxx MIL5 (111)

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF12 HIGH DENSITY D FLIP FLOP, ASYNC. RESET; Q, QN

AR	D	C	I	Qn+1	QNn+1
0	X	0	I	Qn	QNn
0	X	1	I	Qn	QNn
0	0	R	I	0	1
0	1	R	I	1	0
1	X	X	I	0	1
0	X	F	I	Qn	QNn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

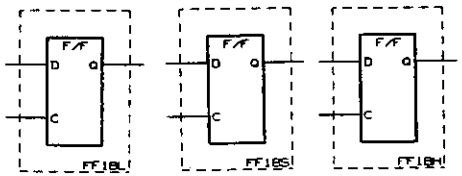
FF18 D FLIP FLOP; Q

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} C->Q	++	252/411	153/261	147/265	ps
	+-	175/331	128/255	119/250	ps
k_{fo}, k_{net} rising Q		1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
falling		3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:		1.09/1.00	1.09/1.00	1.09/1.00	
IEE		0.636	0.789	1.36	mA
FAN-IN C,D		1	1	1	load
FAN-OUT Q		18	18	18	loads
T_{su}(D)		300	300	200	ps min
T_h (D)		50	0	50	ps min
PW (C)		650	500	310	ps min
f_{max}		600	800	1300	MHz
SIZE		2	2	3	L cells

C MUST BE DRIVEN BY A MACRO.
FF19H HAS FASTER DELAYS BUT LONGER Tsu.

D	C	I	Qn+1
X	0	I	Qn
X	1	I	Qn
1	R	I	1
0	R	I	0
X	F	I	Qn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

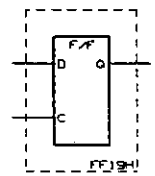
FF19 D FLIP FLOP; Q

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} C->Q	++			147/265	ps
	--			119/250	ps
k_{fo}, k_{net} rising Q				1.20/3.72	ps/LU
falling				2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00	
IEE				1.36	mA
FAN-IN C,D				1	load
FAN-OUT Q				18	loads
T_{su}(D)				200	ps min
T_h (D)				50	ps min
PW (C)				310	ps min
f_{max}				1.3	GHz
SIZE				3	L cells

FF18H AND FF19H ARE IDENTICAL.
FF19H WILL BE OMITTED IN FUTURE LIBRARY RELEASE.
USE FF18L, FF18S FOR L- AND S-OPTION.
C MUST BE DRIVEN BY A MACRO.

D	C	I	Qn+1
X	0	I	Qn
X	1	I	Qn
1	R	I	1
0	R	I	0
X	F	I	Qn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

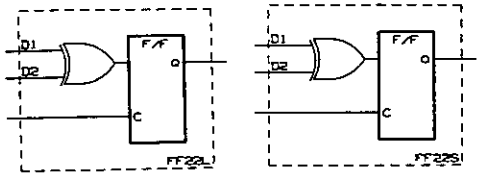
FF22 HIGH-DENSITY FLIP FLOP, EXORed-DATA; Q

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} C->Q	++	294/505	184/336		ps
	+-	209/414	150/323		ps
k_{fo}, k_{net} rising Q		1.95/6.05	1.50/4.65		ps/LU
falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:		1.09/1.00	1.09/1.00		
IEE		0.730	0.883		mA
FAN-IN C,D1,D2		1	1		load
FAN-OUT Q		18	18		loads
T_{su}(D1, D2)		400	400		ps min
T_h (D1, D2)		0	50		ps min
PW (C)		650	500		ps min
f_{max}		600	800		MHz
SIZE		2	2		L cells

C, D2 - EACH MUST BE DRIVEN BY A MACRO.

D1	D2	C	I	Qn+1
X	X	0	I	Qn
X	X	1	I	Qn
0	0	R	I	0
0	1	R	I	1
1	0	R	I	1
1	1	R	I	0
X	X	F	I	Qn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

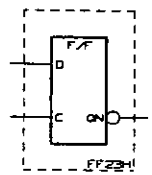
FF23 D FLIP FLOP; QN

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} C->QN	++			165/287	ps
	+-			128/270	ps
k_{fo}, k_{net} rising QN				1.20/3.72	ps/LU
falling				2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00	
IEE				1.36	mA
FAN-IN C,D				1	load
FAN-OUT QN				18	loads
T_{su}(D)				300	ps min
T_h (D)				0	ps min
PW (C)				310	ps min
f_{max}				1.3	GHz
SIZE				3	L cells

C MUST BE DRIVEN BY A MACRO.

D	C	I	QNn+1
X	0	I	Qn
X	1	I	Qn
0	R	I	1
1	R	I	0
X	F	I	Qn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF33 2:1 MUX WITH D FLIP FLOP, ASYNC. RESET; Q, QN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C->Q	++	521/899	303/476	301/483	ps
		+-	350/590	220/418	201/413	ps
	C->QN	++	530/908	309/484	244/416	ps
		+-	350/589	220/417	184/390	ps
	AR->Q	+-	327/585	185/401	201/406	ps
	AR->QN	++	491/913	272/484	246/419	ps
k_{fo}, k_{net} rising Q,QN			1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
falling			3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	1.09/1.00	
IEE			0.818	0.972	1.62	mA
FAN-IN	AR		2	2	2	loads
	C,I0,I1,S1		1	1	1	load
FAN-OUT	Q,QN		18	18	18	loads
T_{su}(I0, I1)			400	400	375	ps min
T_{su}(S1)			450	450	450	ps min
T_h (I0, I1)			100	100	150	ps min
T_h (S1)			50	50	100	ps min
T_{rec}			250	250	250	ps min
PW (AR,C)			650	500	325	ps min
f_{max}			600	800	1300	MHz
SIZE			3	3	4	L cells

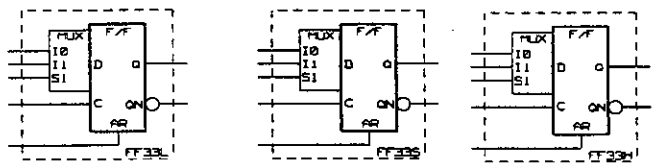
AR, C, S1 - EACH MUST BE DRIVEN BY A MACRO.

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF33 2:1 MUX WITH D FLIP FLOP, ASYNC. RESET; Q, QN

S1	I0	I1	C	AR		Qn+1	QNn+1
X	X	X	0	0	I	Qn	QNn
X	X	X	1	0	I	Qn	QNn
0	0	X	R	0	I	0	1
0	1	X	R	0	I	1	0
1	X	1	R	0	I	1	0
1	X	0	R	0	I	0	1
X	0	0	R	0	I	0	1
X	1	0	R	0	I	UKN	UKN
X	0	1	R	0	I	UKN	UKN
X	1	1	R	0	I	1	0
X	X	X	X	1	I	0	1
X	X	X	F	X	I	Qn	Qn

X = DON'T CARE
UKN = UNKNOWN
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF35 D FLIP FLOP, ASYNC. SET, ASYNC. RESET; Q, QN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C->Q	++	463/841	258/443		ps
		+-	279/440	173/324		ps
	C->QN	++	476/901	264/479		ps
		+-	285/457	182/317		ps
	AR->Q	+-	347/569	216/413		ps
	AR->QN	++	535/965	318/529		ps
	AS->Q	++	521/900	307/490		ps
	AS->QN	+-	363/578	228/409		ps
k_{fo}, k_{net}	rising Q,QN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.818	0.971		mA
FAN-IN	AR,AS,C,D		1	1		load
FAN-OUT	Q,QN		18	18		loads
T_{su}(D)			350	350		ps min
T_h(D)			0	0		ps min
T_{rec}(AR, AS)			650	650		ps min
PW (AR, AS,C)			650	500		ps min
f_{max}			600	800		MHz
SIZE			3	3		L cells

AS, AR, C, D - EACH MUST BE DRIVEN BY A MACRO

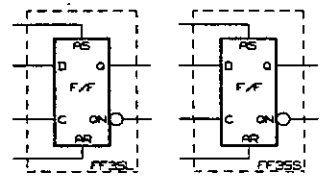
AMCC Q20000 SERIES - FFxx MIL5 (111)

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF35 D FLIP FLOP, ASYNC. SET, ASYNC. RESET; Q, QN

AR	AS	D	C	I	Qn+1	QNn+1
1	0	X	X	I	0	1
0	1	X	X	I	1	0
1	1	X	X	I	UKN	UKN
0	0	X	0	I	Qn	QNn
0	0	X	1	I	Qn	QNn
0	0	0	R	I	0	1
0	0	1	R	I	1	0
X	X	X	F	I	Qn	QNn

X = DON'T CARE
UKN = UNKNOWN
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

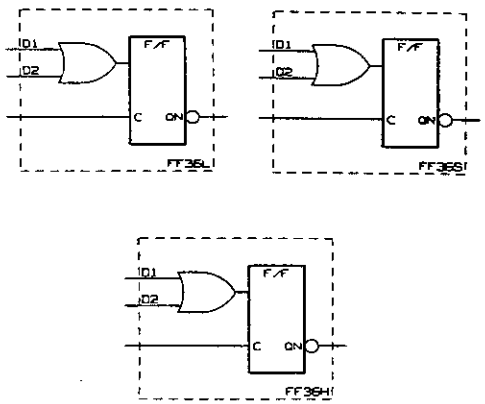
FF36 D FLIP FLOP, ORed-DATA, QN

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} C->QN	++	305/485	188/306	165/287	ps
	+−	184/349	132/265	128/270	ps
k_{fo}, k_{net} rising QN		1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
falling		3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:		1.09/1.00	1.09/1.00	1.09/1.00	
IEE		0.636	0.789	1.36	mA
FAN-IN C,D1,D2		1	1	1	load
FAN-OUT QN		18	18	18	loads
T_{su}(D1, D2)		300	300	300	ps min
T_h (D1, D2)		0	0	0	ps min
PW (C)		650	500	310	ps min
f_{max}		600	800	1300	MHz
SIZE		2	2	3	L cells

C MUST BE DRIVEN BY A MACRO.

D1+D2	C	I	QNn+1
X	0	I	QNn
X	1	I	QNn
0	R	I	1
1	R	I	0
X	F	I	QNn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

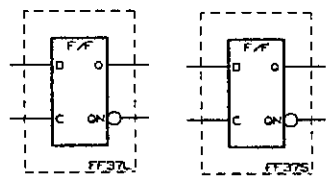
FF37 D FLIP FLOP; Q, QN

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} C->Q	++	453/843	249/436		ps
	+−	295/458	182/320		ps
C->QN	++	504/956	272/490		ps
	+−	307/490	193/329		ps
k_{fo}, k_{net} rising Q, QN		1.95/6.05	1.50/4.65		ps/LU
falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:		1.09/1.00	1.09/1.00		
IEE		0.629	0.783		mA
FAN-IN C,D		1	1		load
FAN-OUT Q,QN		18	18		loads
T_{su}(D)		300	300		ps min
T_h (D)		50	50		ps min
PW (C)		650	500		ps min
f_{max}		600	800		MHz
SIZE		2	2		L cells

C MUST BE DRIVEN BY A MACRO
USE FF38H FOR H-OPTION

D	C	I	Qn+1	QNn+1
X	0	I	Qn	QNn
X	1	I	Qn	QNn
1	R	I	1	0
0	R	I	0	1
X	F	I	Qn	QNn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

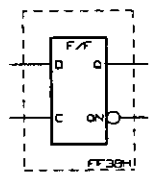
FF38 D FLIP FLOP; Q, QN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C->Q	++			194/311	ps
		+−			130/270	ps
	C->QN	++			229/350	ps
		+−			134/275	ps
k_{fo}, k_{net}	rising Q, QN				1.20/3.72	ps/LU
	falling				2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:					1.09/1.00	
IEE					1.27	mA
FAN-IN	C,D				1	load
FAN-OUT	Q,QN				18	loads
T_{su}(D)					300	ps min
T_h(D)					100	ps min
PW (C)					350	ps min
f_{max}					1200	MHz
SIZE					3	L cells

C MUST BE DRIVEN BY A MACRO
USE FF37L, FF37S FOR L- AND S-OPTION

D	C	I	Qn+1	QNn+1
X	0	I	Qn	QNn
X	1	I	Qn	QNn
1	R	I	1	0
0	R	I	0	1
X	F	I	Qn	QNn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

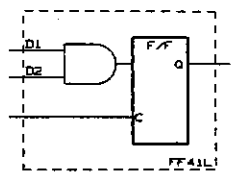
FF41 D FLIP FLOP, ANDed-DATA; Q

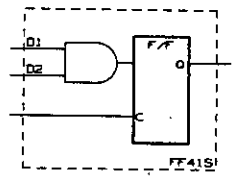
			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C->Q	++	295/484	173/304		ps
		+−	202/396	141/298		ps
k_{fo}, k_{net}	rising Q		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.728	0.882		mA
FAN-IN	C,D1,D2		1	1		load
FAN-OUT	Q		18	18		loads
T_{su}(D1, D2)			400	400		ps min
T_h(D1, D2)			0	0		ps min
PW (C)			650	500		ps min
f_{max}			600	800		MHz
SIZE			2	2		L cells

C, D2 - EACH MUST BE DRIVEN BY A MACRO

D1	D2	C	I	Qn+1
0	0	R	I	0
0	1	R	I	0
1	0	R	I	0
1	1	R	I	1
X	X	0	I	Qn
X	X	1	I	Qn
X	X	F	I	Qn

X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE





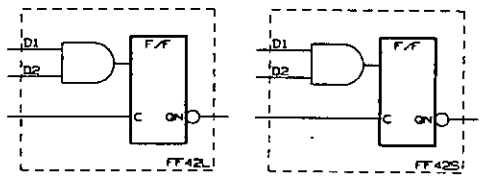
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF42 D FLIP FLOP, ANDed-DATA; QN

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} C->QN	++	299/492	175/313		ps
	+−	199/387	138/289		ps
k_{fo}, k_{net} rising QN		1.95/6.05	1.50/4.65		ps/LU
falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:		1.09/1.00	1.09/1.00		
IEE		0.730	0.881		mA
FAN-IN C,D1,D2		1	1		load
FAN-OUT QN		18	18		loads
T_{su}(D1, D2)		400	400		ps min
T_h (D1, D2)		0	0		ps min
PW (C)		650	500		ps min
f_{max}		600	800		MHz
SIZE		2	2		L cells

C, D2 - EACH MUST BE DRIVEN BY A MACRO

D1	D2	C	I	QNn+1
0	0	R	I	1
0	1	R	I	1
1	0	R	I	1
1	1	R	I	0
X	X	0	I	QNn
X	X	1	I	QNn
X	X	F	I	QNn



X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE

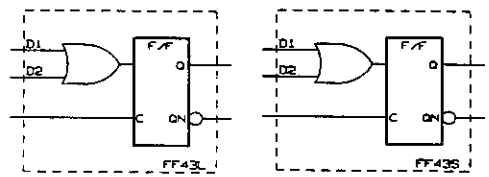
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF43 D FLIP FLOP, OR-DATA; Q, QN

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} C->Q	++	453/844	249/436		ps
	+−	295/461	182/321		ps
C->QN	++	504/956	272/490		ps
	+−	306/490	193/329		ps
k_{fo}, k_{net} rising Q, QN		1.95/6.05	1.50/4.65		ps/LU
falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:		1.09/1.00	1.09/1.00		
IEE		0.628	0.783		mA
FAN-IN C,D1,D2		1	1		load
FAN-OUT Q,QN		18	18		loads
T_{su}(D1, D2)		300	300		ps min
T_h (D1, D2)		50	50		ps min
PW (C)		650	500		ps min
f_{max}		600	800		MHz
SIZE		2	2		L cells

C, D2 - EACH MUST BE DRIVEN BY A MACRO

D1	D2	C	I	Qn+1	QNn+1
X	X	0	I	Qn	QNn
X	X	1	I	Qn	QNn
1	X	R	I	1	0
X	1	R	I	1	0
0	0	R	I	0	1
X	X	F	I	Qn	QNn



X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF46 2 :1 MUX WITH D FLIP FLOP, ASYNC. RESET; Q

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C->Q	++	365/608	221/399		ps
		+-	259/503	179/383		ps
	AR->Q	+-	229/503	146/376		ps
k_{fo}, k_{net}	rising Q		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.822	1.26		mA
FAN-IN	AR		2	2		loads
	C,I0,I1,S1		1	1		load
FAN-OUT	Q		18	18		loads
T_{su}(I0, I1)			400	400		ps min
T_{su}(S1)			450	450		ps min
T_h (I0, I1)			200	200		ps min
T_h (S1)			0	0		ps min
T_{rec}			420	420		ps min
PW (AR, C)			650	500		ps min
f_{max}			600	800		MHz
SIZE			3	3		L cells

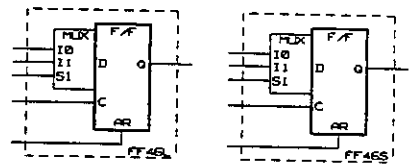
C, S1, AR - EACH MUST BE DRIVEN BY A MACRO.

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF46 2:1 MUX WITH D FLIP FLOP, ASYNC. RESET; Q

S1	I1	I0	C	AR	I	Qn+1
X	X	X	0	0	I	Qn
X	X	X	1	0	I	Qn
0	X	0	R	0	I	0
0	X	1	R	0	I	1
1	0	X	R	0	I	0
1	1	X	R	0	I	1
X	0	0	R	0	I	0
X	1	0	R	0	I	UKN
X	0	1	R	0	I	UKN
X	1	1	R	0	I	1
X	X	X	R	1	I	0
X	X	X	F	X	I	Qn

X = DON'T CARE
UKN = UNKNOWN
R = RISING EDGE
F = FALLING EDGE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF48 3 :1 MUX WITH D FLIP FLOP, Q

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} C->Q	++	319/578	171/340		ps
	+-	238/496	151/347		ps
k_{fo}, k_{net} rising Q		1.95/6.05	1.50/4.65		ps/LU
falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:		1.09/1.00	1.09/1.00		
IEE		0.986	1.137		mA
FAN-IN C,I0,I1,I2		1	1		load
S0,S1		2	2		loads
FAN-OUT Q		18	18		loads
T_{su}(I0, I1, I2)		400	400		ps min
T_{su}(S0, S1)		450	450		ps min
T_h (I0, I1, I2, S0, S1)		0	0		ps min
PW (C)		650	500		ps min
f_{max}		600	800		MHz
SIZE		3	3		L cells

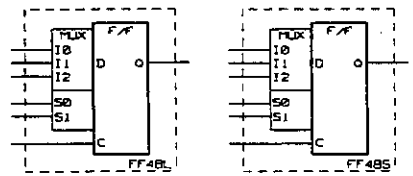
C, S0, S1 - EACH MUST BE DRIVEN BY A MACRO.

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

FF48 3:1 MUX WITH D FLIP FLOP, Q

S0	S1	I0	I1	I2	C		Qn+1
X	X	X	X	X	0	|	Qn
X	X	X	X	X	1	|	Qn
0	0	0	X	X	R	|	0
0	0	1	X	X	R	|	1
1	0	X	0	X	R	|	0
1	0	X	1	X	R	|	1
0	1	X	X	0	R	|	0
0	1	X	X	1	R	|	1
1	1	X	X	X	R	|	1
0	X	1	X	1	R	|	1
0	X	0	X	0	R	|	0
X	0	1	1	X	R	|	1
X	0	0	0	X	R	|	0
X	X	X	X	X	F	|	Qn

X = DON'T CARE
R = RISING EDGE
F = FALLING



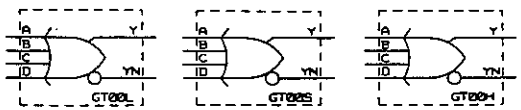
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT00 4-INPUT OR/NOR; Y, YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i->Y	++	298/677	141/339	115/264	ps
		−−	211/365	126/215	84/153	ps
	i->YN	+−	183/344	117/208	78/153	ps
		−+	416/958	196/459	139/296	ps
	i = A or B or C or D					
k_{fo}, k_{net}	rising Y,YN		1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
	falling		3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	1.09/1.00	
IEE			0.357	0.507	0.691	mA
FAN-IN	A,B,C,D		1	1	1	load
FAN-OUT	Y,YN		18	18	18	loads
PW			1150	620	450	ps min
f_{max}			350	650	900	MHz
SIZE			2	2	2	L cells

$Y = A + B + C + D$

$YN = \overline{A + B + C + D}$

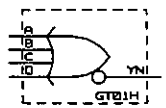


Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT01 4-INPUT NOR; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i->YN	+−			57/124	ps
		−+			93/178	ps
	i = A or B or C or D					
k_{fo}, k_{net}	rising YN				1.20/3.72	ps/LU
	falling				2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:					1.09/1.00	
IEE					0.603	mA
FAN-IN	A,B,C,D				1	load
FAN-OUT	YN				18	loads
PW					350	ps min
f_{max}					1.2	GHz
SIZE					1	L cell

$YN = \overline{A + B + C + D}$

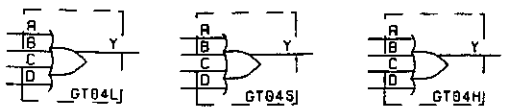


Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT04 4-INPUT OR

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i->Y	++	126/278	73/162	65/147	ps
		--	91/166	58/122	46/96	ps
	i = A or B or C or D					
k_{fo}, k_{net}	rising Y		1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
	falling		3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	1.09/1.00	
IEE			0.266	0.420	0.602	mA
FAN-IN	A,B,C,D		1	1	1	load
FAN-OUT	Y		18	18	18	loads
PW			650	500	350	ps min
f_{max}			600	800	1200	MHz
SIZE			1	1	1	L cell

$Y = A + B + C + D$



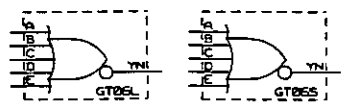
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT06 5-INPUT NOR; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i->YN	+-	92/217	73/173		ps
		-+	218/442	166/390		ps
	i = A or B or C or D or E					
k_{fo}, k_{net}	rising YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.361	0.515		mA
FAN-IN	A;B,C,D,E		1	1		load
FAN-OUT	YN		18	18		loads
PW			650	500		ps min
f_{max}			600	800		MHz
SIZE			2	2		L cells

A, B, C, D, E - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$YN = \overline{A + B + C + D + E}$



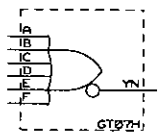
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT07 6-INPUT NOR; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i->YN	+−			83/137	ps
		−+			109/176	ps
	i = A or B or C or D or E or F					
k_{fo}, k_{net}	rising YN				1.20/3.72	ps/LU
	falling				2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:					1.09/1.00	
IEE					0.959	mA
FAN-IN	A,B,C,D,E,F				1	load
FAN-OUT	YN				18	loads
PW					350	ps min
f_{max}					1200	MHz
SIZE					2	L cells

A, B, C - AT LEAST ONE MUST BE DRIVEN BY A MACRO
D, E, F - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$YN = \overline{A + B + C + D + E + F}$

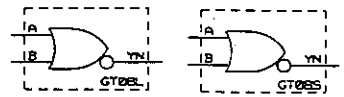


Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT08 2-INPUT NOR; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i->YN	+−	103/186	72/141		ps
		−+	163/285	88/152		ps
	i = A or B					
k_{fo}, k_{net}	rising YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.265	0.421		mA
FAN-IN	A,B		1	1		load
FAN-OUT	YN		18	18		loads
PW			650	500		ps min
f_{max}			600	800		MHz
SIZE			1	1		L cell

$YN = \overline{A + B}$

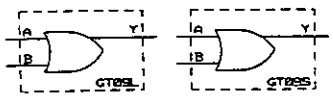


Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT09 2-INPUT OR; Y

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i->Y	++	145/267	88/161		ps
		−−	107/188	69/138		ps
	i = A or B					
k_{fo}, k_{net}	rising Y		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.268	0.422		mA
FAN-IN	A,B		1	1		load
FAN-OUT	Y		18	18		loads
PW			650	500		ps min
f_{max}			600	800		MHz
SIZE			1	1		L cell

Y = A + B



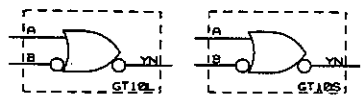
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT10 2-INPUT NOR, WITH ONE INVERTED INPUT; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->YN	+−	106/171	82/140		ps
		−+	150/232	94/146		ps
	B->YN	++	227/353	149/236		ps
		−−	152/262	134/228		ps
k_{fo}, k_{net}	rising YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.361	0.515		mA
FAN-IN	A,B		1	1		load
FAN-OUT	YN		18	18		loads
PW			650	500		ps min
f_{max}			600	800		MHz
SIZE			1	1		L cell

B MUST BE DRIVEN BY A MACRO

$YN = \overline{A + \overline{B}}$



A	B	I	YN
0	0	I	0
1	0	I	0
0	1	I	1
1	1	I	0

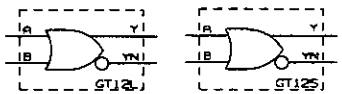
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT12 2-INPUT OR/NOR; Y, YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i->Y	++	313/673	155/337		ps
		−−	194/333	123/196		ps
	i->YN	+−	178/324	120/200		ps
		−+	369/793	177/382		ps
	i = A or B					
k_{fo}, k_{net}	rising Y,YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.357	0.510		mA
FAN-IN A,B			1	1		load
FAN-OUT Y,YN			18	18		loads
PW			1150	620		ps min
f_{max}			350	650		MHz
SIZE			2	2		L cells

$Y = A + B$

$YN = \overline{A + B}$

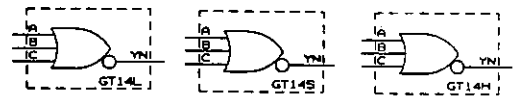


Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT14 3-INPUT NOR; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i->YN	+−	101/186	70/140	55/119	ps
		−+	178/363	97/189	80/149	ps
	i = A or B or C					
k_{fo}, k_{net}	rising YN		1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
	falling		3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	1.09/1.00	
IEE			0.268	0.421	0.604	mA
FAN-IN A,B,C			1	1	1	load
FAN-OUT YN			18	18	18	loads
PW			650	500	310	ps min
f_{max}			600	800	1300	MHz
SIZE			1	1	1	L cell

$YN = \overline{A + B + C}$



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT30 DUAL 2-INPUT AND, WITH ONE INPUT INVERTED; Y0, Y1

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A0->Y0	++	199/339	116/194	104/162	ps
		−−	111/172	73/129	59/107	ps
	B0->Y0	+−	173/294	123/228	103/198	ps
		−+	235/361	135/205	106/172	ps
	A1->Y1	++	199/339	116/195	104/163	ps
		−−	110/171	73/130	60/107	ps
	B1->Y1	+−	173/294	123/228	103/198	ps
		−+	235/362	136/205	106/173	ps
k_{fo}, k_{net}	rising Y0,Y1		1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
	falling		3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	1.09/1.00	
IEE			0.721	1.20	1.72	mA
FAN-IN	A0,B0,A1,B1		1	1	1	load
FAN-OUT	Y0,Y1		18	18	18	loads
PW			650	500	310	ps min
f_{max}			600	800	1300	MHz
SIZE			2	2	3	L cells

B0, B1 - EACH MUST BE DRIVEN BY A MACRO.

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT30 DUAL 2-INPUT AND, WITH ONE INPUT INVERTED; Y0, Y1

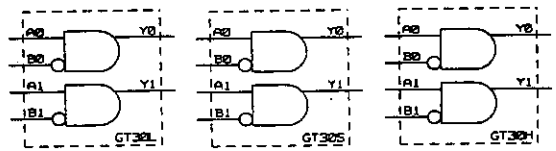
$Y0 = A0 * \overline{B0}$

$Y1 = A1 * \overline{B1}$

* = AND

A0	B0	I	Y0
0	0	I	0
0	1	I	0
1	0	I	1
1	1	I	0

A1	B1	I	Y1
0	0	I	0
0	1	I	0
1	0	I	1
1	1	I	0



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

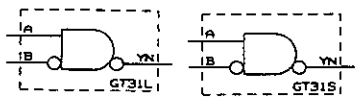
GT31 2-INPUT NAND WITH ONE INPUT INVERTED; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->YN	+−	109/168	80/133		ps
		−+	195/315	116/181		ps
	B->YN	++	273/413	169/261		ps
		−−	157/260	109/186		ps
k_{fo}, k_{net}	rising YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.447	0.679		mA
FAN-IN	A		2	2		loads
	B		1	1		load
FAN-OUT	YN		18	18		loads
PW			650	500		ps min
f_{max}			600	800		MHz
SIZE			1	1		L cell

B MUST BE DRIVEN BY A MACRO

$YN = \overline{A * \overline{B}}$

A	B	I	YN
0	0	I	1
0	1	I	1
1	0	I	0
1	1	I	1



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT32 2-INPUT AND/NAND; Y, YN

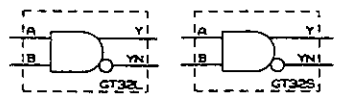
			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->Y	++	395/808	197/405		ps
		−−	201/363	135/222		ps
	A->YN	+−	195/325	136/205		ps
		−+	312/618	160/321		ps
	B->Y	++	437/834	238/439		ps
		−−	284/481	207/328		ps
	B->YN	+−	245/377	162/274		ps
		−+	400/731	232/422		ps
k_{fo}, k_{net}	rising Y,YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.450	0.604		mA
FAN-IN	A,B		1	1		load
FAN-OUT	Y,YN		18	18		loads
PW			1150	620		ps min
f_{max}			350	650		MHz
SIZE			2	2		L cells

B MUST BE DRIVEN BY A MACRO

$Y = A * B$

$YN = \overline{A * B}$

* = AND



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

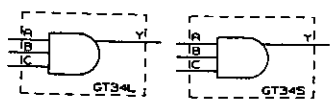
GT34 3-INPUT AND; Y

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->Y	++	229/384	131/222		ps
		−−	133/202	87/149		ps
	B->Y	++	285/432	174/266		ps
		−−	227/345	180/277		ps
	C->Y	++	320/505	197/326		ps
		−−	275/418	215/337		ps
k_{fo}, k_{net}	rising Y		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.457	0.611		mA
FAN-IN	A,B,C		1	1		load
FAN-OUT	Y		18	18		loads
PW			650	500		ps min
f_{max}			600	800		MHz
SIZE			2	2		L cells

B, C - EACH MUST BE DRIVEN BY A MACRO

Y = A * B * C

* = AND



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT38 3-INPUT AND/NAND; Y, YN

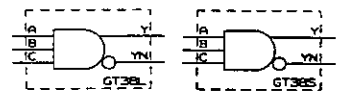
			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->Y	++	381/745	189/374		ps
		−−	204/367	133/214		ps
	A->YN	+−	212/360	139/214		ps
		−+	340/697	162/333		ps
	B->Y	++	434/778	234/412		ps
		−−	296/502	216/343		ps
	B->YN	+−	266/401	167/279		ps
		−+	434/824	242/452		ps
	C->Y	++	485/833	273/449		ps
		−−	349/568	255/396		ps
	C->YN	+−	311/501	195/353		ps
		−+	498/902	287/507		ps
k_{fo}, k_{net}	rising Y,YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.545	0.698		mA
FAN-IN	A,B,C		1	1		load
FAN-OUT	Y,YN		18	18		loads
PW			1150	620		ps min
f_{max}			350	650		MHz
SIZE			2	2		L cells

B, C - EACH MUST BE DRIVEN BY A MACRO

Y = A * B * C

YN = $\overline{A * B * C}$

* = AND



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

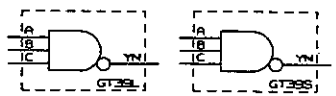
GT39 3-INPUT NAND; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->YN	+–	118/192	88/151		ps
		–+	152/239	94/147		ps
	B->YN	+–	154/287	116/226		ps
		–+	252/380	182/288		ps
	C->YN	+–	192/383	145/302		ps
		–+	303/469	230/354		ps
k_{fo}, k_{net}	rising YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.456	0.609		mA
FAN-IN	A,B,C		1	1		load
FAN-OUT	YN		18	18		loads
PW			650	500		ps min
f_{max}			600	800		MHz
SIZE			2	2		L cells

B, C - EACH MUST BE DRIVEN BY A MACRO
USE GT40H AS THE H-OPTION

$YN = \overline{A * B * C}$

* = AND



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

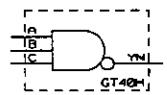
GT40 HIGH SPEED 3-INPUT NAND; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->YN	+–			68/123	ps
		–+			64/98	ps
	B->YN	+–			102/216	ps
		–+			107/169	ps
	C->YN	+–			139/314	ps
		–+			132/210	ps
k_{fo}, k_{net}	rising YN				1.20/3.72	ps/LU
	falling				2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:					1.09/1.00	
IEE					1.05	mA
FAN-IN	A,B				2	loads
	C				1	load
FAN-OUT	YN				18	loads
PW					350	ps min
f_{max}					1.2	GHz
SIZE					2	L cells

B, C - EACH MUST BE DRIVEN BY A MACRO.
USE GT39L, GT39S AS THE L AND S OPTIONS.

$YN = \overline{A * B * C}$

* = AND



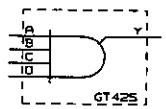
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT42 HIGH SPEED 4-INPUT AND; Y

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->Y	++		180/295		ps
		−−		152/262		ps
	B->Y	++		175/285		ps
		−−		150/257		ps
	C->Y	++		174/283		ps
		−−		149/256		ps
	D->Y	++		169/274		ps
		−−		147/251		ps
k_{fo}, k_{net}	rising Y			1.50/4.65		ps/LU
	falling			2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00		
IEE				3.02		mA
FAN-IN	A,B,C,D			1		load
FAN-OUT	Y			18		loads
PW				500		ps min
f_{max}				800		MHz
SIZE				5		L cells

Y = A * B * C * D

* = AND



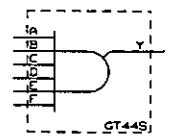
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT44 HIGH SPEED 6-INPUT AND; Y

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->Y	++		213/325		ps
		−−		150/280		ps
	B->Y	++		210/322		ps
		−−		148/276		ps
	C->Y	++		210/322		ps
		−−		148/276		ps
	D->Y	++		257/429		ps
		−−		152/288		ps
	E->Y	++		257/429		ps
		−−		152/288		ps
	F->Y	++		258/430		ps
		−−		153/289		ps
k_{fo}, k_{net}	rising Y			1.50/4.65		ps/LU
	falling			2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:				1.09/1.00		
IEE				4.58		mA
FAN-IN	A,B,C,D,E,F			1		load
FAN-OUT	Y			18		loads
PW				500		ps min
f_{max}				800		MHz
SIZE				7		L cells

Y = A * B * C * D * E * F

* = AND



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

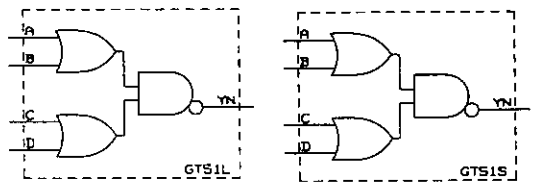
GT51 2-WIDE 2-2 INPUT OR/AND; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->YN	+−	104/159	76/125		ps
		−+	182/297	109/173		ps
	B->YN	+−	115/185	85/146		ps
		−+	162/262	97/155		ps
	C->YN	+−	140/251	108/203		ps
		−+	255/389	176/269		ps
	D->YN	+−	152/281	116/222		ps
		−+	260/399	184/289		ps
k_{fo}, k_{net}	rising YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.361	0.515		mA
FAN-IN	A,B,C,D		1	1		load
FAN-OUT	YN		18	18		loads
PW			650	500		ps min
f_{max}			600	800		MHz
SIZE			1	1		L cell

C, D - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$YN = \overline{(A + B) * (C + D)}$

* = AND



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

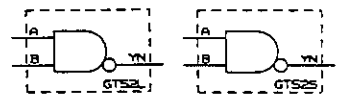
GT52 2-INPUT NAND; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->YN	+−	105/172	80/139		ps
		−+	139/215	88/136		ps
	B->YN	+−	139/259	108/209		ps
		−+	209/329	156/237		ps
k_{fo}, k_{net}	rising YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.361	0.515		mA
FAN-IN	A,B		1	1		load
FAN-OUT	YN		18	18		loads
PW			650	500		ps min
f_{max}			600	800		MHz
SIZE			1	1		L cell

B MUST BE DRIVEN BY A MACRO
USE GT53H AS THE H-OPTION

$YN = \overline{A * B}$

* = AND



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

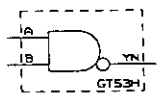
GT53 HIGH SPEED 2-INPUT NAND; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	A->YN	+−			69/121	ps
		−+			75/114	ps
	B->YN	+−			100/204	ps
		−+			123/197	ps
k_{fo}, k_{net}	rising YN				1.20/3.72	ps/LU
	falling				2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:					1.09/1.00	
IEE					0.931	mA
FAN-IN	A				2	loads
	B				1	load
FAN-OUT	YN				18	loads
PW					350	ps min
f_{max}					1200	MHz
SIZE					2	L cells

B MUST BE DRIVEN BY A MACRO
USE GT52L, GT52S AS THE L AND S OPTIONS

$YN = \overline{A * B}$

* = AND

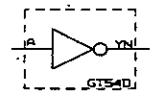


Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT54D INVERTING SUPER DRIVER; YN

			D MIN/MAX	
T_{pd}	A->YN	+−	84/150	ps
		−+	92/147	ps
k_{fo}, k_{net}	rising YN		0.90/2.79	ps/LU
	falling		1.25/3.88	ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	
IEE			0.842	mA
FAN-IN	A		2	loads
FAN-OUT	YN		32	loads
PW			350	ps min
f_{max}			1200	MHz
SIZE			2	L cells

$YN = \overline{A}$

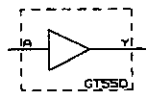


Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT55D NON-INVERTING SUPER DRIVER; Y

		D MIN/MAX	
T_{pd} A->Y	++	125/194	ps
	−−	89/159	ps
k_{fo}, k_{net} rising Y		0.90/2.79	ps/LU
falling		1.25/3.88	ps/LU
MIL4 ADJ. FACTOR:		1.09/1.00	
IEE		1.02	mA
FAN-IN A		1	load
FAN-OUT Y		32	loads
PW		350	ps min
f_{max}		1200	MHz
SIZE		2	L cells

Y = A



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

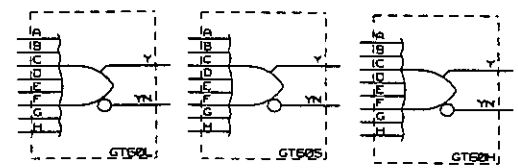
GT60 8-INPUT OR/NOR; Y, YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i->Y	++	282/649	155/366	135/284	ps
		−−	274/500	145/238	100/171	ps
	i->YN	+−	162/348	103/223	80/192	ps
		−+	452/925	180/351	147/264	ps
i = A or B or C or D or E or F or G or H						
k_{fo}, k_{net}	rising Y,YN		1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
	falling		3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	1.09/1.00	
IEE			0.506	0.865	1.20	mA
FAN-IN	i		1	1	1	load
	i = A,B,C,D,E,F,G,H					
FAN-OUT	Y,YN		18	18	18	loads
PW			1150	620	450	ps min
f_{max}			350	650	900	MHz
SIZE			3	3	3	L cells

A, B, C, D - AT LEAST ONE MUST BE DRIVEN BY A MACRO
E, F, G, H - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$Y = A + B + C + D + E + F + G + H$

$YN = \overline{A + B + C + D + E + F + G + H}$



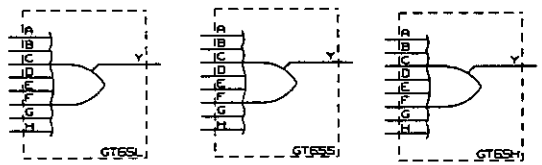
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GT65 8-INPUT OR; Y

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i->Y	++	142/308	93/205	88/192	ps
		−−	175/296	100/185	76/139	ps
	i = A or B or C or D or E or F or G or H					
k_{fo}, k_{net}	rising Y		1.95/6.05	1.50/4.65	1.20/3.72	ps/LU
	falling		3.25/10.08	2.50/7.75	2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00	1.09/1.00	
IEE			0.455	0.776	1.12	mA
FAN-IN	A,B,C,D,E,F,G,H		1	1	1	load
FAN-OUT	Y		18	18	18	loads
PW			650	500	350	ps min
f_{max}			600	800	1200	MHz
SIZE			3	3	3	L cells

A, B, C, D - AT LEAST ONE MUST BE DRIVEN BY A MACRO
E, F, G, H - AT LEAST ONE MUST BE DRIVEN BY A MACRO

Y = A + B + C + D + E + F + G + H



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

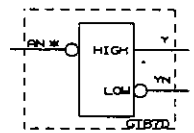
GT87D STATIC DRIVER LOW, HIGH; Y, YN

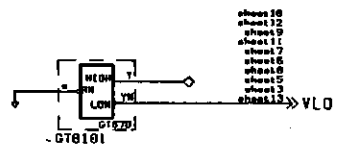
		D MIN/MAX	
T_{pd}	AN->Y,YN	000/000	ps
k_{fo}, k_{net}	rising Y,YN	0.90/2.79	ps/LU
	falling	1.25/3.88	ps/LU
MIL4 ADJ. FACTOR:		1.09/1.00	
IEE		0.453	mA
FAN-IN	AN	1	load
FAN-OUT	Y,YN	50	loads
SIZE		1	L cell

AN MUST BE TIED TO GROUND

Y = 1

YN = 0





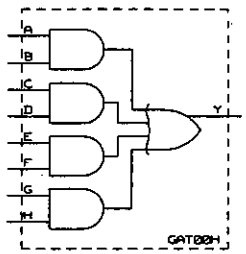
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GAT00 QUAD 2-INPUT AND -4-INPUT OR

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i1->Y	++			172/319	ps
		−−			133/258	ps
	i2->Y	++			198/386	ps
		−−			163/313	ps
	i1 = A or C or E or G i2 = B or D or F or H					
k_{fo}, k_{net}	rising Y				1.20/3.72	ps/LU
	falling				2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:					1.09/1.00	
IEE					3.72	mA
FAN-IN A,B,C,D,E,F,G,H					1	load
FAN-OUT Y					18	loads
PW					350	ps min
f_{max}					1200	MHz
SIZE					6	L cells

B, D, F, H - EACH MUST BE DRIVEN BY A MACRO

$Y = (A * B) + (C * D) + (E * F) + (G * H)$

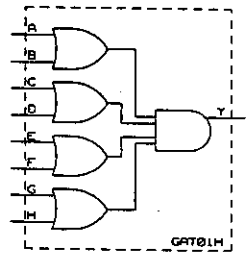


Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

GAT01 QUAD 2-INPUT OR -4-INPUT AND

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	i->Y	++			178/295	ps
		−−			146/270	ps
	i = A or B or C or D or E or F or G or H					
k_{fo}, k_{net}	rising Y				1.20/3.72	ps/LU
	falling				2.00/6.20	ps/LU
MIL4 ADJ. FACTOR:					1.09/1.00	
IEE					3.02	mA
FAN-IN A,B,C,D,E,F,G,H					1	load
FAN-OUT Y					18	loads
PW					350	ps min
f_{max}					1200	MHz
SIZE					5	L cells

$Y = (A + B) * (C + D) * (E + F) * (G + H)$



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

LA01 D-LATCH, TRANSPARENT HIGH; Q, QN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C->Q	++	460/865	248/445		ps
		+−	315/518	205/327		ps
	C->QN	++	469/871	257/457		ps
		+−	270/444	171/305		ps
	D->Q	++	419/887	211/412		ps
		−−	223/398	145/226		ps
	D->QN	+−	215/365	144/225		ps
		−+	384/758	188/371		ps
k_{fo}, k_{net}	rising Q,QN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.450	0.603		mA
FAN-IN	C,D		1	1		load
FAN-OUT	Q,QN		18	18		loads
T_{su}(D)			650	400		ps min
T_h(D)			50	50		ps min
PW (C)			650	500		ps min
f_{max}			600	800		MHz
SIZE			2	2		L cells

C MUST BE DRIVEN BY A MACRO

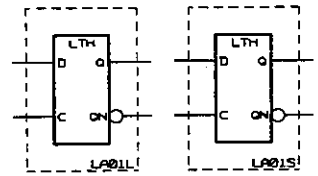
AMCC Q20000 SERIES - LAxx MIL5 (111)

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

LA01 D-LATCH, TRANSPARENT HIGH; Q, QN

D	C	I	Qn+1	QNn+1	
1	1	I	1	0	TRANSPARENT
0	1	I	0	1	TRANSPARENT
X	0	I	Qn	QNn	

X = DON'T CARE



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

LA11 D-LATCH, TRANSPARENT HIGH; Q

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C->Q	++	271/415	151/249		ps
		+−	207/356	135/257		ps
	D->Q	++	228/372	123/191		ps
		−−	134/227	82/154		ps
k_{fo}, k_{net}	rising Q		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.00/1.00	1.00/1.00		
IEE			0.456	0.610		mA
FAN-IN	C,D		1	1		load
FAN-OUT	Q		18	18		loads
T_{su}(D)			500	350		ps min
T_h(D)			50	50		ps min
PW (C)			650	500		ps min
f_{max}			600	800		MHz
SIZE			1	1		L cell

C MUST BE DRIVEN BY A MACRO

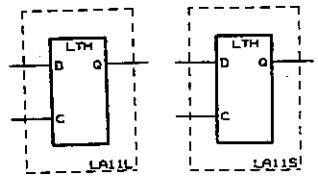
AMCC Q20000 SERIES - LAxx MIL5 (111)

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

LA11 D-LATCH, TRANSPARENT HIGH; Q

D	C	I	Qn+1	
1	1	I	1	TRANSPARENT
0	1	I	0	TRANSPARENT
X	0	I	Qn	

X = DON'T CARE

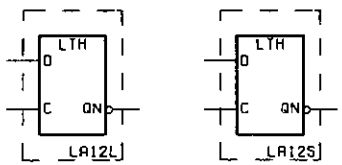


Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

LA12 D-LATCH, TRANSPARENT HIGH; QN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	C->QN	++	225/355	134/222		ps
		+-	142/264	102/204		ps
	D->QN	+-	109/178	77/135		ps
		-+	159/249	87/133		ps
k_{fo}, k_{net}	rising QN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.456	0.609		mA
FAN-IN	C,D		1	1		load
FAN-OUT	QN		18	18		loads
T_{su}(D)			500	400		ps min
T_h (D)			50	50		ps min
PW (C)			650	500		ps min
f_{max}			600	800		MHz
SIZE			1	1		L cell

C MUST BE DRIVEN BY A MACRO.



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

LA12 D-LATCH, TRANSPARENT HIGH; QN

D	C	I	QNn+1	
1	1	I	0	TRANSPARENT
0	1	I	1	TRANSPARENT
X	0	I	QNn	

X = DON'T CARE

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

MX13 2:1 MUX; Y

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	I0->Y	++	189/305	110/176		ps
		−−	110/178	73/132		ps
	I1->Y	++	190/305	111/177		ps
		−−	109/177	72/132		ps
	S1->Y	++	236/369	144/234		ps
		−−	190/307	148/245		ps
		+−	181/317	124/233		ps
		−+	227/354	159/243		ps
k_{fo}, k_{net}	rising Y		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.341	0.495		mA
FAN-IN	I0, I1, S1		1	1		load
FAN-OUT	Y		18	18		loads
PW			650	500		ps min
f_{max}			600	800		MHz
SIZE			1	1		L cell

S1 MUST BE DRIVEN BY A MACRO

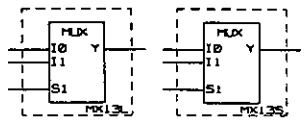
AMCC Q20000 SERIES - MXxx MIL5 (111)

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

MX13 2:1 MUX; Y

S1	I1	I0		Y
0	X	0	I	0
0	X	1	I	1
1	0	X	I	0
1	1	X	I	1
X	0	0	I	0
X	1	1	I	1
X	0	1	I	UKN
X	1	0	I	UKN

X = DON'T CARE
UKN = UNKNOWN



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

MX18 2:1 MUX; Y, YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	I0->Y	++	350/686	174/345		ps
		−−	195/339	126/197		ps
	I0->YN	+−	202/346	131/203		ps
		−+	351/728	168/351		ps
	I1->Y	++	352/686	175/345		ps
		−−	193/337	125/196		ps
	I1->YN	+−	203/347	132/204		ps
		−+	351/730	168/352		ps
	S1->Y	++	405/727	219/383		ps
		−−	285/466	205/314		ps
		+−	287/441	175/285		ps
		−+	395/713	228/409		ps
	S1->YN	++	462/873	240/438		ps
		−−	265/423	200/303		ps
		+−	263/397	163/271		ps
		−+	447/857	247/461		ps
k_{fo}, k_{net}	rising Y,YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		
IEE			0.450	0.604		mA
FAN-IN	I0,I1, S1		1	1		load
FAN-OUT	Y,YN		18	18		loads
PW			1150	620		ps min
f_{max}			350	650		MHz
SIZE			2	2		L cells

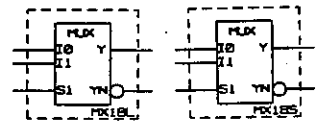
S1 MUST BE DRIVEN BY A MACRO

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

MX18 2:1 MUX; Y, YN

S1	I1	I0		Y	YN
0	X	0	I	0	1
0	X	1	I	1	0
1	0	X	I	0	1
1	1	X	I	1	0
X	0	0	I	0	1
X	0	1	I	UKN	UKN
X	1	0	I	UKN	UKN
X	1	1	I	1	0

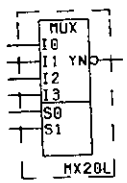
X = DON'T CARE
UKN = UNKNOWN

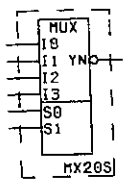


Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

MX20 4:1 MUX; YN

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	I0->YN	+−	107/173	82/134		ps
		−+	118/210	102/165		ps
	I1->YN	+−	107/174	82/135		ps
		−+	116/209	100/165		ps
	I2->YN	+−	107/177	82/139		ps
		−+	114/209	94/164		ps
	I3->YN	+−	107/178	82/140		ps
		−+	113/211	93/165		ps
	S0->YN	++	208/317	164/267		ps
		−−	133/233	101/180		ps
		+−	146/275	115/223		ps
		−+	162/274	130/214		ps
	S1->YN	++	247/411	197/351		ps
		−−	151/255	116/188		ps
		+−	193/394	151/316		ps
		−+	182/294	143/224		ps
k_{fo}, k_{net}	rising YN		1.95/6.05	1.50/4.65		ps/LU
	falling		3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		





Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

MX20 4:1 MUX; YN

		L	S	H	
IEE		0.776	1.12		mA
FAN-IN	Ii, S0, S1 i = 0, 1, 2, 3	1	1		load
FAN-OUT	YN	18	18		loads
PW		650	500		ps min
f_{max}		600	800		MHz
SIZE		2	2		L cells

S0, S1 - EACH MUST BE DRIVEN BY A MACRO.

S1	S0	I3	I2	I1	I0	I	YN
0	0	X	X	X	0	I	1
0	0	X	X	X	1	I	0
0	1	X	X	0	X	I	1
0	1	X	X	1	X	I	0
1	0	X	0	X	X	I	1
1	0	X	1	X	X	I	0
1	1	0	X	X	X	I	1
1	1	1	X	X	X	I	0
X	X	0	0	0	0	I	1
X	X	1	1	1	1	I	0
X	0	X	0	X	0	I	1
X	0	X	1	X	1	I	0
X	1	0	X	0	X	I	1
X	1	1	X	1	X	I	0
0	X	X	X	0	0	I	1
0	X	X	X	1	1	I	0
1	X	0	0	X	X	I	1
1	X	1	1	X	X	I	0

X = DON'T CARE

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

MX21 4:1 MUX; Y

			L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd}	I0->Y	++	152/265	128/208		ps
		−−	108/170	79/132		ps
	I1->Y	++	154/265	129/208		ps
		−−	108/168	79/130		ps
	I2->Y	++	156/265	135/208		ps
		−−	108/166	79/125		ps
	I3->Y	++	157/265	137/208		ps
		−−	107/165	79/124		ps
	S0->Y	++	216/330	171/285		ps
		−−	159/248	115/187		ps
		+−	173/307	130/239		ps
		−+	180/296	149/235		ps
	S1->Y	++	261/433	208/368		ps
		−−	162/270	123/199		ps
		+−	204/411	158/328		ps
		−+	198/317	156/242		ps
k_{fo}, k_{net} rising Y			1.95/6.05	1.50/4.65		ps/LU
falling			3.25/10.08	2.50/7.75		ps/LU
MIL4 ADJ. FACTOR:			1.09/1.00	1.09/1.00		

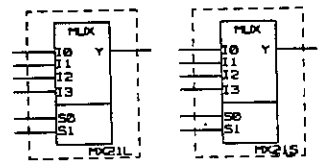
Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

MX21 4:1 MUX; Y

		L	S	H	
IEE		0.775	0.91		mA
FAN-IN	Ii, S0, S1 i = 0, 1, 2, 3	1	1		load
FAN-OUT	Y	18	18		loads
PW		650	500		ps min
f_{max}		600	800		MHz
SIZE		2	2		L cells

S1, S0 - EACH MUST BE DRIVEN BY A MACRO.

S1	S0	I3	I2	I1	I0	I	Y
0	0	X	X	X	0	I	0
0	0	X	X	X	1	I	1
0	1	X	X	0	X	I	0
0	1	X	X	1	X	I	1
1	0	X	0	X	X	I	0
1	0	X	1	X	X	I	1
1	1	0	X	X	X	I	0
1	1	1	X	X	X	I	1
X	X	0	0	0	0	I	0
X	X	1	1	1	1	I	1
X	0	X	0	X	0	I	0
X	0	X	1	X	1	I	1
X	1	0	X	0	X	I	0
X	1	1	X	1	X	I	1
0	X	X	X	0	0	I	0
0	X	X	X	1	1	I	1
1	X	0	0	X	X	I	0
1	X	1	1	X	X	I	1



X = DON'T CARE

Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

VB01 VBB GENERATOR FOR ECL 100K OUTPUT REFERENCE

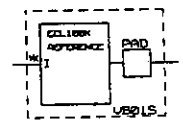
	L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} INPUT->PO		000/000		ps
k_{cap} rising PO		000/000		ps/pF
falling		000/000		ps/pF
MIL4 ADJ. FACTOR:		1.09/1.00		
IEE		3.57		mA
FAN-IN INPUT		0		load
FAN-OUT PO		0.5		load
PW		350		ps min
f_{max}		1.2		GHz
SIZE		1		I/O cell

INPUT MUST BE TIED TO GROUND.
CONSULT AMCC BEFORE USING THIS MACRO.

TEST REQUIREMENTS:

1 /THIS MACRO IS A COMPLETE REFERENCE GENERATOR BUILT IN AN I/O CELL. THIS GENERATOR CAN BE EITHER ECL100K BY DESIGN (DETERMINED BY MODE CELL TYPE), AND REQUIRES NO EXTERNAL TERMINATION./

PO = $\overline{\text{INPUT}}$



Minimum and maximum specifications account for temperature, voltage, and process variations over the MIL5 operating range

VB02 ON-CHIP VBB LEVEL FOR ECL OUTPUT REFERENCE

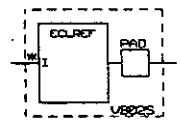
	L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} INPUT->PO		000/000		ps
k_{cap} rising PO		000/000		ps/pF
falling		000/000		ps/pF
MIL4 ADJ. FACTOR:		1.09/1.00		
IEE		10.7		mA
FAN-IN INPUT		0		load
FAN-OUT PO		50.0		uA
PW		350		ps min
f_{max}		1.2		GHz
SIZE		1		I/O cell

INPUT MUST BE TIED TO GROUND.
10K OR 100K DETERMINED BY MODE OF OPERATION.
CONSULT AMCC BEFORE USING THIS MACRO.
THE VB02 IS VERY SUSCEPTIBLE TO EXTERNAL NOISE AND LOADING EFFECTS. IT MUST BE ELECTRICALLY ISOLATED. A OPERATIONAL AMPLIFIER IS RECOMMENDED.

TEST REQUIREMENTS:

1 /THIS MACRO IS A WIRE THAT TAPS INTO AN INTERNAL VTA GENERATOR. THIS GENERATOR CAN BE EITHER ECL10K OR ECL100K BY DESIGN (DETERMINED BY MODE CELL TYPE), AND REQUIRES NO EXTERNAL TERMINATION./

PO = $\overline{\text{INPUT}}$



Chip Macros

The inclusion of the chip macro documents (to the software) the number of fixed power and ground pads that a particular array has for a given I/O mode. It also documents the internal pin count limit, cell type limits, ECL output limits, TTL output limits, SSO rules, allowed cell utilization, the default power supply or supplies, the worst-case current multipliers for COM and MIL product grades, overhead current, and other parameters as required by the current AMCC MacroMatrix software.

A chip macro must be used.

MacroMatrix software will not run without one.

If there is more than one, the first encountered will be used.

Follow directions in the AMCC EWS Schematic Rules for pin connections, and see the AMCCERC User's Guide for further information on the chip macros.

Follow directions in the MacroMatrix Installation and Operation Guide which provides information on assigning values to the chip macro parameters.

Ground and Terminate the input and output macro pins respectively.

Chip macros are not real macros in that they are not placed on the array. A name is not required. CHIP00 is a good name if you follow consistent structured design procedures and name all macros regardless of type.

Chip macros use no cells and draw no current.

Place the chip macro on page one of the schematics along with added power and ground and VBBxx macros. This is for human readability.

Assign values to the chip macro parameters. The software will use defaults and run anyway but the results may be invalid to the design.

Chip macro parameters:

product_name	AMCC assigned name	X	X	X	X
device_number	AMCC assigned number	X	X	X	X
product_grade	MIL or COM	X	X	X	X
power_supply	ECL supply only	X	X	X	X

The first three parameters are required for design submission. The AMCCERC program will use default values and continue but the resulting report cannot be submitted.

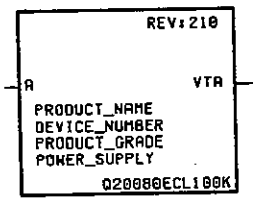
Allowed power_supply parameter values for the Q20000 Series:

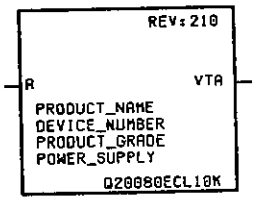
default	what appears on the chip macro graphic
STD4	-4.5V ECL VEE supply; ECL VCC = 0V
STD5	-5.2V ECL VEE supply; ECL VCC = 0V
5VREF	+5V ECL VCC supply; ECL VEE = 0V

For Single Supply Circuits: 100% ECL

Power supply = -5.2V; -4.5V or +5V

Q20010ECL10K	For 100% ECL 10K circuit on a Q20010
Q20010ECL100K	For 100% ECL 100K circuit on a Q20010
Q20025ECL10K	For 100% ECL 10K circuit on a Q20025
Q20025ECL100K	For 100% ECL 100K circuit on a Q20025
Q20045ECL10K	For 100% ECL 10K circuit on a Q20045
Q20045ECL100K	For 100% ECL 100K circuit on a Q20045
Q20080ECL10K	For 100% ECL 10K circuit on a Q20080
Q20080ECL100K	For 100% ECL 100K circuit on a Q20080
Q20120ECL10K	For 100% ECL 10K circuit on a Q20120
Q20120ECL100K	For 100% ECL 100K circuit on a Q20120

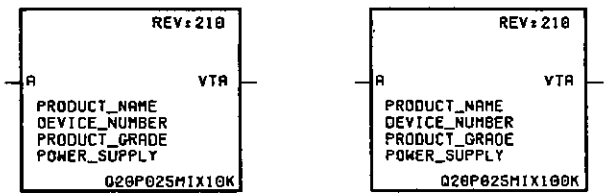




For Dual Supply Circuits: ECL/TTL Mix

Power supply = -5.2V; -4.5V or +5V

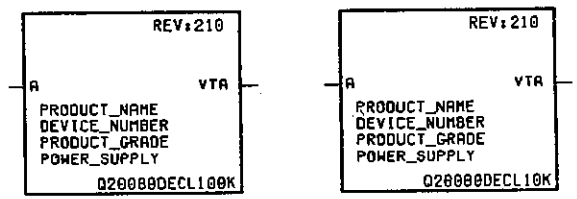
Q20010MIX10K	For ECL 10K /TTL circuit on a Q20010
Q20010MIX100K	For ECL 100K /TTL circuit on a Q20010
Q20P010MIX10K	For ECL 10K /TTL circuit on a Q20P010
Q20P010MIX100K	For ECL 100K /TTL circuit on a Q20P010
Q20025MIX10K	For ECL 10K /TTL circuit on a Q20025
Q20025MIX100K	For ECL 100K /TTL circuit on a Q20025
Q20P025MIX10K	For ECL 10K /TTL circuit on a Q20P025
Q20P025MIX100K	For ECL 100K /TTL circuit on a Q20P025
Q20045MIX10K	For ECL 10K /TTL circuit on a Q20045
Q20045MIX100K	For ECL 100K /TTL circuit on a Q20045
Q20080MIX10K	For ECL 10K /TTL circuit on a Q20080
Q20080MIX100K	For ECL 100K /TTL circuit on a Q20080
Q20120MIX10K	For ECL 10K /TTL circuit on a Q20120
Q20120MIX100K	For ECL 100K /TTL circuit on a Q20120



For Dual Supply Circuits: 100% ECL

Power supply = -5.2V or -4.5V and +5V

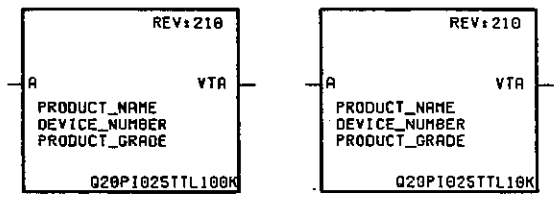
Q20010DECL10K	For 100% ECL 10K circuit on a Q20010
Q20010DECL100K	For 100% ECL 100K circuit on a Q20010
Q20025DECL10K	For 100% ECL 10K circuit on a Q20025
Q20025DECL100K	For 100% ECL 100K circuit on a Q20025
Q20045DECL10K	For 100% ECL 10K circuit on a Q20045
Q20045DECL100K	For 100% ECL 100K circuit on a Q20045
Q20080DECL10K	For 100% ECL 10K circuit on a Q20080
Q20080DECL100K	For 100% ECL 100K circuit on a Q20080
Q20120DECL10K	For 100% ECL 10K circuit on a Q20120
Q20120DECL100K	For 100% ECL 100K circuit on a Q20120



For Single supply circuits: ECL/TTL Mix

Power supply = +5V

Q20010TTL10K	For ECL 10K /TTL circuit on a Q20010
Q20010TTL100K	For ECL 100K /TTL circuit on a Q20010
Q20P010TTL10K	For ECL 10K /TTL circuit on a Q20P010
Q20P010TTL100K	For ECL 100K /TTL circuit on a Q20P010
Q20025TTL10K	For ECL 10K /TTL circuit on a Q20025
Q20025TTL100K	For ECL 100K /TTL circuit on a Q20025
Q20P025TTL10K	For ECL 10K /TTL circuit on a Q20P025
Q20P025TTL100K	For ECL 100K /TTL circuit on a Q20P025
Q20045TTL10K	For ECL 10K /TTL circuit on a Q20045
Q20045TTL100K	For ECL 100K /TTL circuit on a Q20045
Q20080TTL10K	For ECL 10K /TTL circuit on a Q20080
Q20080TTL100K	For ECL 100K /TTL circuit on a Q20080
Q20120TTL10K	For ECL 10K /TTL circuit on a Q20120
Q20120TTL100K	For ECL 100K /TTL circuit on a Q20120



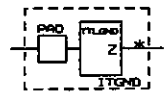
ADDED POWER AND GROUNDS

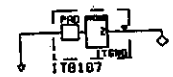
ITGND ADDED TTL GND PAD

REQUIRED WHEN AN ADDED TTL GROUND PAD IS NEEDED.
USES THE PAD PORTION OF THE I/O CELL.
USED TO OBTAIN A CORRECT POPULATION REPORT AND EXTERNAL PIN (PAD) COUNT BY THE AMCC MACROMATRIX ERC SOFTWARE.

- GROUND THE INPUT PIN WITH THE WIRE POINTING DOWN
- TERMINATE THE OUTPUT

NOTE: When placing an ITGND macro, the macro must be interspersed with the simultaneously switching outputs it supports. On the Q20000T array and any other array with packages that contain internal power-ground planes, an ITGND must be placed on a PAD that will allow it to be connected to the internal plane if it is at all possible. Placing it on a pad that must connect to a package pin requires a custom DUT board for test.



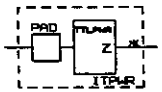


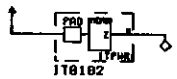
ITPWR **ADDED ECL V_{CC} (+5V) PAD**

REQUIRED WHEN AN ADDED TTL POWER PAD IS NEEDED.
USES THE PAD PORTION OF THE I/O CELL.
USED TO OBTAIN A CORRECT POPULATION REPORT AND EXTERNAL PIN (PAD) COUNT BY THE AMCC MACROMATRIX ERC SOFTWARE.

- GROUND THE INPUT PIN WITH THE WIRE POINTING UP
- TERMINATE THE OUTPUT

NOTE: When placing an ITPWR macro, the macro must be interspersed with the simultaneously switching outputs it supports. On the Q20000T array and any other array with packages that contain internal power-ground planes, an ITPWR must be placed on a PAD that will allow it to be connected to the internal plane if it is at all possible. Placing it on a pad that must connect to a package pin requires a custom DUT board for test.



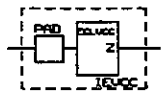


IEVCC **ADDED ECL VCC PAD**

REQUIRED WHEN AN ADDED ECL VCC PAD IS NEEDED.
USES THE PAD PORTION OF THE I/O CELL.
USED TO OBTAIN A CORRECT POPULATION REPORT AND EXTERNAL PIN (PAD) COUNT BY THE AMCC MACROMATRIX ERC SOFTWARE.

- GROUND THE INPUT PIN WITH THE WIRE POINTING DOWN FOR STANDARD-REFERENCE ECL; POINTING UP FOR +5V REF ECL.
- TERMINATE THE OUTPUT
- IEVCC is a GROUND pad in a STD-REF ECL circuit.
- IEVCC is a POWER pad in a +5V REF ECL circuit.

NOTE: When placing an IEVCC macro, the macro must be interspersed with the simultaneously switching outputs it supports. On the Q20000T array and any other array with packages that contain internal power-ground planes, an IEVCC must be placed on a PAD that will allow it to be connected to the internal plane if it is at all possible. Placing it on a pad that must connect to a package pin requires a custom DUT board for test.



Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

VB01 VBB GENERATOR FOR ECL 100K OUTPUT REFERENCE

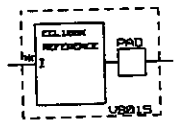
	L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} INPUT->PO		000/000		ps
k_{cap} rising PO		000/000		ps/pF
falling		000/000		ps/pF
COM4 ADJ. FACTOR:		1.05/1.03		
IEE		3.57		mA
FAN-IN INPUT		0		load
FAN-OUT PO		0.5		load
PW		350		ps min
f_{max}		1.2		GHz
SIZE		1		I/O cell

INPUT MUST BE TIED TO GROUND.
CONSULT AMCC BEFORE USING THIS MACRO.

TEST REQUIREMENTS:

1 /THIS MACRO IS A COMPLETE REFERENCE GENERATOR BUILT IN AN I/O CELL. THIS GENERATOR CAN BE EITHER ECL100K BY DESIGN (DETERMINED BY MODE CELL TYPE), AND REQUIRES NO EXTERNAL TERMINATION./

PO = $\overline{\text{INPUT}}$



Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

VB02 ON-CHIP VBB LEVEL FOR ECL OUTPUT REFERENCE

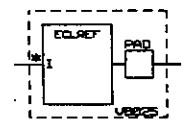
	L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{pd} INPUT->PO		000/000		ps
k_{cap} rising PO		000/000		ps/pF
falling		000/000		ps/pF
COM4 ADJ. FACTOR:		1.05/1.03		
IEE		10.7		mA
FAN-IN INPUT		0		load
FAN-OUT PO		50.0		uA
PW		350		ps min
f_{max}		1.2		GHz
SIZE		1		I/O cell

INPUT MUST BE TIED TO GROUND.
10K OR 100K DETERMINED BY MODE OF OPERATION.
CONSULT AMCC BEFORE USING THIS MACRO.
THE VB02 IS VERY SUSCEPTIBLE TO EXTERNAL NOISE AND LOADING EFFECTS. IT MUST BE ELECTRICALLY ISOLATED. A OPERATIONAL AMPLIFIER IS RECOMMENDED.

TEST REQUIREMENTS:

1 /THIS MACRO IS A WIRE THAT TAPS INTO AN INTERNAL VTA GENERATOR. THIS GENERATOR CAN BE EITHER ECL10K OR ECL100K BY DESIGN (DETERMINED BY MODE CELL TYPE), AND REQUIRES NO EXTERNAL TERMINATION./

PO = $\overline{\text{INPUT}}$



Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

CRU04 CLOCK RECOVERY MACROS

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
MAXIMUM SKEW:					
SERCLKOP,->SERDATOP					
SERCLKON	(+ –) +			125/200	ps
	(+ –) –			100/175	ps
LKLPCKOP->LKLPDTOP (ZERO CROSS TO ZERO CROSS)				100/225	ps
OPERATING FREQUENCY:				1000 ± 12%	MHz
k_{fo}, k_{net}	rising	LOCKDETA, FRKCNT		1.80/3.90	ps/LU
	falling			3.00/6.50	ps/LU
k_{fo}, k_{net}	rising	SERDATOP,SERCLKOP, REFCKOUT,TESTEN, SERCLKON		1.44/3.12	ps/LU
	falling			2.40/5.20	ps/LU
k_{cap}	rising	LKLPCKOP,LKLPCKON, LKLPDTOP,LKLPDTON		21/46	ps/pF
	falling			21/46	ps/pF
k_{cap}	rising	LOCKDET		15/34	ps/pF
	falling			40/88	ps/pF
COM4 ADJ. FACTOR:				1.05/1.03	

TSTRST, BYTCLKIP, DIVNCNT0, DIVNCNT1, DIVNCNT2, LOCLPEN, LCKDETOV, ACQCTL0, ACQCTL1, ACQCONT, RST - EACH MUST BE DRIVEN BY A MACRO

AMCC Q20000 SERIES - CRUxx COM5 (210)

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

CRU04 CLOCK RECOVERY MACROS

	L	S	H	
ARRAY: Q20P025				
CHIPMACRO: Q20P025TTL10K, Q20P025TTL100K				
ICC			164	mA
FAN-IN BYTCLKIP,DIVNCNT1, DIVNCNT2,ACQCONT, LCKDETOV,ACQCTL0, ACQCTL1,SERDATIP, SERDATIN,LPDATIP, LPDATIN,REFCKINP, REFCKINN,TSTCLKEN			1	load
TSTRST,LOCLPEN			2	loads
DIVNCNT0,RST			3	loads
FAN-OUT TESTEN			16	loads
LOCKDETA,REFCKOUT, SERCLKOP,SERCLKON			17	loads
FRKCNT,SERDATOP			18	loads
SIZE			1	G cell

The CRU04 recovers clock and data from an incoming serial bit stream. The CRU will output synchronous clock and data signals to the array and to the link loopback I/O pins. The clock and data signals can be used to clock a serial to parallel register in the array and used for framing functions. The CRU also checks the serial data inputs for minimum transition density and maximum run length. If either of these tests fail, the phase locked loop cannot be guaranteed to accurately recover the clock from the serial data and an out of lock condition is indicated via the lockdetect I/O pin and the lockdetect array pad. The CRU can be programmed to recover the clock from the serial data inputs operating at the VCO frequency divided by 1, 2, 4 or 8 as programmed by the DIVNCNTi pads from the array.

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

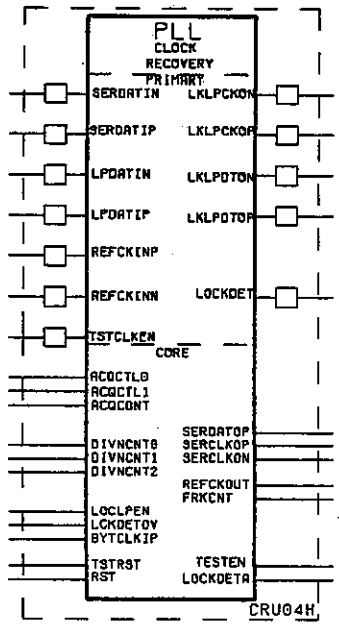
CRU04 CLOCK RECOVERY MACROS

The CRU04 model will initiate with the VCO set to the center frequency. If serial data is present and passes the transition density and run length checks, the VCO will measure the width of the first 25 pulses on the serial data. It will then phase and frequency align the serial clock to the serial data. In the actual circuit this alignment may take up to 2.5µsec.

The CRU requires an external clock reference to reduce the initial acquisition time and to provide stability in the absence of serial data. When there is no signal on the selected serial data inputs, the VCO frequency will be a multiplied value of the reference clock input. A typical frequency multiplication factor is 20 but can go as high as 40.

A byte clock counter in the array should take the serial clock output (as programmed by the DIVNCNTi pins) and divide it down to match the reference clock input.

If at any time during the simulation, the serial data inputs are inactive and the byte clock and reference clock frequencies drift by more than 3%, the VCO will be phase and frequency shifted to bring the byte clock within the 3% tolerance. In the actual circuit this alignment will initially take up to 2.5µsec. and then be performed continously.



CLOCK RECOVERY MACRO CRU04

PIN DESCRIPTIONS FOR CLOCK RECOVERY MACRO

PIN NAME	PIN COUNT	I/O	POLARITY
REFCKINP	1	diff ECL in	H
REFCKINN	1	diff ECL in	L
DIVNCNT0	1	from array	H
DIVNCNT1	1	from array	H
DIVNCNT2	1	from array	H
TSTCLKEN	1	TTL in	H
LKLPCKOP	1	diff ECL out	H
LKLPCKON	1	diff ECL out	L
LKLPDTOP	1	diff ECL out	H
LKLPDTON	1	diff ECL out	L
LOCLPEN	1	from array	L
ACQCONT	1	from array	H
SERDATOP	1	to array	H
SERDATIP	1	diff ECL in	H
SERDATIN	1	diff ECL in	L
LPDATIP	1	diff ECL in	H
LPDATIN	1	diff ECL in	L
SERCLKOP	1	to array	H
SERCLKON	1	to array	L
LOCKDET	1	TTL out	H
BYTCLKIP	1	from array	H
TESTEN	1	to array	H
LCKDETOV	1	from array	H
LOCKDETA	1	to array	H
REFCKOUT	1	to array	H
RST	1	from array	H
TSTRST	1	from array	H
ACQCTL0	1	from array	H
ACQCTL1	1	from array	H
FRKCNT	1	to array	H

REFCKINP/N This clock should be equal in frequency to the byte clock (BYTCLKIP) input from the array. The byte clock will frequency lock to the reference clock when the acquisition control line is high, when RST is active, or when there its no serial data present. This pin can also be used to bypass the internal VCO when enabled by the TSTCLKEN pin. The reference clock inputs can then be used for functional test or VCO bypass. This path is capable of operating at 625 MHz.

DIVNCNT0,1,2 Control lines from the array which determine the value of the divide by N counter. Possible values are as follows:

DIVNCNT0	DIVNCNT1	DIVNCNT2	VALUE OF N
1	x	x	1
0	0	0	2
0	0	1	4
0	1	0	8

TSTCLKEN Enables the reference clock through the VCO clock path. This pin is intended to be used for functional test and bypass mode.

LKLPCKOP/N Link Loop Clock Output: This signal is a buffered version of the serial clock signal.

LKLPDTOP/N Link Loop Data Output: This signal is a buffered version of the serial data signal.

LOCLPEN Local Loopback Enable: Enables the loopback data inputs to be used as the source of data for clock recovery.

ACQCONT Acquisition Control: This signal, when high, will force the lock detect signal to the unlocked (L) state and force the byte clock output and the divide by N output to be in phase with the reference clock input. When low, the PLL will phase lock to the incoming serial data stream if data is present.

SERDATOP Serial Data Out: RECLocked serial data which is in phase with the output of the divide by N counter.

SERDATIP/N Serial Data Inputs: Serial data which is retimed by the phase detector so that it is in phase with the output of the divide by N counter and then output on the serial data outputs.

LPDATIP/N Loopback Data In: This signal is enabled through the serial data path using the loopback enable pin. When enabled, this input will be retimed by the phase detector so that it is in phase with the output of the divide by N counter and output on the serial data outputs just like the serial data inputs.

SERCLKOP/N Serial Clock Out: Output of the divide by N counter. This clock is phase locked to the serial data and can be used to clock a serial to parallel shift register.

LOCKDET Lock Detect: This pin will be low until 2500 edges are seen at the serial data input. The overide pin will cause the lock detect pin to go high regardless of the serial data input edge count.

BYTCLKIP Byte Clock Input: This clock input should be equal in frequency to the reference clock input. It is used by the PLL to acquire frequency lock to the reference clock in the absence of serial data.

TESTEN Test Enable: Test clock enable pin routed to the array.

LCKDETOV Lock Detect Overide: This signal will force the PLL to attempt to acquire phase and frequency lock on the serial data inputs regardless of the state of the data, i.e., the PLL will attempt to acquire lock even if no data is present.

LOCKDETA Lock detect to array: This pin functions identically to LOCKDET except it is an array output instead of an I/O pin.

REFCKOUT Reference clock out to array: This pin is a buffered version of the reference clock input.

RST Reset: This pin will reset the state machine in the PLL macro. This causes the PLL to acquire frequency lock to the reference clock and lock detect to go inactive. (See power up initialization procedure.)

TSTRST Test Reset: This pin will reset the divide by 2, 4 and 8 counters. If this pin is not used the divide by 2, 4 and 8 counters will free run. (See power up initialization procedure.)

ACQCTL0/1 Acquisition Counter Control: These bits control the acquisition time of the phase locked loop. The acquisition counter value should be selected based on the coding scheme used by the serial data. Recommended selections are shown in the table below.

ACQCTL0	ACQCTL1	COUNTER VALUE (Divn clock cycles)
0	0	500
0	1	1000
1	0	2000
1	1	4000

FRKCNT Four thousand count output: This is the output of a four thousand serial clock cycle ripple counter. It can be used as watchdog timer. It is only active when lock detect is high.

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

CRU05 CLOCK RECOVERY MACROS

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
MAXIMUM SKEW:					
SERCLKOP,->SERDATOP SERCLKON	(+ –) +			125/200	ps
	(+ –) –			100/175	ps
LKLPCKOP->LKLPDTOP (ZERO CROSS TO ZERO CROSS)				100/225	ps
OPERATING FREQUENCY:				1000 ± 12%	MHz
k_{fo}, k_{net}	rising	LOCKDETA, FRKCNT		1.80/3.90	ps/LU
	falling			3.00/6.50	ps/LU
k_{fo}, k_{net}	rising	SERDATOP,SERCLKOP, REFCKOUT,TESTEN, SERCLKON		1.44/3.12	ps/LU
	falling			2.40/5.20	ps/LU
k_{cap}	rising	LKLPCKOP,LKLPCKON, LKLPDTOP,LKLPDTON		21/46	ps/pF
	falling			21/46	ps/pF
k_{cap}	rising	LOCKDET		33/72	ps/pF
	falling			33/72	ps/pF
COM4 ADJ. FACTOR:				1.05/1.03	

TSTRST, BYTCLKIP, DIVNCNT0, DIVNCNT1, DIVNCNT2, LOCLPEN, LCKDETOV, ACQCTL0, ACQCTL1, ACQCONT, RST - EACH MUST BE DRIVEN BY A MACRO

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

CRU05 CLOCK RECOVERY MACROS

	L	S	H	
ARRAY:				
Q20P025				
CHIPMACRO:				
Q20P025MIX10K,				
Q20P025MIX100K				
ICC			4	mA
IEE			160	mA
FAN-IN BYTCLKIP,DIVNCNT1, DIVNCNT2,ACQCONT, LCKDETOV,ACQCTL0, ACQCTL1,SERDATIP, SERDATIN,LPDATIP, LPDATIN,REFCKINP, REFCKINN,TSTCLKEN			1	load
TSTRST,LOCLPEN			2	loads
DIVNCNT0,RST			3	loads
FAN-OUT TESTEN			16	loads
LOCKDETA,REFCKOUT,			17	loads
SERCLKOP,SERCLKON FRKCNT,SERDATOP			18	loads
SIZE			1	G cell

The CRU05 recovers clock and data from an incoming serial bit stream. The CRU will output synchronous clock and data signals to the array and to the link loopback I/O pins. The clock and data signals can be used to clock a serial to parallel register in the array and used for framing functions. The CRU also checks the serial data inputs for minimum transition density and maximum run length. If either of these tests fail, the phase locked loop cannot be guaranteed to accurately recover the clock from the serial data and an out of lock condition is indicated via the lockdetect I/O pin and the lockdetect array pad. The CRU can be programmed to recover the clock from the serial data inputs operating at the VCO frequency divided by 1, 2, 4 or 8 as programmed by the DIVNCNTi pads from the array.

AMCC Q20000 SERIES - CRUxx COM5 (210)

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

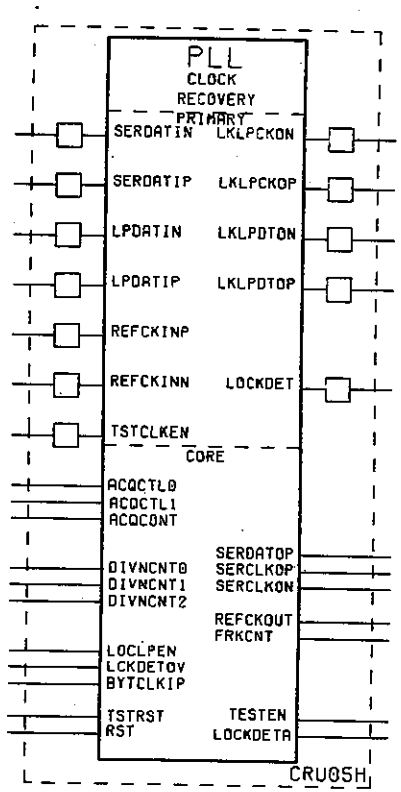
CRU05 CLOCK RECOVERY MACROS

The CRU05 model will initiate with the VCO set to the center frequency. If serial data is present and passes the transition density and run length checks, the VCO will measure the width of the first 25 pulses on the serial data. It will then phase and frequency align the serial clock to the serial data. In the actual circuit this alignment may take up to 2.5µsec.

The CRU requires an external clock reference to reduce the initial acquisition time and to provide stability in the absence of serial data. When there is no signal on the selected serial data inputs, the VCO frequency will be a multiplied value of the reference clock input. A typical frequency multiplication factor is 20 but can go as high as 40.

A byte clock counter in the array should take the serial clock output (as programmed by the DIVNCNTi pins) and divide it down to match the reference clock input.

If at any time during the simulation, the serial data inputs are inactive and the byte clock and reference clock frequencies drift by more than 3%, the VCO will be phase and frequency shifted to bring the byte clock within the 3% tolerance. In the actual circuit this alignment will initially take up to 2.5µsec. and then be performed continously.



CLOCK RECOVERY MACRO CRU05

PIN DESCRIPTIONS FOR CLOCK RECOVERY MACRO

PIN NAME	PIN COUNT	I/O	POLARITY
REFCKINP	1	diff ECL in	H
REFCKINN	1	diff ECL in	L
DIVNCNT0	1	from array	H
DIVNCNT1	1	from array	H
DIVNCNT2	1	from array	H
TSTCLKEN	1	TTL in	H
LKLPCKOP	1	diff ECL out	H
LKLPCKON	1	diff ECL out	L
LKLPDTOP	1	diff ECL out	H
LKLPDTON	1	diff ECL out	L
LOCLPEN	1	from array	L
ACQCONT	1	from array	H
SERDATOP	1	to array	H
SERDATIP	1	diff ECL in	H
SERDATIN	1	diff ECL in	L
LPDATIP	1	diff ECL in	H
LPDATIN	1	diff ECL in	L
SERCLKOP	1	to array	H
SERCLKON	1	to array	L
LOCKDET	1	TTL out	H
BYTCLKIP	1	from array	H
TESTEN	1	to array	H
LCKDETOV	1	from array	H
LOCKDETA	1	to array	H
REFCKOUT	1	to array	H
RST	1	from array	H
TSTRST	1	from array	H
ACQCTL0	1	from array	H
ACQCTL1	1	from array	H
FRKCNT	1	to array	H

REFCKINP/N This clock should be equal in frequency to the byte clock (BYTCLKIP) input from the array. The byte clock will frequency lock to the reference clock when the acquisition control line is high, when RST is active, or when there its no serial data present. This pin can also be used to bypass the internal VCO when enabled by the TSTCLKEN pin. The reference clock inputs can then be used for functional test or VCO bypass. This path is capable of operating at 625 MHz.

DIVNCNT0,1,2 Control lines from the array which determine the value of the divide by N counter. Possible values are as follows:

DIVNCNT0	DIVNCNT1	DIVNCNT2	VALUE OF N
1	x	x	1
0	0	0	2
0	0	1	4
0	1	0	8

TSTCLKEN Enables the reference clock through the VCO clock path. This pin is intended to be used for functional test and bypass mode.

LKLPCKOP/N Link Loop Clock Output: This signal is a buffered version of the serial clock signal.

LKLPDTOP/N Link Loop Data Output: This signal is a buffered version of the serial data signal.

LOCLPEN Local Loopback Enable: Enables the loopback data inputs to be used as the source of data for clock recovery.

ACQCONT Acquisition Control: This signal, when high, will force the lock detect signal to the unlocked (L) state and force the byte clock output and the divide by N output to be in phase with the reference clock input. When low, the PLL will phase lock to the incoming serial data stream if data is present.

SERDATOP Serial Data Out: RECLocked serial data which is in phase with the output of the divide by N counter.

SERDATIP/N Serial Data Inputs: Serial data which is retimed by the phase detector so that it is in phase with the output of the divide by N counter and then output on the serial data outputs.

LPDATIP/N Loopback Data In: This signal is enabled through the serial data path using the loopback enable pin. When enabled, this input will be retimed by the phase detector so that it is in phase with the output of the divide by N counter and output on the serial data outputs just like the serial data inputs.

SERCLKOP/N Serial Clock Out: Output of the divide by N counter. This clock is phase locked to the serial data and can be used to clock a serial to parallel shift register.

LOCKDET Lock Detect: This pin will be low until 2500 edges are seen at the serial data input. The overide pin will cause the lock detect pin to go high regardless of the serial data input edge count.

BYTCLKIP Byte Clock Input: This clock input should be equal in frequency to the reference clock input. It is used by the PLL to acquire frequency lock to the reference clock in the absence of serial data.

TESTEN Test Enable: Test clock enable pin routed to the array.

LCKDETOV Lock Detect Overide: This signal will force the PLL to attempt to acquire phase and frequency lock on the serial data inputs regardless of the state of the data, i.e., the PLL will attempt to acquire lock even if no data is present.

LOCKDETA Lock detect to array: This pin functions identically to LOCKDET except it is an array output instead of an I/O pin.

REFCKOUT Reference clock out to array: This pin is a buffered version of the reference clock input.

RST Reset: This pin will reset the state machine in the PLL macro. This causes the PLL to acquire frequency lock to the reference clock and lock detect to go inactive. (See power up initialization procedure.)

TSTRST Test Reset: This pin will reset the divide by 2, 4 and 8 counters. If this pin is not used the divide by 2, 4 and 8 counters will free run. (See power up initialization procedure.)

ACQCTL0/1 Acquisition Counter Control: These bits control the acquisition time of the phase locked loop. The acquisition counter value should be selected based on the coding scheme used by the serial data. Recommended selections are shown in the table below.

ACQCTL0	ACQCTL1	COUNTER VALUE (Divn clock cycles)
0	0	500
0	1	1000
1	0	2000
1	1	4000

FRKCNT Four thousand count output: This is the output of a four thousand serial clock cycle ripple counter. It can be used as watchdog timer. It is only active when lock detect is high.

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

CRU12 CLOCK RECOVERY MACROS

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
MAXIMUM SKEW:					
SERCLKOP->SERDATOP					
	++			125/200	ps
	+-			100/175	ps
LKLPCKOP->LKLPDTOP (ZERO CROSS TO ZERO CROSS)				100/225	ps
OPERATING FREQUENCY:				600 ± 12%	MHz
k_{fo}, k_{net}	rising	LOCKDETA, FRKCNT		1.80/3.90	ps/LU
	falling			3.00/6.50	ps/LU
k_{fo}, k_{net}	rising	SERDATOP,SERCLKOP REFCKOUT,TESTEN		1.44/3.12	ps/LU
	falling			2.40/5.20	ps/LU
k_{cap}	rising	LKLPCKOP,LKLPCKON, LKLPDTOP,LKLPDTON		21/46	ps/pF
	falling			21/46	ps/pF
k_{cap}	rising	LOCKDET		33/72	ps/pF
	falling			33/72	ps/pF
COM4 ADJ. FACTOR:				1.05/1.03	

TSTRST, BYTCLKIP, DIVNCNT0, DIVNCNT1, DIVNCNT2, LOCLPEN, LCKDETOV, ACQCTL0, ACQCTL1, ACQCONT, RST - EACH MUST BE DRIVEN BY A MACRO.

AMCC Q20000 SERIES - CRUxx COM5 (210)

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

CRU12 CLOCK RECOVERY MACROS

	L	S	H	
ARRAY: Q20P010				
CHIPMACRO: Q20P010MIX10K, Q20P010MIX100K				
ICC			4	mA
IEE			160	mA
FAN-IN DIVNCNT1,DIVNCNT2, ACQCONT,LCKDETOV, ACQCTL0,ACQCTL1 SERDATIP,SERDATIN, LPDATIP,LPDATIN, REFCKINP,REFCKINN			1	load
BYTCLKIP,LOCLPEN			2	load
TSTCLKEN,DIVNCNT0,RST			3	loads
TSTRST			4	loads
FAN-OUT TESTEN,REFCKOUT			16	loads
LOCKDETA			17	loads
FRKCNT,SERDATOP,SERCLKOP			18	loads
SIZE			1	G cell

The CRU12 recovers clock and data from an incoming serial bit stream. The CRU will output synchronous clock and data signals to the array and to the link loopback I/O pins. The clock and data signals can be used to clock a serial to parallel register in the array and used for framing functions. The CRU also checks the serial data inputs for minimum transition density and maximum run length. If either of these tests fail, the phase locked loop cannot be guaranteed to accurately recover the clock from the serial data and an out of lock condition is indicated via the lockdetect I/O pin and the lockdetect array pad. The CRU can be programmed to recover the clock from the serial data inputs operating at the VCO frequency divided by 1, 2, 4 or 8 as programmed by the DIVNCNTi pads from the array.

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

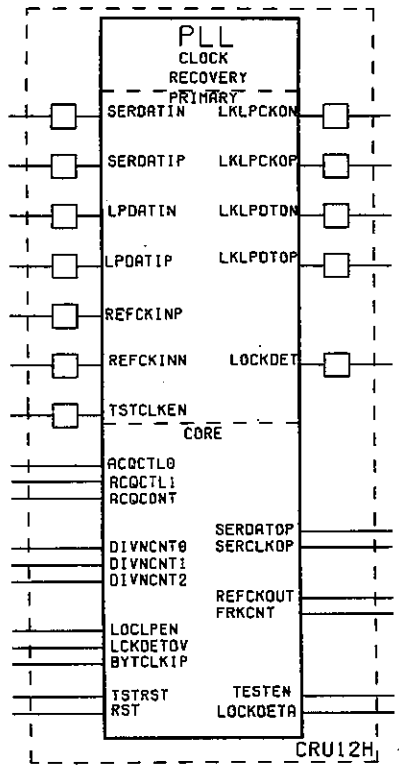
CRU12 CLOCK RECOVERY MACROS

The CRU12 model will initiate with the VCO set to the center frequency. If serial data is present and passes the transition density and run length checks, the VCO will measure the width of the first 25 pulses on the serial data. It will then phase and frequency align the serial clock to the serial data. In the actual circuit this alignment may take up to 2.5µsec.

The CRU requires an external clock reference to reduce the initial acquisition time and to provide stability in the absence of serial data. When there is no signal on the selected serial data inputs, the VCO frequency will be a multiplied value of the reference clock input. A typical frequency multiplication factor is 20 but can go as high as 40.

A byte clock counter in the array should take the serial clock output (as programmed by the DIVNCNTi pins) and divide it down to match the reference clock input.

If at any time during the simulation, the serial data inputs are inactive and the byte clock and reference clock frequencies drift by more than 3%, the VCO will be phase and frequency shifted to bring the byte clock within the 3% tolerance. In the actual circuit this alignment will initially take up to 2.5µsec. and then be performed continously.



CLOCK RECOVERY MACRO CRU12

PIN DESCRIPTIONS FOR CLOCK RECOVERY MACRO

PIN NAME	PIN COUNT	I/O	POLARITY
REFCKINP	1	diff ECL in	H
REFCKINN	1	diff ECL in	L
DIVNCNT0	1	from array	H
DIVNCNT1	1	from array	H
DIVNCNT2	1	from array	H
TSTCLKEN	1	TTL in	H
LKLPCKOP	1	diff ECL out	H
LKLPCKON	1	diff ECL out	L
LKLPDTOP	1	diff ECL out	H
LKLPDTON	1	diff ECL out	L
LOCLPEN	1	from array	L
ACQCONT	1	from array	H
SERDATOP	1	to array	H
SERDATIP	1	diff ECL in	H
SERDATIN	1	diff ECL in	L
LPDATIP	1	diff ECL in	H
LPDATIN	1	diff ECL in	L
SERCLKOP	1	to array	H
LOCKDET	1	TTL out	H
BYTCLKIP	1	from array	H
TESTEN	1	to array	H
LCKDETOV	1	from array	H
LOCKDETA	1	to array	H
REFCKOUT	1	to array	H
RST	1	from array	H
TSTRST	1	from array	H
ACQCTL0	1	from array	H
ACQCTL1	1	from array	H
FRKCNT	1	to array	H

REFCKINP/N This clock should be equal in frequency to the byte clock (BYTCLKIP) input from the array. The byte clock will frequency lock to the reference clock when the acquisition control line is high, when RST is active, or when there its no serial data present. This pin can also be used to bypass the internal VCO when enabled by the TSTCLKEN pin. The reference clock inputs can then be used for functional test or VCO bypass. This path is capable of operating at 625 MHz.

DIVNCNT0,1,2 Control lines from the array which determine the value of the divide by N counter. Possible values are as follows:

DIVNCNT0	DIVNCNT1	DIVNCNT2	VALUE OF N
1	x	x	1
0	0	0	2
0	0	1	4
0	1	0	8

TSTCLKEN Enables the reference clock through the VCO clock path. This pin is intended to be used for functional test and bypass mode.

LKLPCKOP/N Link Loop Clock Output: This signal is a buffered version of the serial clock signal.

LKLPDTOP/N Link Loop Data Output: This signal is a buffered version of the serial data signal.

LOCLPEN Local Loopback Enable: Enables the loopback data inputs to be used as the source of data for clock recovery.

ACQCONT Acquisition Control: This signal, when high, will force the lock detect signal to the unlocked (L) state and force the byte clock output and the divide by N output to be in phase with the reference clock input. When low, the PLL will phase lock to the incoming serial data stream if data is present.

SERDATOP Serial Data Out: RECLocked serial data which is in phase with the output of the divide by N counter.

SERDATIP/N Serial Data Inputs: Serial data which is retimed by the phase detector so that it is in phase with the output of the divide by N counter and then output on the serial data outputs.

LPDATIP/N Loopback Data In: This signal is enabled through the serial data path using the loopback enable pin. When enabled, this input will be retimed by the phase detector so that it is in phase with the output of the divide by N counter and output on the serial data outputs just like the serial data inputs.

SERCLKOP Serial Clock Out: Output of the divide by N counter. This clock is phase locked to the serial data and can be used to clock a serial to parallel shift register.

LOCKDET Lock Detect: This pin will be low until 2500 edges are seen at the serial data input. The overide pin will cause the lock detect pin to go high regardless of the serial data input edge count.

BYTCLKIP Byte Clock Input: This clock input should be equal in frequency to the reference clock input. It is used by the PLL to acquire frequency lock to the reference clock in the absence of serial data.

TESTEN Test Enable: Test clock enable pin routed to the array.

LCKDETOV Lock Detect Overide: This signal will force the PLL to attempt to acquire phase and frequency lock on the serial data inputs regardless of the state of the data, i.e., the PLL will attempt to acquire lock even if no data is present.

LOCKDETA Lock detect to array: This pin functions identically to LOCKDET except it is an array output instead of an I/O pin.

REFCKOUT Reference clock out to array: This pin is a buffered version of the reference clock input.

RST Reset: This pin will reset the state machine in the PLL macro. This causes the PLL to acquire frequency lock to the reference clock and lock detect to go inactive. (See power up initialization procedure.)

TSTRST Test Reset: This pin will reset the divide by 2, 4 and 8 counters. If this pin is not used the divide by 2, 4 and 8 counters will free run. (See power up initialization procedure.)

ACQCTL0/1 Acquisition Counter Control: These bits control the acquisition time of the phase locked loop. The acquisition counter value should be selected based on the coding scheme used by the serial data. Recommended selections are shown in the table below.

ACQCTL0	ACQCTL1	COUNTER VALUE (Divn clock cycles)
0	0	500
0	1	1000
1	0	2000
1	1	4000

FRKCNT Four thousand count output: This is the output of a four thousand serial clock cycle ripple counter. It can be used as watchdog timer. It is only active when lock detect is high.

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

CSU05 CLOCK SYNTHESIS MACROS

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{su}	(SERDATIP, SERDATIN) *			60	ps
T_h	(SERDATIP, SERDATIN) *			180	ps
	* WITH RESPECT TO SERCLKOP				
OPERATING FREQUENCY:				1000 ± 12%	MHz
k_{fo}, k_{net}	rising LOCKDETA, REFCKOUT			1.80/3.90	ps/LU
	falling			3.00/6.50	ps/LU
k_{fo},k_{net}	rising TESTEN,SERCLKOP, SERCLKON			1.44/3.12	ps/LU
	falling			2.40/5.20	ps/LU
k_{cap}	rising SERDATOP,SERDATON, LPDATOP,LPDATON			21/46	ps/pF
	falling			21/46	ps/pF
k_{cap}	rising LOCKDET			33/72	ps/pF
	falling			33/72	ps/pF
COM4 ADJ. FACTOR:				1.05/1.03	

DIVNCNT0, DIVNCNT1, DIVNCNT2, SERDATIP, SERDATIN, BYTCLKIP, BYTCLKIN, TSTRST, SERDATEN, LNKLPEN, LOCLPEN, VCOOEN - EACH MUST BE DRIVEN BY A MACRO.

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

CSU05 CLOCK SYNTHESIS MACROS

	L	S	H	
ARRAY: Q20P025				
CHIPMACRO: Q20P025MIX10K, Q20P025MIX100K				
ICC			4	mA
IEE			159	mA
FAN-IN DIVNCNT1,DIVNCNT2 TSTRST,BYTCLKIP, REFCKINP,REFCKINN, TSTCLKEN,LKLPDTIP, LKLPDTIN,LKLPCKIP, LKLPCKIN BYTCLKIN,SERDATIN, SERDATIP			1	load
DIVNCNT0,LNKLPEN, LOCLPEN,SERDATEN, VCOOEN			2	loads
FAN-OUT TESTEN			16	loads
LOCKDETA,SERCLKOP, SERCLKON			17	loads
REFCKOUT			18	loads
SIZE			1	G cell

CLOCK SYNTHESIS MACRO DESCRIPTION:

The CSU05 will align the phase and frequency of the byte clock (supplied from the array) and the reference clock (supplied from the external oscillator). The VCO frequency will power up at the center frequency and then phase and frequency lock the byte clock to the reference clock.

AMCC Q20000 SERIES - CSUxx COM5 (210)

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

CSU05 CLOCK SYNTHESIS MACROS

The final VCO frequency will be a multiplied value of the reference clock input. A typical frequency multiplication factor is 20 but can go as high as 64. A byte clock counter in the array should take the serial clock output (as programmedby the DIVNCNTi pins) and divide it down to match the reference clock input.

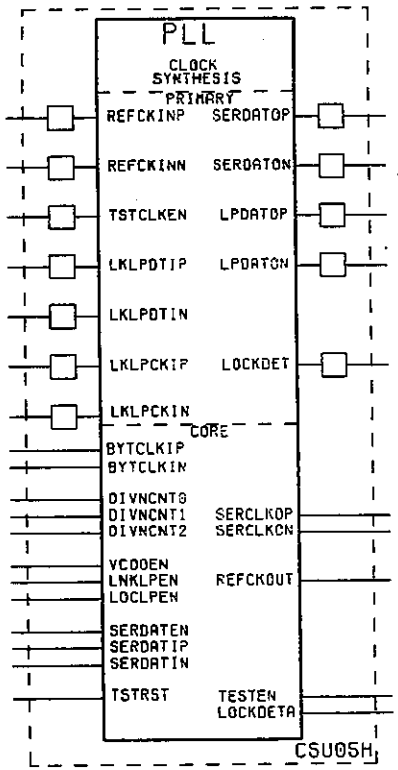
As an example: if a 50MHz reference clock is used and a 500 MHz serial clock is selected, the byte clock counter should divide the 500 MHz serial clock by 10 and drive the byte clock differential inputs with the output of the counter.

The VCO will wait until the byte clock input has stabilized by detecting two consecutive clock cycles with identical periods and then adjust the phase of the VCO to phase align the byte clock with the reference clock. In the actual circuit this alignment may take up to 2.5µsec.

If at any time during the simulation, the byte clock and reference clock frequencies drift by more than 3% the VCO will be phase and frequency shifted to bring the byte clock within the 3% tolerance. In the actual circuit this alignment will be performed continously.

The VCO will be allowed to frequency adjust over a ± 12% range from the center frequency.

The required set up and hold times for the serial clock output to serial data input are shown in the timing table. All other propagation delays are simulated using nominal delay values.



CLOCK SYNTHESIS MACRO CSU05

PIN DESCRIPTIONS FOR FREQUENCY SYNTHESIS MACRO

PIN NAME	PIN COUNT	I/O	POLARITY
REFCKINP	1	diff ECL in	H
REFCKINN	1	diff ECL in	L
DIVNCNT0	1	from array	H
DIVNCNT1	1	from array	H
DIVNCNT2	1	from array	H
TSTCLKEN	1	TTL in	H
LKLPCKIP	1	diff ECL in	H
LKLPCKIN	1	diff ECL in	L
LKLPDTIP	1	diff ECL in	H
LKLPDTIN	1	diff ECL in	L
LNKLPEN	1	from array	L
LOCLPEN	1	from array	L
SERDATEN	1	from array	L
SERDATOP	1	diff ECL out	H
SERDATON	1	diff ECL out	L
SERDATIP	1	from array	H
SERDATIN	1	from array	L
LPDATOP	1	diff ECL out	H
LPDATON	1	diff ECL out	L
SERCLKOP	1	to array	H
SERCLKON	1	to array	L
LOCKDET	1	TTL out	H
BYTCLKIP	1	from array	H
BYTCLKIN	1	from array	L
TESTEN	1	to array	H
LOCKDETA	1	to array	H
REFCKOUT	1	to array	H
TSTRST	1	from array	H
VCOOEN	1	from array	L

REFCKINP/N This clock should be equal in frequency to the byte clock (BYTCLKIP/N) input from the array. The clock synthesis macro will frequency and phase lock the byte clock to the reference clock. This pin can also be used to bypass the internal VCO when enabled by the TSTCLKEN pin. The reference clock inputs can then be used for functional test or VCO bypass. This path is capable of operating at 1.2GHz.

DIVNCNT0,1,2 Control lines from the array which determine the value of the divide by N counter. Possible values are as follows:

DIVNCNT0	DIVNCNT1	DIVNCNT2	VALUE OF N
1	x	x	1
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16

TSTCLKEN Enables the reference clock through the VCO clock path. This pin is intended to be used for functional test or PLL bypass.

LKLPCKIP/N Link Loop Clock input: This signal will clock the serial data flip-flop when the link loop enable signal is high.

LKLPDTIP/N Link Loop Data input: This signal will be applied to the serial data flip-flop D input when the link loop enable signal is high.

LNKLPEN Link Loop Enable input: This signal controls the path of the 2:1 mux's which determine the inputs to the serial data flip-flop. A low will enable the link loop inputs. A high will enable the serial data and the serial clock inputs.

LOCLPEN Local Loopback Enable: Enables the loopback data outputs.

SERDATEN Serial Data Enable: Enables the serial data outputs.

SERDATOP/N Serial Data Out: RECLocked serial data which is enabled by the serial data enable signal.

SERDATIP/N Serial Data In: Serial data input from the array which must meet the setup and hold time of the FF clocked by the serial clock.

LPDATOP/N Loopback Data Out: Same signal as serial data out except it is enabled by the loopback enable pin. The serial clock will be output on these pins if enabled by the VCOOEN pin.

SERCLKOP/N Serial Clock Out: Output of the divide by N block.

LOCKDET Lock Detect: This signal indicates the phase locked loop has acquired bit synchronization. It will be initially low until approximately 2500 edges are seen at the reference clock input.

BYTCLKIP/N Byte Clock In: This clock input form the array should be equal in frequency to the reference clock input. It is used by the CSU to establish frequency and phase lock to the reference clock input.

TESTEN Test Enable: Test clock enable input pin routed to the array.

LOCKDETA Lock detect to array: This pin functions identically to LOCKDET except it is an array output instead of an output pin.

REFCKOUT Reference clock out to array: This is a buffered version of the reference clock input.

TSTRST Test Reset: This signal will reset the divide by 2, 4 and 8 counters. The divide by 2, 4 and 8 counters will be free running if this signal is not used.

VCOOEN VCO Output Enable: This signal will enable the serial clock onto the loopback data outputs. This function can be used for test purposes or as a high frequency clock output.

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

CSU12 CLOCK SYNTHESIS MACROS

		L MIN/MAX	S MIN/MAX	H MIN/MAX	
T_{su}	(SERDATIP, SERDATIN) *			60	ps
T_h	(SERDATIP, SERDATIN) *			180	ps
	* WITH RESPECT TO SERCLKOP				
OPERATING FREQUENCY:				600 ± 12 %	MHz
k_{fo}, k_{net}	rising LOCKDETA, REFCKOUT			1.80/3.90	ps/LU
	falling			3.00/6.50	ps/LU
kf_o,k_{net}	rising TESTEN, SERDTOP, SERDTON			1.44/3.12	ps/LU
	falling			2.40/5.20	ps/LU
k_{fo},k_{net}	rising SERCLKOP			1.08/2.34	ps/LU
	falling			1.50/3.25	ps/LU
k_{cap}	rising SERDATOP,SERDATON, LPDATOP,LPDATON			21/46	ps/pF
	falling			21/46	ps/pF
k_{cap}	rising LOCKDET			33/72	ps/LU
	falling			33/72	ps/LU
COM4 ADJ. FACTOR:				1.05/1.03	

DIVNCNT0, DIVNCNT1, DIVNCNT2, SERDATIP, SERDATIN, BYTCLKIP, BYTCLKIN, TSTRST, SERDATEN, LNKLPEN, LOCLPEN, VCOOEN - EACH MUST BE DRIVEN BY A MACRO.

AMCC Q20000 SERIES - CSUxx COM5 (210)

Minimum and maximum specifications account for temperature, voltage, and process variations over the COM5 operating range

CSU12 CLOCK SYNTHESIS MACROS

	L	S	H	
ARRAY: Q20P010				
CHIPMACRO: Q20P010MIX10K, Q20P010MIX100K				
ICC			4	mA
IEE			159	mA
FAN-IN DIVNCNT1,DIVNCNT2, TSTRST,SERDATIN, SERDATIP,REFCKINP, REFCKINN,TSTCLKEN, LKLPDTIP,LKLPDTIN, LKLPCKIP,LKLPCKIN			1	load
DIVNCNT0,LNKLPEN, LOCLPEN,SERDATEN, VCOOEN,BYTCLKIP, BYTCLKIN			2	loads
FAN-OUT TESTEN			15	loads
LOCKDETA			17	loads
SERDTOP,SERDTON, REFCKOUT			18	loads
SERCLKOP			30	loads
SIZE			1	G cell

CLOCK SYNTHESIS MACRO DESCRIPTION:

The CSU12 will align the phase and frequency of the byte clock (supplied from the array) and the reference clock (supplied from the external oscillator). The VCO frequency will power up at the center frequency and then phase and frequency lock the byte clock to the reference clock.

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The final VCO frequency will be a multiplied value of the reference clock input. A typical frequency multiplication factor is 20 but can go as high as 64. A byte clock counter in the array should take the serial clock output (as programmedby the DIVNCNTi pins) and divide it down to match the reference clock input.

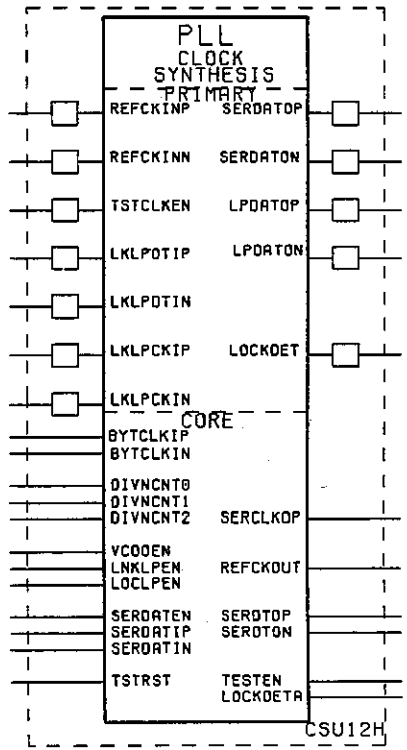
As an example: if a 50MHz reference clock is used and a 500 MHz serial clock is selected, the byte clock counter should divide the 500 MHz serial clock by 10 and drive the byte clock differential inputs with the output of the counter.

The VCO will wait until the byte clock input has stabilized by detecting two consecutive clock cycles with identical periods and then adjust the phase of the VCO to phase align the byte clock with the reference clock. In the actual circuit this alignment may take up to 2.5µsec.

If at any time during the simulation, the byte clock and reference clock frequencies drift by more than 3% the VCO will be phase and frequency shifted to bring the byte clock within the 3% tolerance. In the actual circuit this alignment will be performed continously.

The VCO will be allowed to frequency adjust over a ± 12% range from the center frequency.

The required set up and hold times for the serial clock output to serial data input are shown in the timing table. All other propagation delays are simulated using nominal delay values.



CLOCK SYNTHESIS MACRO CSU12

PIN DESCRIPTIONS FOR FREQUENCY SYNTHESIS MACRO

PIN NAME	PIN COUNT	I/O	POLARITY
REFCKINP	1	diff ECL in	H
REFCKINN	1	diff ECL in	L
DIVNCNT0	1	from array	H
DIVNCNT1	1	from array	H
DIVNCNT2	1	from array	H
TSTCLKEN	1	TTL in	H
LKLPCKIP	1	diff ECL in	H
LKLPCKIN	1	diff ECL in	L
LKLPDTIP	1	diff ECL in	H
LKLPDTIN	1	diff ECL in	L
LNKLPEN	1	from array	L
LOCLPEN	1	from array	L
SERDATEN	1	from array	L
SERDATOP	1	diff ECL out	H
SERDATON	1	diff ECL out	L
SERDATIP	1	from array	H
SERDATIN	1	from array	L
LPDATOP	1	diff ECL out	H
LPDATON	1	diff ECL out	L
SERCLKOP	1	to array	H
LOCKDET	1	TTL out	H
BYTCLKIP	1	from array	H
BYTCLKIN	1	from array	L
TESTEN	1	to array	H
LOCKDETA	1	to array	H
REFCKOUT	1	to array	H
TSTRST	1	from array	H
VCOOEN	1	from array	L

REFCKINP/N This clock should be equal in frequency to the byte clock (BYTCLKIP/N) input from the array. The clock synthesis macro will frequency and phase lock the byte clock to the reference clock. This pin can also be used to bypass the internal VCO when enabled by the TSTCLKEN pin. The reference clock inputs can then be used for functional test or VCO bypass. This path is capable of operating at 1.2GHz.

DIVNCNT0,1,2 Control lines from the array which determine the value of the divide by N counter. Possible values are as follows:

DIVNCNT0	DIVNCNT1	DIVNCNT2	VALUE OF N
1	x	x	1
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16

TSTCLKEN Enables the reference clock through the VCO clock path. This pin is intended to be used for functional test or PLL bypass.

LKLPCKIP/N Link Loop Clock input: This signal will clock the serial data flip-flop when the link loop enable signal is high.

LKLPDTIP/N Link Loop Data input: This signal will be applied to the serial data flip-flop D input when the link loop enable signal is high.

LNKLPEN Link Loop Enable input: This signal controls the path of the 2:1 mux's which determine the inputs to the serial data flip-flop. A low will enable the link loop inputs. A high will enable the serial data and the serial clock inputs.

LOCLPEN Local Loopback Enable: Enables the loopback data outputs.

SERDATEN Serial Data Enable: Enables the serial data outputs.

SERDATOP/N Serial Data Out: RECLocked serial data which is enabled by the serial data enable signal.

SERDATIP/N Serial Data In: Serial data input from the array which must meet the setup and hold time of the FF clocked by the serial clock.

LPDATOP/N Loopback Data Out: Same signal as serial data out except it is enabled by the loopback enable pin. The serial clock will be output on these pins if enabled by the VCOOEN pin.

SERCLKOP Serial Clock Out: Output of the divide by N block.

LOCKDET Lock Detect: This signal indicates the phase locked loop has acquired bit synchronization. It will be initially low until approximately 2500 edges are seen at the reference clock input.

BYTCLKIP/N Byte Clock In: This clock input form the array should be equal in frequency to the reference clock input. It is used by the CSU to establish frequency and phase lock to the reference clock input.

TESTEN Test Enable: Test clock enable input pin routed to the array.

LOCKDETA Lock detect to array: This pin functions identically to LOCKDET except it is an array output instead of an output pin.

REFCKOUT Reference clock out to array: This is a buffered version of the reference clock input.

TSTRST Test Reset: This signal will reset the divide by 2, 4 and 8 counters. The divide by 2, 4 and 8 counters will be free running if this signal is not used.

VCOOEN VCO Output Enable: This signal will enable the serial clock onto the loopback data outputs. This function can be used for test purposes or as a high frequency clock output.