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Application Note 4 Timing Analysis for Bipolar Arrays

CHAP 11 - APPLICATION NOTE 4
TIMING ANALYSIS FOR BIPOLAR ARRAYS

There has been a significant specification change for the Q3500 series since this application note was first drafted. The fanout limits were changed as follows:

	FROM	TO
S option	6	9 loads
L option	3	4
H option	6	9
3-state drivers	12	8
drivers	15	15

The application note will be redone ASAP. In the meantime, corrections have been indicated.

JANUARY 1985

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Deleted - See Design Guides

APPENDIX B

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2. 15 loads on a High-fanout driver
3. 4-Bit Twisted Tail Mobius, Ring, Johnson counter
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Q1500 Example
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Q3500 Example
1. High-Speed TTL I/O

TIMING ANALYSIS - Q700, Q1500, Q3500 SERIES ARRAYS
JANUARY 1985 - DATED MATERIAL

TIMING ANALYSIS
FOR THE AMCC Q700, Q1500, Q3500 SERIES LOGIC ARRAYS

Prior to schematic capture, a preliminary analysis of the critical paths of a circuit is usually performed to assure that the circuit may be placed on a given array.

A detailed timing analysis of a circuit and its critical paths is required before a circuit can be submitted for place and route.

Timing analysis of a circuit generally includes: worst-case path propagation delays for both rising and falling edge inputs for all critical or suspected critical paths; external/internal set-up, hold and recovery time; pulse skew/tracking due to placement (process variation); pulse distortion due to wire-OR and fanout loading (pulse stretch, pulse shrink); and the maximum frequency of operation (worst-case).

If a DAISY, MENTOR or VALID engineering workstation (EWS) is used for schematic capture, timing analysis is supported by the simulation portions of the EWS software. On the DAISY, for example, the DAISY TIMING VERIFIER (DTV) is used to measure propagation delays, perform timing checks, and to evaluate overall circuit timing.

- Loading and wire-OR* delays are added to the basic circuit information file using the Timing Calculator (TCAL) package.**

- Metal length delays are added after layout using the AMCC BACK-ANNOTATION software package.

- Both TCAL and the back-annotation software alter the circuit parameter file as created by the execution of the SOM_MCF.SING SOM control file and the SOM command. (on DAISY)

DESIGN GUIDE SPECIFICATION

The AMCC design guides for the Q700 logic array series, the Q1500/QH1500 logic arrays and the Q3500 logic array series include the description of the macro libraries for those arrays. The EWS macro graphics are provided with the typical propagation delays, typical current dissipation, along with worst-case set-up, hold and recovery times.

* DAISY: must use component WIRE-ORs
** Front annotation is under β test; Back annotation is also under β test.

INTRINSIC Tpd DELAY

The propagation delay specifications in the macro library documentation are typical delay times. The propagation delays given for the input, buffer, and internal logic macros are for unloaded macros. Output macros are specified for 15pf load (TTL outputs) or 5pf load (ECL outputs).

MACRO OPTIONS

The Q700 library has a power (P) option in addition to the standard (S) version of many of its macros (drivers excepted). In most of the specifications, the Tpd specification appears in the S column only. The Tpd parameters for the P option macro are identical to those of the S option macro. The only parameters which change between them are the current drain and the fanout limitation.

The Q1500/QH1500 library has a power (P) option and a high-speed (H) option in addition to the standard (S) option of many of its macros. The Tpd parameters for the P option macro are identical to those of the corresponding S option macro, while current and fanout restrictions are increased.

The Q3500 library has a low-power (L) option and a high-speed (H) option in addition to the standard (S) version of most of its macros. In this design guide the timing is listed in each column. The fanout for the H and S options is 6 loads and the fanout for the L option macros is 3 loads.

DESIGN GUIDE IS THE REFERENCE

The graphic symbol on the DAISY, MENTOR and VALID libraries currently shows the unloaded propagation delay in the upper right corner if there is only one path through the circuit. No propagation delay appears on the macro if there are different delays for different paths. Future versions of the libraries will delete this information from the graphic symbol.

In any case, the designer must reference the design guide. It should always be the overriding reference for the macro parameters.

PATH PROPAGATION DELAY

Computation of the propagation delay for a circuit path involves an evaluation of the following: input, buffer, logic and output macro propagation delays (Tpd, Tpd+, Tpd-); loading (fanout, wire-OR) on each macro in the path (tpd+, tpd-); capacitive loading on the output macros (delta-Tpd); circuit classification (COMMERCIAL, MILITARY); circuit I/O mode (TTL, ECL, TTLMIX); set-up, hold or recovery times as they affect the path; and an estimate of the metal (etch) delays.

For front annotation, multipliers which approximate the metal delay are used. After layout (auto-place and auto-route) the actual etch lengths are known and can be substituted. (Translator portion)

For the Q700 and Q1500 series arrays, TTL inputs will use a different multiplier than the other macros for propagation and set-up and hold computations. For the Q3500 series arrays, the multiplier for the TTL input macros is the same as for the rest of the macros.

TABLE 12
WORST-CASE DELAY MULTIPLICATION FACTORS

1.5	--- For COMMERCIAL applications (ALL BUT TTL INPUT MACROS) $0^{o}C$ to $70^{o}C$, ±5% power supplies
2.0	--- FOR TTL INPUTS - COMMERCIAL APPLICATIONS
1.6	--- For MILITARY applications (ALL BUT TTL INPUT MACROS) $-55^{o}C$ ambient to $+125^{o}C$ case ±10% power supplies
2.5	--- FOR TTL INPUTS - MILITARY APPLICATIONS

$$Tpd_{|typical} * M.F. = Tpd_{|worst\text{-}case}$$

TTL INPUT TYPICAL Tpd DELAYS - Q700, Q1500 ARRAYS ONLY

Circuits with TTL input macros will need to group the TTL input propagation delay serarate from the propagation delays of all other macros since the TTL macros will use a different worst-case commercial or military multiplier (2.0 or 2.5) from the rest of the macros in the path (1.5 or 1.6). Where a buffer or logic/buffer is included in the input macro, as for the Q1500 series macros, the macro will be specified with two sets of Tpd delays, one group for the input translation which will use the larger multiplier, and one for the logic/buffer which will use the same multiplier used with the rest of the macros in the path.

TTL INPUT TYPICAL Tpd DELAYS - ALL ARRAYS

TTL input macros are provided with a rising edge and a falling edge propagation delay. Any circuit which uses 100% TTL or TTLMIX input macros must compute both the rising edge input and falling edge input path delays. Asymmetrical set-up and hold times must also be evaluated.

100% ECL circuits should also compute rising and falling edge input delays for propagation delay and set-up and hold time.

TYPICAL LOADING DELAY

Once the macro propagation delays are listed, the next step in performing timing analysis on a circuit designed for any of the arrays in the Q700, Q1500 or Q3500 series is to evaluate the loading for each macro in the circuit path. The typical rising edge delays due to load (tpd+) and the typical falling edge delays due to load (tpd-) are listed in the table below.

TYPICAL PROPAGATION DELAY DUE TO LOADING

Array Series:	Macro Option:	tpd+ ns/load	tpd- ns/load
Q700:	S	0.05	0.10
	P	0.05	0.10
	Driver	0.05	0.10
Q1500:	S	0.05	0.10
	P	0.05	0.10
	H	0.05	0.10
	Driver	0.05	0.10
Q3500:	S	0.03	0.05
	L	0.03	0.10
	H	0.03	0.05
	Driver	0.03	0.03

Multiple output macros could have different loads on each output and each output will belong to a separate timing path.

TIMING ANALYSIS - Q700, Q1500, Q3500 SERIES ARRAYS
JANUARY 1985 - DATED MATERIAL

TYPICAL WIRE-OR DELAY

The wire-OR loading, if any wire-ORs appear in the path, must also be considered. The typical rising edge delays due to wire-OR connections (tpd+) and the typical falling edge delays due to wire-OR connections (tpd-) are listed in the table below.

There are significant differences in the Q3500 family in the sense that tpd+ is slower than tpd-, the reverse of the Q700 and Q1500 series logic arrays. This is because of the high resistance of the oxide ISO process. The tpd- actually becomes faster as more outputs are wire-ORed due to more current capacity. The Q3500 series is limited to low-power options only for WIREOR4.

Other concerns, do not wire-OR mixed options, do not wire-OR high-fanout drivers, do not cascade wire-ORS and honor individual macro restrictions.

TYPICAL PROPAGATION DELAY DUE TO WIRE-OR

Array Series:	Net Size:	tpd+ ns	tpd- ns	
Q700:	WIREOR2	0.05	0.10	
	WIREOR3	0.10	0.20	
	WIREOR4	0.15	0.30	(limit, S or P option)
Q1500:	WIREOR2	0.05	0.10	(limit P, H options)
	WIREOR3	0.10	0.20	
	WIREOR4	0.15	0.30	(limit, S option)
Q3500:	WIREOR2	0.10	0.05	
	WIREOR3	0.20	0.05	(limit for S, H)
	WIREOR4	0.30	0.05	(limit for LP option)

Q1500 EXAMPLE

For example, if a Q1500 macro has an unloaded propagation delay (Tpd) of 1.3ns, is wire-ORed with two other sources (WIREOR3) and fans out to six loads, the total net is:

2 (# of wire-or inputs - 1) $+ 6$ (load outputs) $= 8$ wires total.

- The added delay due to loading is:
  8 * 0.05 = 0.40ns for the rising edge.
  8 * 0.10 = 0.80ns for the falling edge.

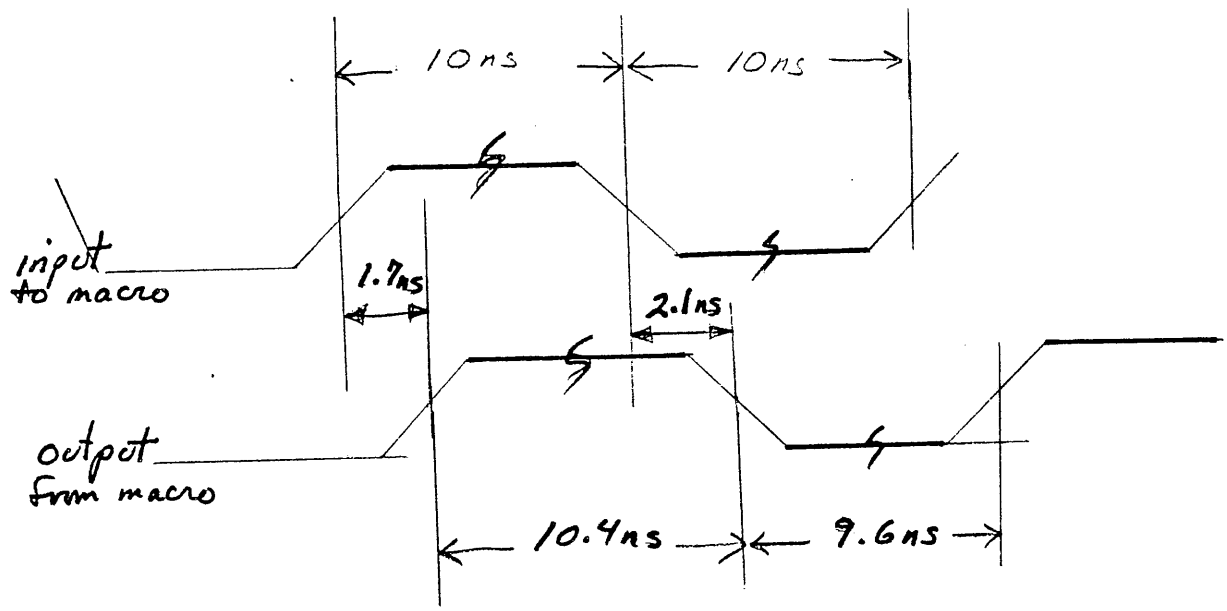
- The rising edge delay through the loaded macro totals:
  1.3 + 0.4 = 1.7ns TYP

- The falling edge delay through the loaded macro totals:
  1.3 + 0.8 = 2.1ns TYP (one decimal place accuracy)

PULSE DISTORTION

For heavily loaded paths, the designer should alternate the signals through inversion to cancel the cumulative effect of the difference between rise and fall delays. Otherwise, pulse stretch and pulse shrink become areas of concern and can lower the maximum operating speed for the circuit such as the case when the pulse shrink results in a pulse that falls below the minimum pulse width requirements for a macro.)

TYPICAL PROPAGATION DELAY THROUGH 1 MACRO, Tpd=1.3ns, 6 LOADS, WIREOR3



FANOUT LIMITATIONS

Different macros have different loading limitations, as summarized in the table shown on the next page. Loading limits for clock paths and distortion-sensitive paths should be derated by 20%. Fanout violations or fanout in excess of derated levels should be checked when performing the timing analysis.

FANIN RESTRICTIONS

The loading that a typical macro presents to its driving source is one load. For those cases where the fanin is greater than one, an "*" is used on the pin (on the EWS graphic) and a notation is made in the design guide.

Some macros look like they present two or more loads to their driving source when they do not. In this case an "*" is used on the pin and a notation is made in the design guide.

Q700 TTL output macros being driven by internal logic (100% TTL mode) require that the fanout of their driving source be derated. This is equivalent to the output macros having a fanin of three. The Q700 design guide in the future will carry an "*" and a comment on these macros.

Q700 FANIN:

OUTPUT MACRO	3 LOADS
OTHERS	1
	exceptions as specified

FANOUT RESTRICTIONS:
(STANDARD/DERATED)

Q700 Series	Macro Option: S	P
Unbuffered input macros	1	-
Input buffers	6/4	9/7
Logic	6/4	9/7
Output buffers	1	
Output macros	REFER TO DATA SHEET	
D cell drivers	16	
Three-state enable drivers	8	
High-fanout drivers	15/12	

Q1500 Series	S	P	H
Unbuffered input macros-TTL	1	-	-
Unbuffered input macros-ECL	8	-	-
Buffered input macros	6/4	6/4	6/4
Logic	6/4	9/7	9/7
Output buffers	1		
Output macros	REFER TO DATA SHEET		
Three-state enable drivers	8	-	-
High-fanout drivers	15/12	-	-

Q3500 Series	S	L	H
Unbuffered input macros-TTL	1	-	-
Unbuffered input macros-ECL	8	-	-
Input buffers	9/7	4/3	9/7
Logic	9/7	4/3	9/7
Output buffers	1	-	-
Output macros	REFER TO DATA SHEET		
Three-state enable drivers	8	8	8
High-fanout drivers	15/12	15/12	15/12

- Latch output may be restricted from wire-OR - check the individual macro documentation
- Unbuffered input macros cannot be wire-ORed
- Output buffers cannot be wire-ORed

HIGH-CAPACITIVE LOADING ON OUTPUT MACROS - ALL ARRAYS

The design guides specify that timing is given for a 15pf load for TTL output macros and a 5pf load for ECL macros. TTL outputs can handle up to 50pf loading at a cost of 2.0ns per timing parameter for the added 35pf load. ECL outputs with high capacitive loading will add 80ps (0.08ns) to each timing parameter per each 1pf over the specified 5pf load.

PROPAGATION DELAY MULTIPLICATION FACTORS

All of the tables shown in this note and all of the macro propagation delay specifications given in the design guides provide typical propagation delays. To perform worst-case analysis, the following multipliers must be used.

WORST-CASE MULTIPLICATION FACTORS

Circuit Classification:	Array Series:	Macro Type:	M.F.
Nominal	any	any	1.0
Commercial	Q700;Q1500	TTL translators	2.0
	Q3500	TTL input	1.5
	any	any other	1.5
Military	Q700,Q1500	TTL translators	2.5
	Q3500	TTL input	1.6
	any	any other	1.6
Minimum	any	any	0.7*

* Guideline only; not guaranteed

These multiplication factors take into account the following:

- Process variations (~30%);
- Temperature variations (~25%);
- Voltage variations (~20%);
- Signal skew;
- Package pin delays;
- Metal length or macro-macro metal delay, both layers, (~10%).

An assumption (100mils/net) is made as to the maximum etch length (first and second layer metal) that will occur. This assumption will hold for all typical connections. Etch runs that wander around the chip (edge to edge, for whatever reason) will experience a longer delay. Most of the actual etch runs will, in fact, experience a shorter delay. The front annotation multiplier was designed to be conservative.

COMMERCIAL SPECIFICATION

Commercial worst-case multipliers are for $0^{o}C$ to $70^{o}C$ with ±5% power supply variation.

MILITARY SPECIFICATION

Military worst-case multipliers are for $-55^{o}C$ ambient to $+125^{o}C$ case with ±10% power supply variation. MIL-STD-883C Class B screening is used.

METAL DELAYS

Metal delays are known after layout. When the metal length for a net exceeds 100 mils, then the added delay due to the etch length over 100 mils must be added into both propagation delay and set-up and hold-time comptations.

TYPICAL METAL DELAYS (ps/mil)

Technology:	Junction-Isolated		Oxide-Isolated	
Array Series:	Q700	Q1500	Q3500	
Macro Option:	S,P	S,P,H	S,H	L
First Metal:	7.0	7.0	5.0	10.0
Second Metal:	4.0	4.0	3.5	7.0

Metal length as accounted for in the worst-case multipliers is assumed to be 100mils/net MAXIMUM. For circuits with longer etch runs, adjustments must be made for the additional delay. A BACK-ANNOTATION program is being developed by AMCC to assist in verification of worst-case paths using actual etch metal lengths as computed by QUASAR (post-layout).

COMPUTING PROPAGATION DELAY

Once the input, buffer, internla logic and output macro propagation delays, loading and wire-OR delays and high-capacitive output macro loading delays are known, the maximum worst-case is computed by:

- Compute the propagation of the falling edge input. The falling edge is typically the worst-case, depending on the alternation of the signal switching.
- Sum the individual macro delays in the path is question. For TTL, TTLMIX circuits, keep the TTL input macro pad->buffer delay (Tpd-) as a separate sum.
- Adjust output macro delays according to the capacitive loading.
- Add the tpd+ or tpd- loading delay (as appropriate) for each input and internal macro. Every connected macro has at least one load
- Add the tpd+ or tpd- wire-OR loading (as appropriate) for any wire-OR in the path.
- IF METAL LENGTHS ARE KNOWN (after routing) add in the metal delays. (Backannotation only.)
- Multiply the sums by the appropriate multiplication factor.
- Add any Tsu, Th or Trec (set-up, hold or recovery time) that affects the path.
- Repeat the process for the rising edge input. For the TTL, TTLMIX input macros, use Tpd+.

PULSE STRETCH, PULSE SHRINK

Compare the results for each path for input rising edge propagation delay and for input falling edge propagation delay. Verify that the minimum pulse width requirements of the latch and flip/flip macros are not violated. If they are, adjust the propagation delay by the amount needed to allow the specified worst-case minimum pulse width specification to be met.

INTRINSIC SET-UP, HOLD AND RECOVERY TIMES

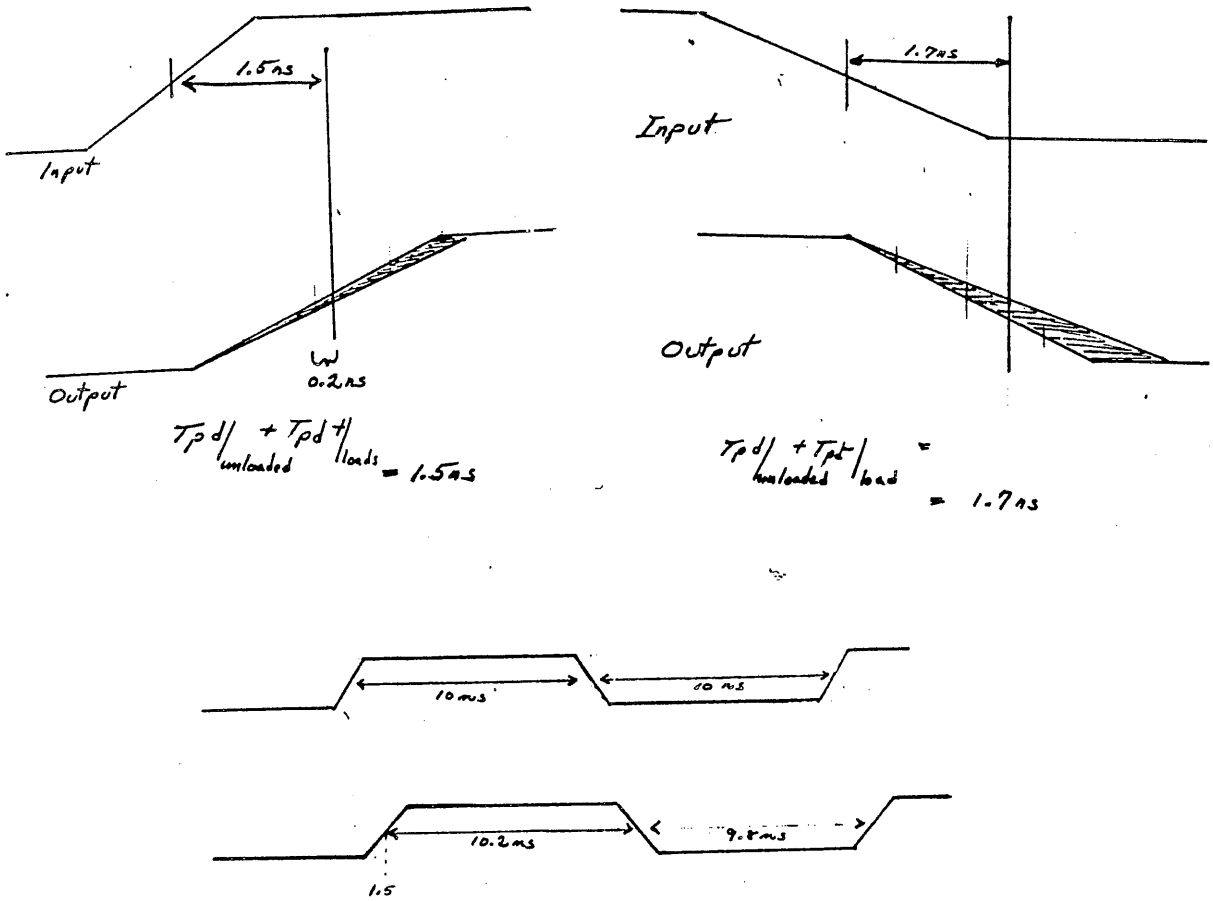
The Tsu, Th and Trec times specified in the design guide for memory macros (latches, flip/flops) are worst-case minimum times and are not multiplied.

INTRINSIC PULSE WIDTH

The pulse width (PW) specifications in the design guide are worst-case minimum.

SELECTING CRITICAL PATHS

Compute the timing for all paths that can or could be considered to be critical to the circuit operation. A critical path may or may not be the longest path in a circuit. A timing PERT chart is a useful tool for multiple path analysis.



Effect of loading on the rise and fall edges for a single macro, 4 loads. Unloaded Tpd = 1.3ns. Loaded, Tpd (+) = 1.5ns; Tpd(-) = 1.7ns. Pulse shrink is at signal = low at 9.8ns; pulse stretch is at signal = high at 10.2ns.

Q700 EXAMPLE

On the next two pages a sample Q700 TTLMIX circuit is shown along with its PERT chart timing analysis. This technique is useful for evaluating the critical path(s) in a circuit. In this case, the longest path is the SELECT path at 14.4ns (TYP). Assume that the capacitive loading on the output macro is <15pf.

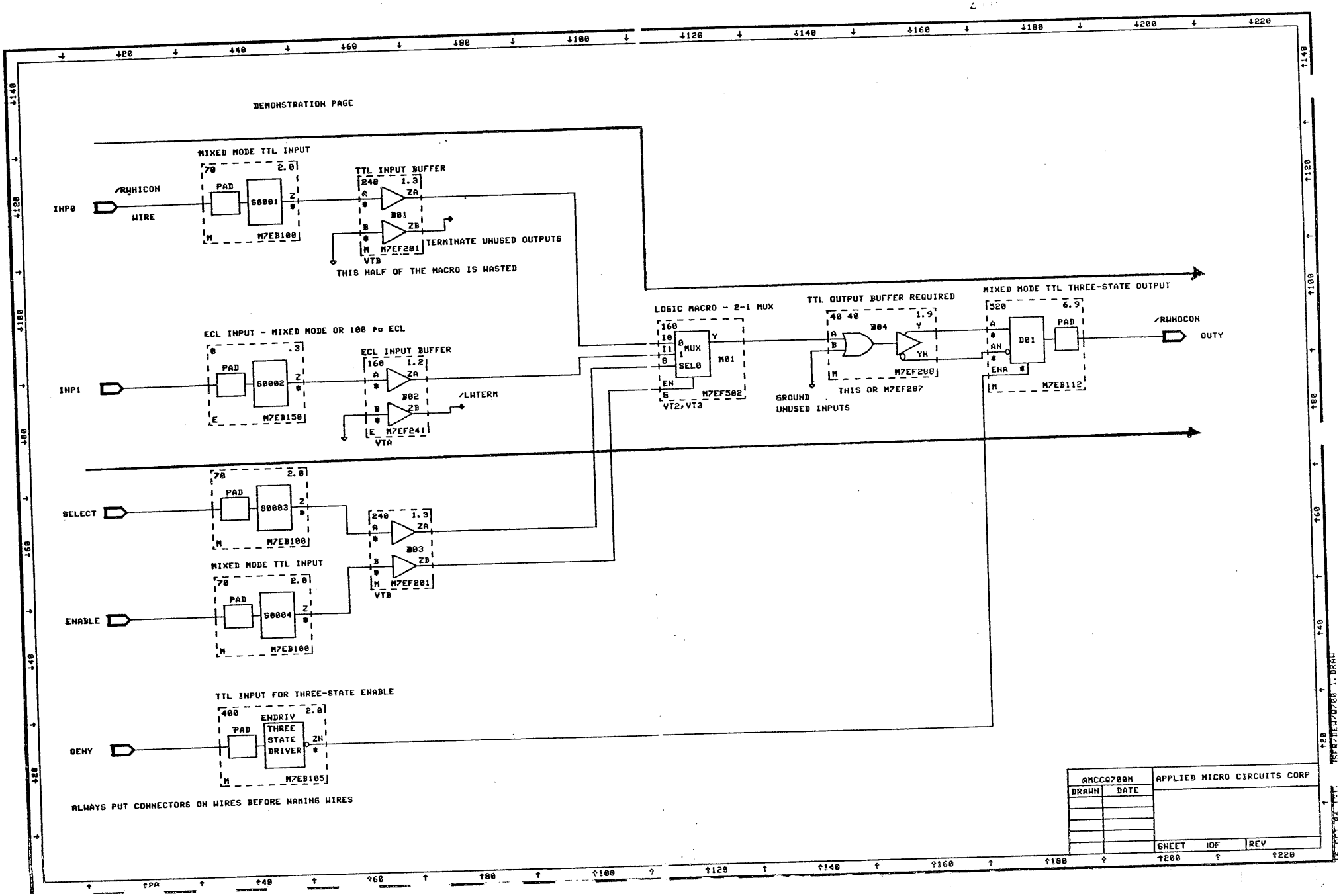
Worst case MILITARY is found by:

TTL input Tpd+:		2.1 * 2.5 = 5.25
Loads (total):	4 * 0.05 = 0.2	(lumped together)
Buffer EF201:		1.3
MUX select->Y:		2.0
Output buffer:		1.9
Output:		6.9
Total		12.3 * 1.6 = 19.68

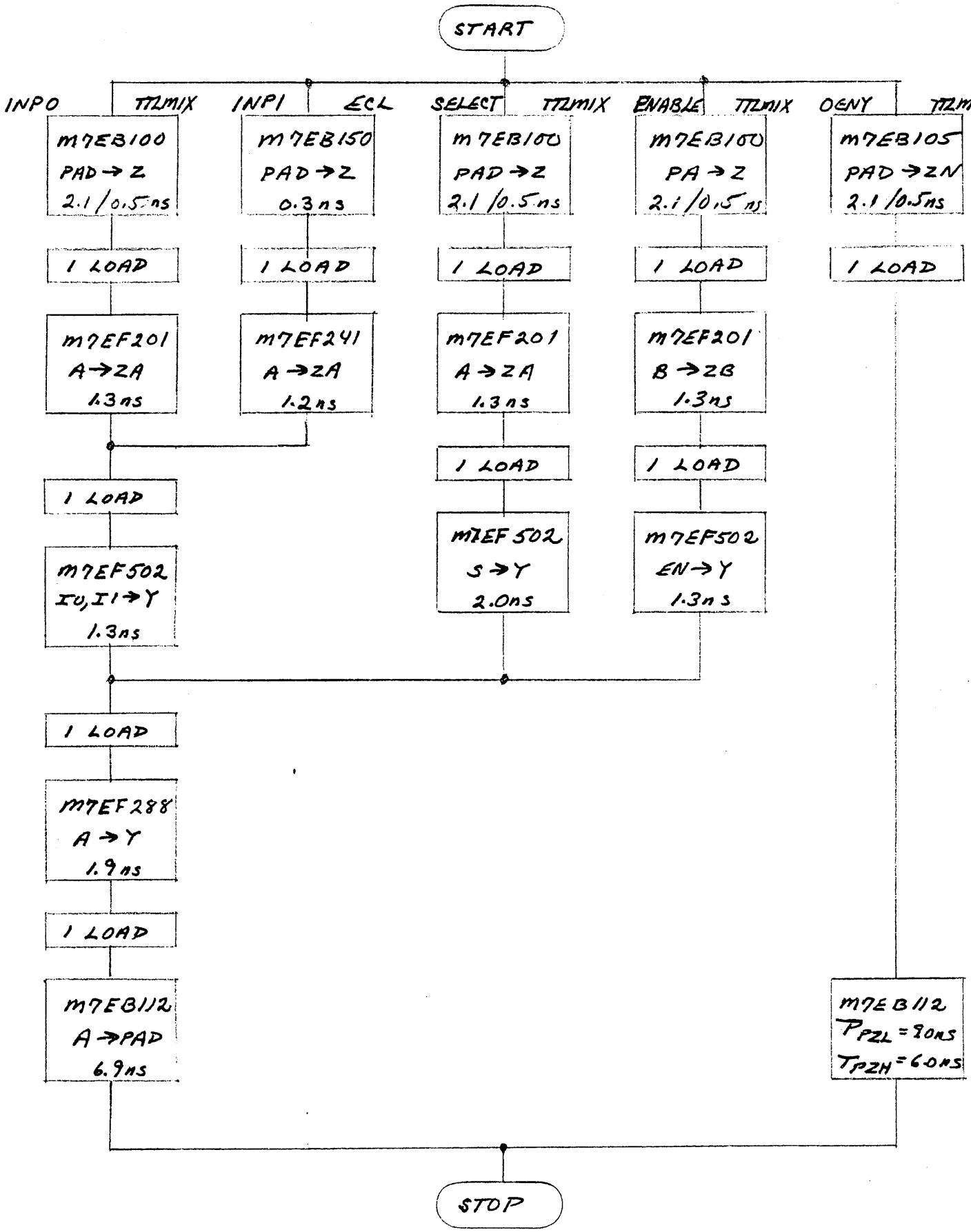
Adding these two together gives 24.93ns worst-case MIL for the rising edge input. Now compute the falling edge input.

TTL input Tpd-:		0.5 * 2.5 = 1.25
Loads (total):	4 * 0.10 = 0.4	
Buffer EF201:		1.3
MUX select->Y:		2.0
Output buffer:		1.9
Output:		6.9
Total		12.5 * 1.6 = 20.0

Adding these two together gives 21.25ns worst-case MIL for the falling edge input.


DEMONSTRATION PAGE
MIXED MODE TTL INPUT
INP0
/RWHICON
WIRE
PAD
S0001
M7EB100
TTL INPUT BUFFER
B01
ZA
ZB
M7EF201
VTB
TERMINATE UNUSED OUTPUTS
THIS HALF OF THE MACRO IS WASTED
ECL INPUT - MIXED MODE OR 100 Po ECL
INP1
PAD
S0002
M7EB150
ECL INPUT BUFFER
B02
/LWTERM
M7EF241
VTA
LOGIC MACRO - 2-1 MUX
MUX
SEL0
M01
M7EF502
VT2,VT3
TTL OUTPUT BUFFER REQUIRED
B04
YN
M7EF288
GROUND
UNUSED INPUTS
THIS OR M7EF287
MIXED MODE TTL THREE-STATE OUTPUT
D01
AN
ENA
M7EB112
PAD
/RWHOCON
OUTY
SELECT
S0003
M7EB100
B03
M7EF201
VTB
MIXED MODE TTL INPUT
ENABLE
S0004
M7EB100
TTL INPUT FOR THREE-STATE ENABLE
OENY
ENDRIV
THREE STATE DRIVER
ZN
M7EB105
ALWAYS PUT CONNECTORS ON WIRES BEFORE NAMING WIRES
AMCC0700M
APPLIED MICRO CIRCUITS CORP
DRAWN
DATE
SHEET 10F
REV

4-22



Q700 2:1 MUX EXAMPLE
(MIXED MODE, TYPICAL VALUES)

Q1500 EXAMPLE

A Q1500 IT02 input macro is connected to an OT21 output macro. What is the worst-case commercial path? The rising edge delay for the IT02 macro is composed of the Tpd+ of the input level conversion and the Tpd of the buffer which are:

Tpd+ = 1.6ns

Tpd buffer = 1.3ns

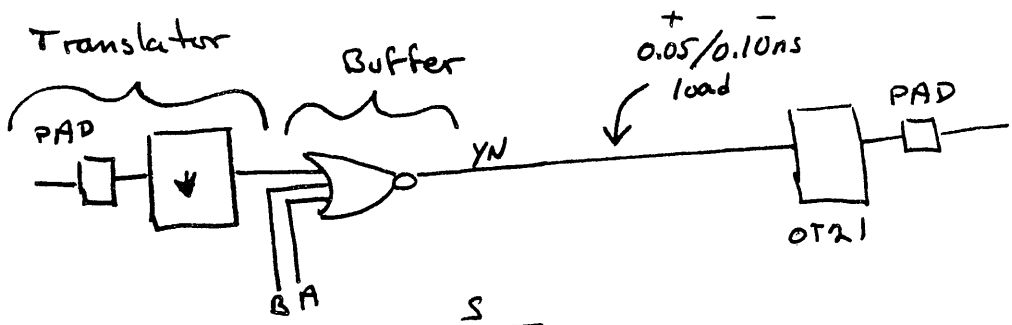
There is one load between the IT02 and the OT21 which contributes 0.05ns. The delay through OT21, assuming that the external capacitive load is <15pf is 7.9ns (buffer and E/T conversion).

The worst case COMMERCIAL rising edge path delay is found by:

(1.6) * 2.0 + (1.3 + 0.05 + 7.9) * 1.5 = 17.08ns

The falling edge delay is:

(0.5) * 2.0 + (1.3 + 0.1 + 7.9) * 1.5 = 14.95ns



		S
$\overline{T}_{pd+}$	PAD → X	1.6
$\overline{T}_{pd-}$	PAD → X	0.5
T_{pd}	+, A, B → YN	1.3

Q3500 EXAMPLE

A partial circuit, a 16:1 MUX composed of MX22L and DE20 macros is shown on the next page. To compute the time delay from page input to page input, choose the select path through the DE20 macro, through the enable of the MUX, through the WIREOR4 to the YOUT page output. Nothing is given about the loading on YOUT.

A->Yi DE20	0.65	
1 load	0.03/0.05	(standard macro)
EN->Y MX22L	1.05	(this is the slow, low-power option)
WIREOR4	.3 /.05	
Total	2.88	rising edge
	3.25	falling edge

Note that the loading tpd+ is different for the Q3500 series and it is option-dependent. A load on the low-power MUX macro would have 0.03/0.10 as its rise/fall time effect.

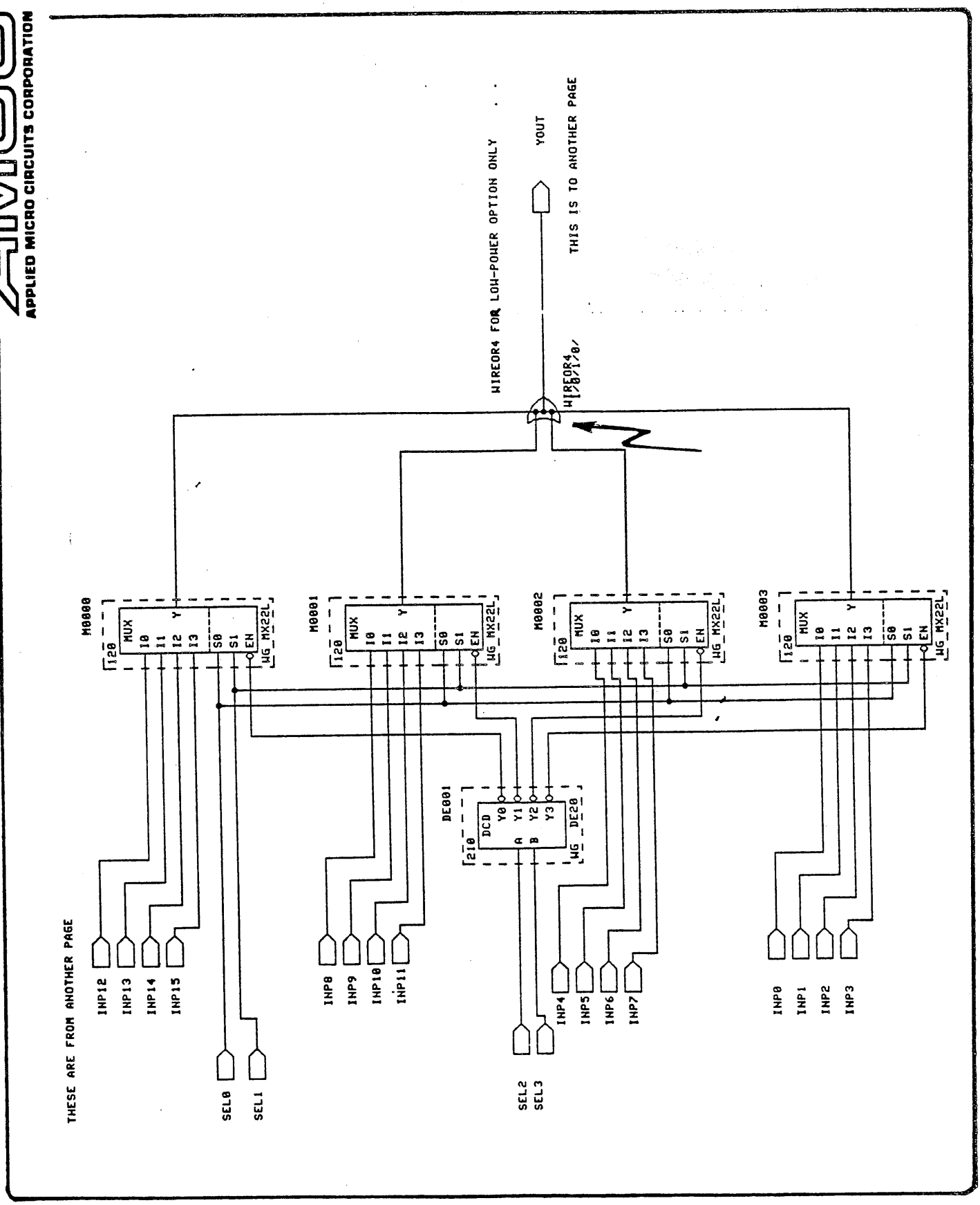
The worst-case MILITARY path is found by multiplying by 1.6; the worst-case COMMERCIAL path is found by multiplying by 1.5.

rising edge

0.65
.05
1.05
.05
1.80ns TYP
* 1.6
2.88ns MIL

falling edge

0.65
.03
1.05
.3
2.03ns TYP
* 1.6
3.25ns MIL


THESE ARE FROM ANOTHER PAGE
INP12
INP13
INP14
INP15
INP8
INP9
INP10
INP11
INP4
INP5
INP6
INP7
INP0
INP1
INP2
INP3
SEL0
SEL1
SEL2
SEL3
M0000
M0001
M0002
M0003
DE001
MUX
I0
I1
I2
I3
S0
S1
EN
Y
WG_MX22L
DCD
A
B
Y0
Y1
Y2
Y3
WG_DE20
WIREOR4 FOR LOW-POWER OPTION ONLY
WIREOR4
YOUT
THIS IS TO ANOTHER PAGE

INTERNAL SIGNAL TRACKING (SKEW)

Factors which affact the signal delay tracking within the array include such things as relative position within the device, process variation, power supply variations, operating temperature, and the characteristics of the various macros.

As a guideline, identical macros located by auto-place and auto-route, exhibit 20% tracking on the same edge (both edges rising or both edges falling). Using preplacement and prerouting, identical macros, plasced adjacent to each other, will exhibit 5% tracking on the same edge. The rising edge effect is 0.5 of the falling edge effect.

This is important when planning clock and reset distribution to register/counter macros.

Process variations are accounted for in the worst-case multiplication factors.

Placement Tracking

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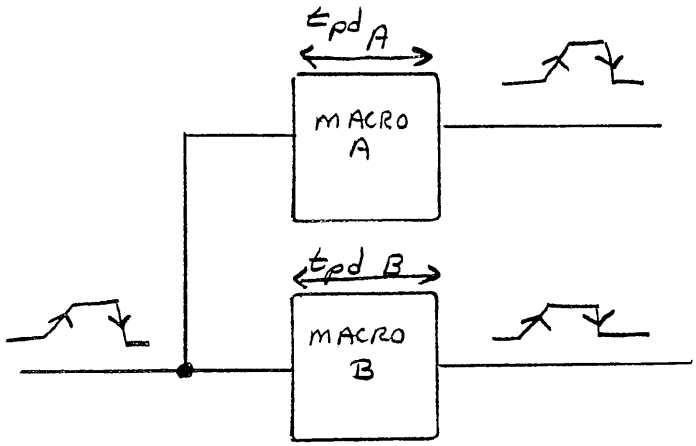


$$\Delta t_{pd}+ \equiv \Delta t_{pd}- = \left| t_{pd_A} - t_{pd_B} \right| = 0.2 * t_{pd}\Big|_{\substack{A \\ (A \text{ or } B)}}$$

If adjacent, preplaced, prerouted

$$\Delta t_{pd}+ \equiv \Delta t_{pd}- = \left| t_{pd_A} - t_{pd_B} \right| = 0.05 * t_{pd}\Big|_{N}$$

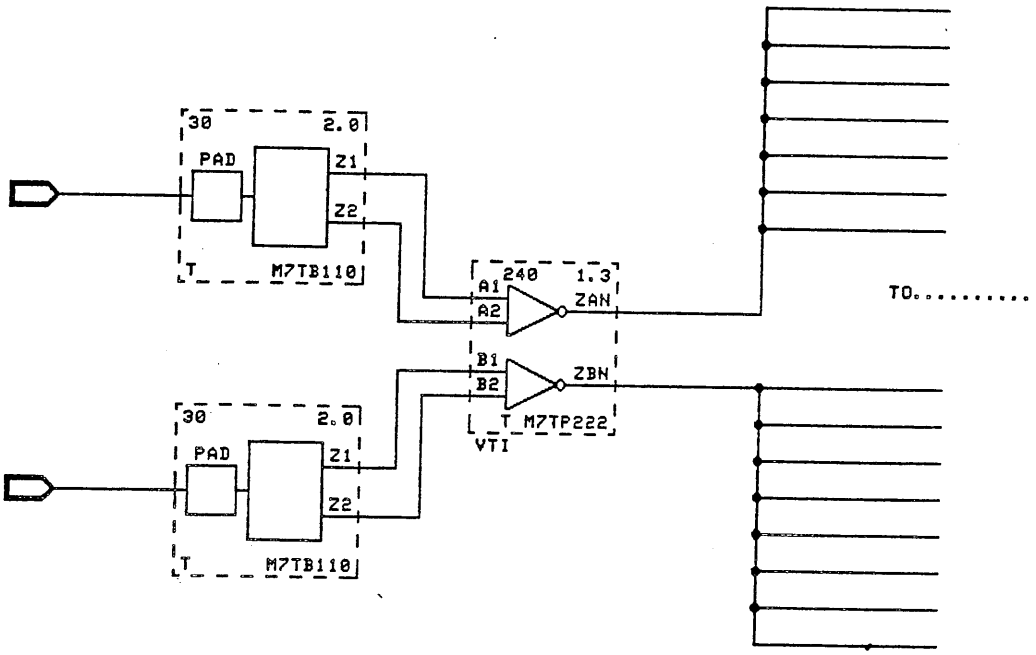
Q700 EXAMPLES

1. M7TB110 INPUT, M7TP222 BUFFER, 15 LOADS.

The loads are evenly distributed across two buffers and two input pads are used. The longest path is the one with 8 loads on the buffer. This is a point to point computation for reference and is not a complete circuit.

	Rising Typical	M.F. MIL	Falling Typical	
M7TB110	2.1	*2.5	0.5	
Worst Case:	5.25ns		1.25ns	MILITARY = 2.5 * TYPICAL (TTL Input only)
		*1.6		
1 Load	0.05		0.10	
M7TP222	1.3		1.3	
8 Loads	0.4		0.8	
Total	1.75ns		2.2ns	
Worst Case:	2.8ns		3.52ns	MILITARY = 1.6 * TYPICAL
Total W.C.:	8.05ns		4.77ns	Sum

The total point-to-point path delay, rising edge input, is 5.25 + 2.8 = 8.05ns. The total for the falling edge input is 4.77ns.



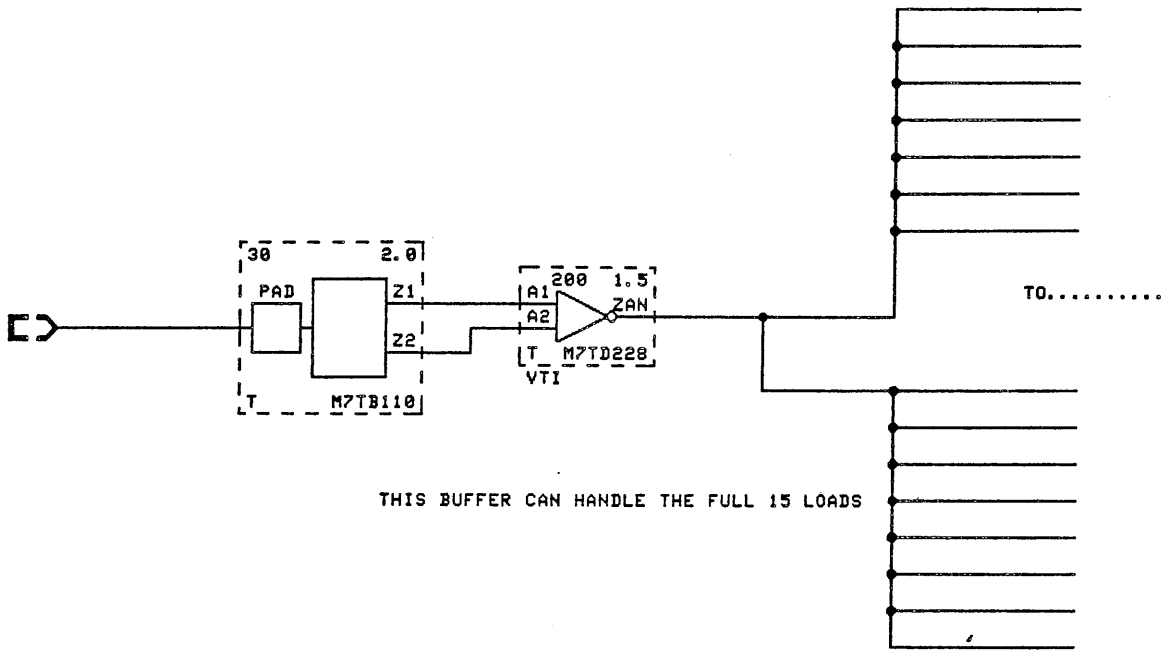
EACH BUFFER DRIVES UP TO AND INCLUDING 9 LOADS
- THIS 15 LOAD OUTPUT IS SPLIT BETWEEN TWO BUFFERS

2. M7TB110 INPUT, M7TD228 DRIVER BUFFER, 15 LOADS

All 15 loads are driven by the high-fanout driver M7TD228. The worst case MILITARY point to point delay is found by:

	Rising Typical	M.F. MIL	Falling Typical	
M7TB110	2.1	*2.5	0.5	
Worst Case:	5.25ns		1.25ns	MILITARY = 2.5 * TYPICAL (TTL input only)
		*1.6		
1 Load	0.05		0.10	
M7TD228	1.5		1.5	
15 Loads	0.75		1.5	
Total	2.3ns		3.1ns	TYPICAL
Worst Case:	3.68ns		4.96ns	MILITARY = 1.6 * TYPICAL
Total W.C.:	8.93ns		6.21ns	Sum

The total point-to-point path delay, rising edge input, is 5.25 + 3.68 = 8.93ns. The total for the falling edge input is 6.21ns.



THIS BUFFER CAN HANDLE THE FULL 15 LOADS

3. 4-BIT TWISTED TAIL (MOBIUS, RING, JOHNSON) COUNTER

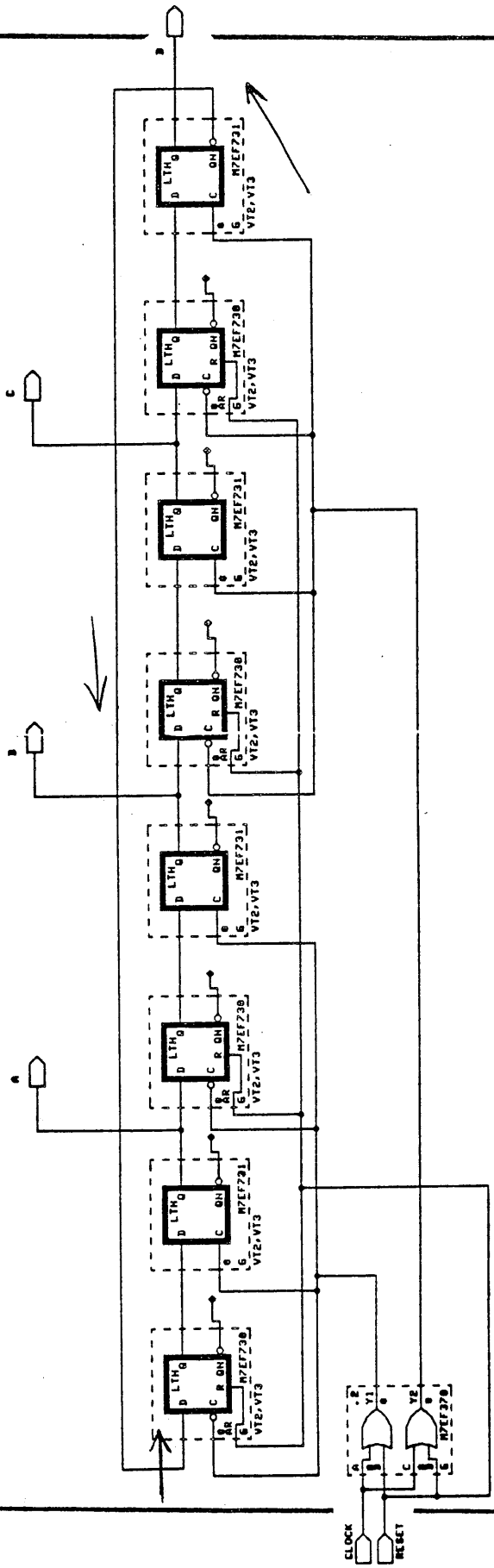
The timing for this circuit depends on the required delay between rising clock edges. The input time for the input macro and clock buffer do not matter so long as they total less than the worst-case path computed below. The worst-case is the clock-to-output of the last stage M7EF731, the loading on QN (2 external loads assumed on all Q, QN although they are not shown), and the intrinsic set-up time for the first stage M7EF730.

Since no TTL input is invloved, the COMMERCIAL worst-case multiplier is 1.5 and the MILITARY worst-case multiplier is 1.6 for all macros and loads shown.

	Rising	Falling	
Clock->QN	1.7	1.7	
3 Loads	0.15	0.3	
T_{set-up}	2.0	2.0	
Total:	3.85	4.0ns	TYPICAL
Worst-case:	6.16	6.4ns	MILITARY = 1.6 * TYPICAL

The speed of this circuit is: 1 / 6.4 = 156.25MHz (worst-case MILITARY).

AMCC
APPLIED MICRO CIRCUITS CORPORATION

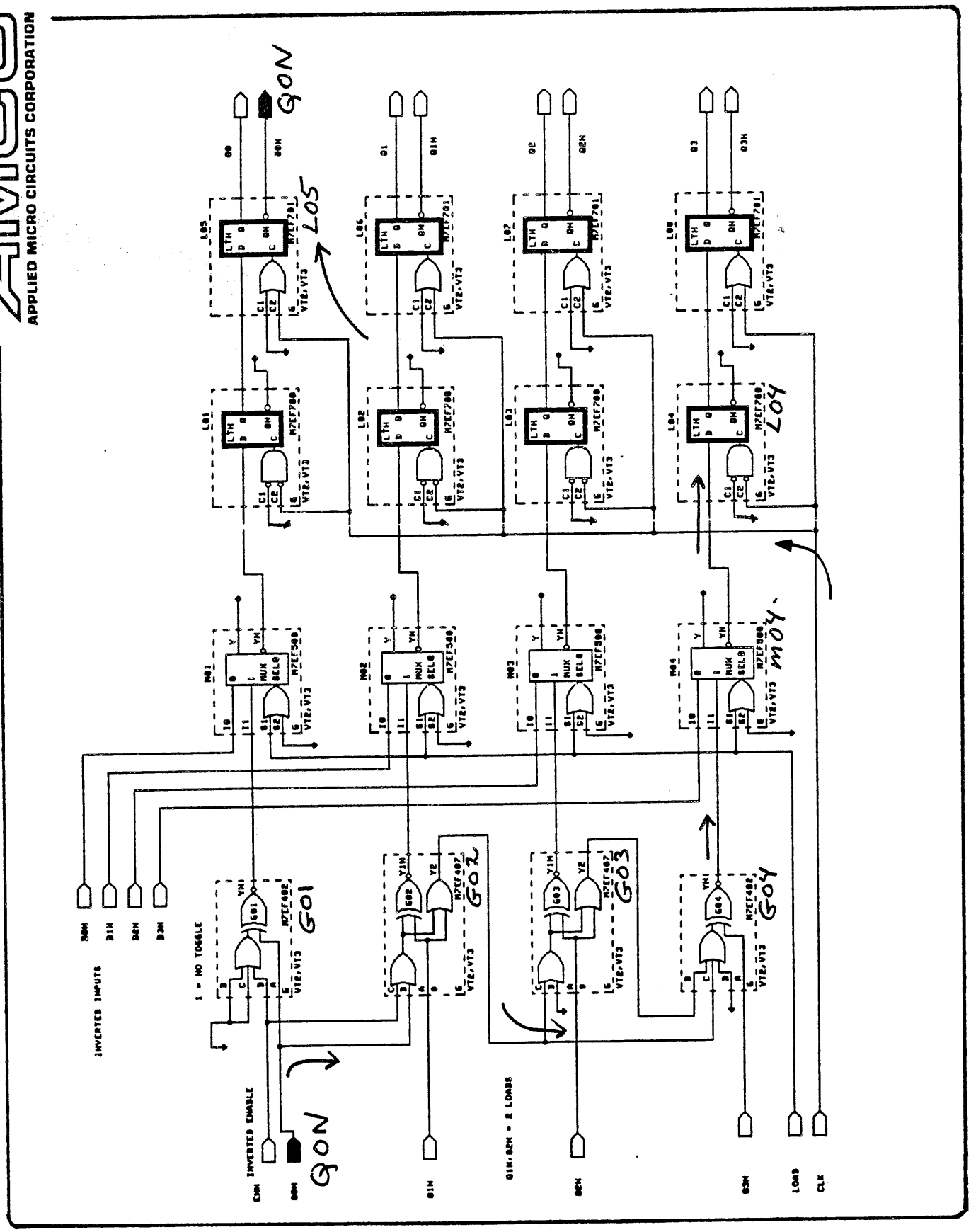


4. 4-BIT PRELOADABLE COUNTER

For this circuit, the rising edge to rising edge delay is also of the most interest. The worst-case (longest) path at first glance appears to be the Q0N generation, fed back to the EXNOR gate G01. Tracing this path produces:

INPUT:	RISING ns	FALLING ns	
Clock->Q0N L05 (M7EF701)	2.0	2.0	
Q0N Loads = 2 loads	0.1	0.2	falling
Tpd G02 (M7EF407) B->Y2	2.0	2.0	
G02 Loads = 2 loads	0.1	0.2	falling
Tpd G04 (M7EF402) C->YN	2.0	2.0	
G04 Loads = 1 load	0.1	0.05	rising
Tpd M04 (M7EF500) I1->YN	1.2	1.2	
M04 Loads = 1 load	0.05	0.1	falling
Total	7.55	7.75	TYPICAL
• Worst case Typical * 1.6 =	12.08	12.40	MILITARY
Tsetup L04 (M7EF700)	2.0	2.0	MIN
• Worst case TOTAL:	14.08	14.40	MILITARY

With a rising-edge to rising-edge delay of 14.40ns worst-case MILITARY, the speed of operation is 69.44MHz. If there are additional loads on Q0N on another page then they must also be factored into the computation before a final value for the path delay can be given. One additional load would add 0.1ns to the time path, and reduce the speed to 68.7MHz.


AMCC
APPLIED MICRO CIRCUITS CORPORATION
INVERTED INPUTS
1 = NO TOGGLE
INVERTED ENABLE
QON
QIN
Q2N
Q3N
LOAD
CLK
QIN, Q2N = 2 LOADS
L01
L02
L03
L04
L05
L06
L07
L08
M01
M02
M03
M04
G01
G02
G03
G04
M2EF701
M2EF708
M2EF508
M2EF402
M2EF407

Q1500 EXAMPLE

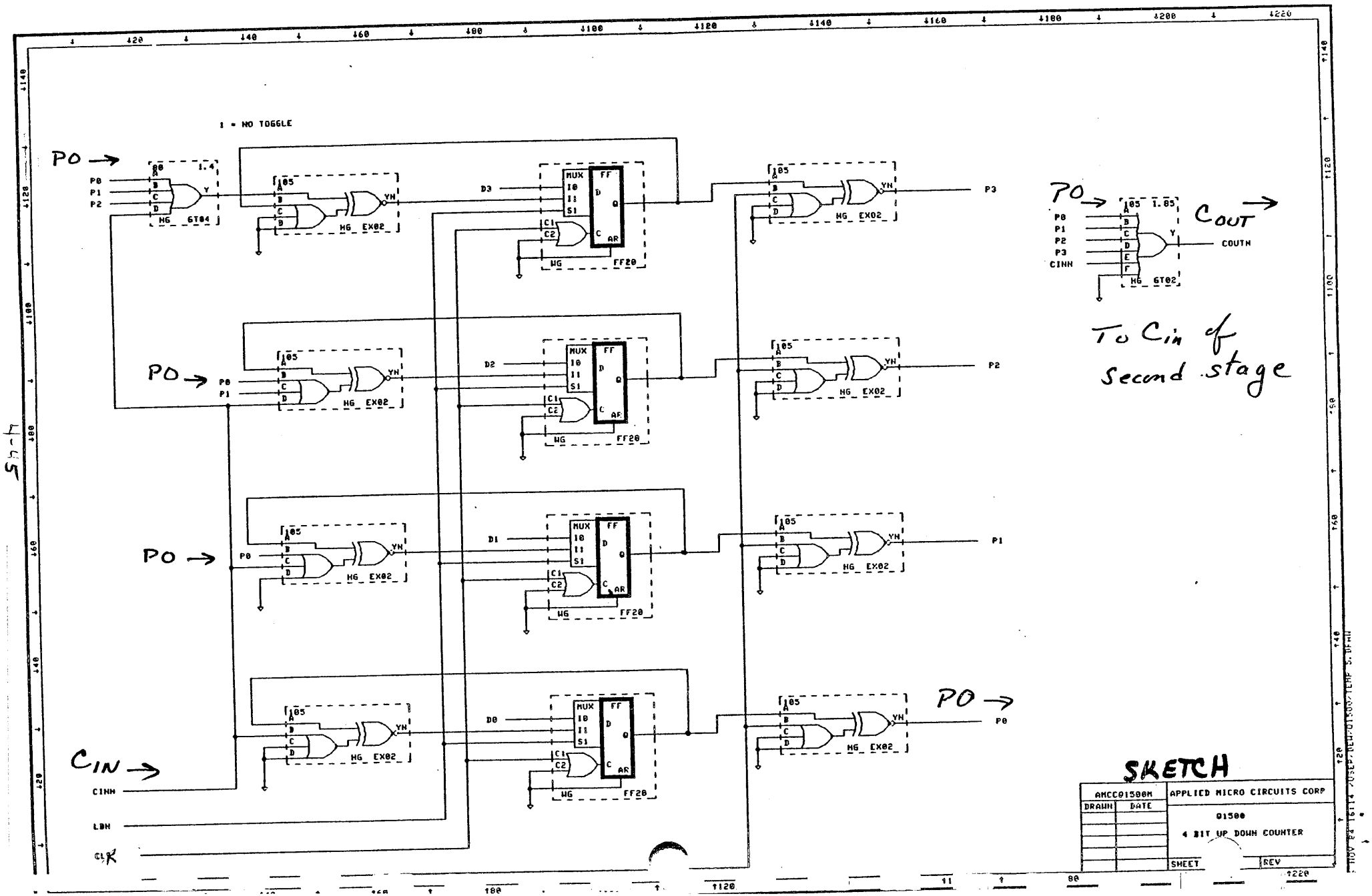
1. 8-BIT UP/DOWN COUNTER

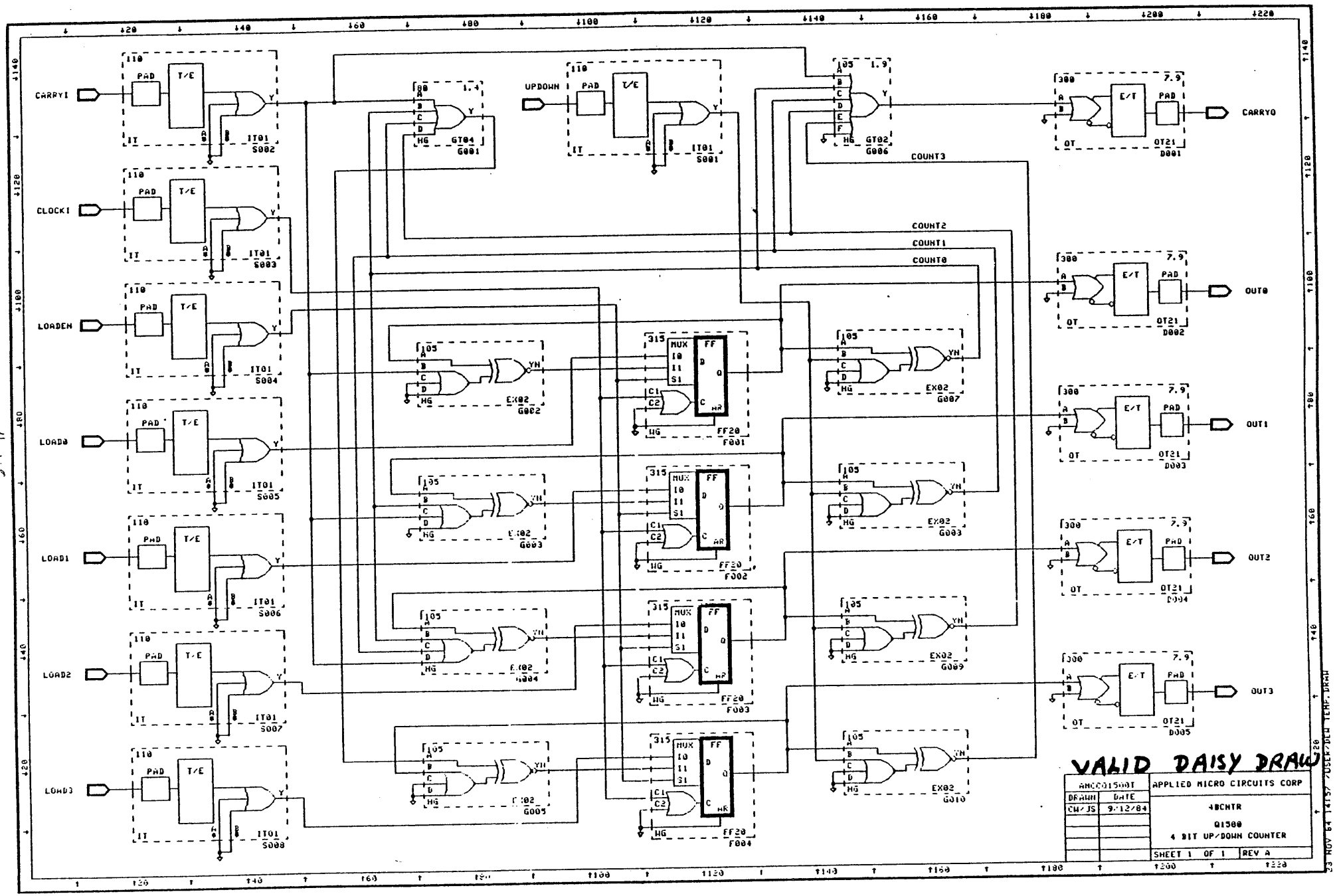
A 4-Bit up/down counter is shown on the following page. (This sketch is not a complete EWS schematic.) A complete 4-bit DIASY schematic is shown on the page following the sketch. (FF20 is an older macro, replace with TBS.)

To build an 8-bit up/down counter, connect two 4-bit counter stages through the C_{out} of the least significant bit stage to the C_{in} of the most significant stage.

Timing for an 8-bit counter is found as follows:

First stage:		
Clock->Q F/F	2.0	
3 Loads (counting output macro)	0.3	falling
Tpd EX02 A->YN	1.3	
4 Loads (P0 generation)	0.2	rising
Tpd GT02 (Cin generation)	1.9	
Second Stage:		
Tpd GT04	1.4	
1 Load	0.05	rising
Tpd EX02 A->YN	1.3	
Total:	8.45ns	TYPICAL
Worst Case = 1.6 * TYPICAL =	13.52ns	
Tsetup F/F	2.0	
Total path delay:	15.52	
Maximum operating frequency:	64.4MHz	MILITARY


1 = NO TOGGLE
P0
P1
P2
P3
D3
D2
D1
D0
CIN
CINH
LDN
CLK
COUT
COUTN
HG_GT04
HG_EX02
HG_GT02
FF20
MUX
FF
To Cin of Second stage
SKETCH
AMCC01500A
APPLIED MICRO CIRCUITS CORP
DRAWN
DATE
01500
4 BIT UP DOWN COUNTER
SHEET
REV


CARRYI
CLOCKI
LOADEN
LOAD0
LOAD1
LOAD2
LOAD3
UPDOWN
COUNT3
COUNT2
COUNT1
COUNT0
CARRYO
OUT0
OUT1
OUT2
OUT3
PAD
T/E
MUX
FF
E/T
VALID DAISY DRAW
ANCC01500T
APPLIED MICRO CIRCUITS CORP
DRAWN
DATE
CW/JS
9/12/84
4BCNTR
Q1500
4 BIT UP/DOWN COUNTER
SHEET 1 OF 1
REV A

- If the carry out of the first stage must go out to another chip (through an output macro), then additional loading must be shown for that load.

- If the two halves of the counter are for some reason on two different arrays, there is a considerable delay through the input and output macro stages (including input and output buffers). The two segments of the counter should be kept on the same array.

Verifying that this is the worst-case path is left as an exercise.

Q3500 EXAMPLE

1. HIGH-SPEED TTL I/O

The simple 3-input OR TTL I/O function on the next page uses H-option macros from the Q3500 library. Worst-case timing is the delay through IT18 and the EN->PAD Tpd for OT32H.

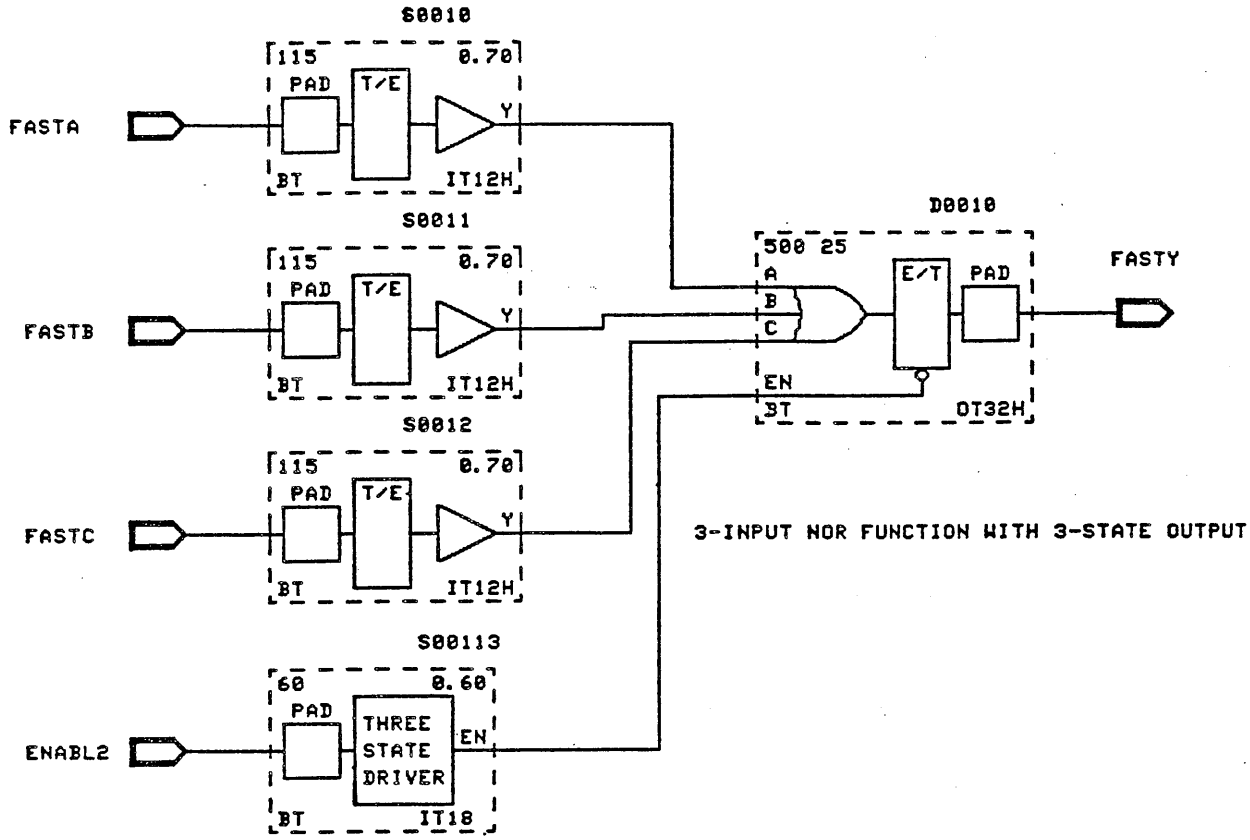
SUMMARY:		Rising	Falling
IT12H	PAD->Y Tpd	2.8	0.6ns
IT18	PAD->Y Tpd	2.7	0.2ns
OT32H	A,B,C->PAD Tpd	3.9	3.9ns
OR32H	EN->PAD Tpd	5.9	5.9ns
1 load	S option	0.03	0.1ns
1 load	H option	0.03	0.5ns

FASTA path = 2.8 + 0.03 + 3.9 = 6.73 ns TYPICAL
ENABL2 path = 2.7 + 0.03 + 5.9 = 8.63 ns TYPICAL

If ENABLE2 had been input to an IT18H:

IT18H	PAD->Y	Tpd	0.8	0.2ns

Then:
ENABLE2 path = 0.8 + 0.03 + 5.9 = 6.73 ns TYPICAL



Naming

A____	=	Adder
B____	=	Buffer
G____	=	Gate
EX____	=	Exclusive or/nor
M____	=	Mux
DE____	=	Decoder
F____	=	Flip flop
L____	=	Latch
MM____	=	Memory module
MI____	=	MSI macro
SP____	=	Special cell
LS____	=	Inputs
D____	=	Outputs
BD____	=	Bidirectional I/O
W____	=	Wireors
X____	=	None of the above

Therefore, the circuit should have used the H option for the three-state enable driver IT18. Additional loads on IT18 would add to the path propagation delay.

Worst case delay is 1.6 * 7.0 ≈ 11.2ns MILITARY worst-case. The Q3500 series has only one multiplier for MILITARY (1.6) and one for COMMERCIAL (1.5).

The Q3500 series library is the only one providing a high-speed option for the three-state enable drivers.