AMCC
APPLIED MICRO CIRCUITS CORPORATION

Application Note 7 Power Considerations For Bipolar Logic Arrays

CHAP 13 - APPLICATION NOTE 7
POWER CONSIDERATIONS FOR BIPOLAR LOGIC ARRAYS

QUESTION: WHAT POWER SUPPLY OPTIONS ARE AVAILABLE?

- +5V SINGLE POWER SUPPLY
  - 100% TTL
  - 100% ECL 10K
  - 100% ECL 100K (QH1500 ARRAY, Q3500 SERIES)
  - TTL/ECL 10K MIXED
  - TTL/ECL 100K MIXED (QH1500; Q3500)
  - ECL 10K/ECL 100K MIXED (Q3500 SERIES)

- +5V AND -5.2V DUAL POWER SUPPLIES
  - TTL/ECL 10K MIXED
  - TTL/ECL 100K MIXED (QH1500; Q3500)

- -5.2V SINGLE POWER SUPPLY
  - 100% ECL 10K
  - 100% ECL 100K (QH1500 ARRAY, Q3500 SERIES)

- -4.5V SINGLE POWER SUPPLY (-4.2V TO -4.8V)
  - 100% ECL 100K (QH1500 ARRAY*, Q3500 SERIES)
    *COMMERCIAL ONLY

- +5V AND -4.5V DUAL POWER SUPPLIES
  - TTL/ECL 100K MIXED (QH1500 ARRAY*; Q3500 SERIES)

QUESTION: WHAT TOLERANCES ARE ALLOWED ON POWER SUPPLIES?

- THE ARRAYS ARE VOLTAGE COMPENSATED
- NORMAL COMMERCIAL RANGE IS SPECIFIED AS ±5%
- NORMAL MILITARY RANGE IS SPECIFIED AS ±10%
- -4.5V SUPPLIES FOR ECL 100K ARE TO BE -4.2V TO -4.8V AND IS FOR COMMERCIAL APPLICATIONS ONLY ON THE QH1500 ARRAY;

QUESTION: WHAT ABOUT THE POWER DISSIPATION ON THE ARRAY?

- IT IS PROGRAMMABLE
  - AMCC PROVIDES OPTIONS ON THE MACROS
    - SUPER HIGH SPEED Q3500 (SOME)
    - HIGH SPEED Q1500, Q3500 SERIES
      Q700 SELECT MACROS
    - POWER Q700, Q1500
    - LOW-POWER Q3500
    - STANDARD ALL ARRAY SERIES

- IF NOT A SPEED-CRITICAL PATH
  CAN USE LOW POWER, SLOWER VERSION OF MACRO
  - BALANCE THE DESIGN
  - QUIDELINE IS NO MORE THAN 30% OF THE
    INTERNAL MACROS ARE P OR H OPTION

QUESTION: WHY IS 30% THE GUIDELINE FOR H AND P OPTION MACROS?

QUESTION: WHAT IS THE MAXIMUM CURRENT SPECIFICATION FOR THE ARRAY?

- IF PREPLACEMENT IS DONE, DO NOT EXCEED THE MAXIMUM CURRENT SPECIFICATION PER ROW

- THE MAXIMUM CURRENT SPECIFICATIONS FOR THE INTERNAL ARRAY (L, B CELLS) ARE DETAILED ON THE LAST PAGES

- THERE IS NO RESTRICTION ON THE NUMBER OF I/O THAT CAN BE P OR H OPTION DUE TO CURRENT LIMITS (VTI load limit)

QUESTION: WHAT IS THE POWER DISSIPATION PER CELL (in mW)?

QUESTION: HOW MUCH POWER IS DRAWN WHEN THE CELL IS NOT USED?

- NO POWER IS USED BY A CELL IN ITS BASE CONFIGURATION

- THE TYPICAL POWER DISSIPATION PER CELL:

ARRAY NAME	POWER (mW)	
Q700	5-8	
Q710	5-8	
Q720	5-8	
Q1500A	5-12	
QH1500A	5-12	
Q3500S	4-15	AVERAGE
	4-9	LOW POWER
	5-11	STANDARD
	7-15	HIGH-SPEED
	TBS	SUPER HIGH SPEED

QUESTION: HOW DO YOU COMPUTE WORST-CASE POWER?

QUESTION: WHAT IS THE OVERHEAD POWER?

- TO COMPUTE THE WORST-CASE POWER FOR A SPECIFIC CIRCUIT:

1. LIST ALL OF THE MACROS AND HOW MANY OF EACH USED IN THE CIRCUIT
    - USE MACROCCUR TABLE ON VAX ERCS (THIS WAS THE MACRO_TAB.DOC FILE)

2. LIST THE CURRENT FOR ONE THEN FOR THE NUMBER USED
    - ON THE ABOVE REFERENCED PRINTOUTS

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MACRO OCCURENCE AND
POWER DISSIPATION TABLE
Revision 1.0.0

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Path name /USER/DEW/MOBIUS
Family G1500
Work station DAISY
Technology T
Date 29-OCT-1984
Time 14:48

The following is the macro occurence table -

old information

MACRO NAME	# USED	SPECS ICC	SPECS IEE	TOTALS ICC	TOTALS IEE
FF13	4	~~0.00~~ 2.85	~~2.85~~	0.00	11.40
DT25	4	6.00	0.00	24.00	0.00
IT01	2	1.10	0.00	2.20	0.00
TOTAL TYP MACRO CURRENT				26.20	11.40
TOTAL TYP OVERHEAD CURRENT					
TOTAL TYP CHIP CURRENT					
TOTAL MAX CHIP CURRENT (TYP CURRENT TIMES 1.4) =					
TOTAL CURRENT =					
WORST CASE POWER DISSIPATION					
VCC ( )v X ( )ma =					Watts
VEE ( )v X ( )ma =					Watts
ECL OUTPUT POWER DISSIPATION					
( )ma X 1.3v X ( )outputs=					Watts
TOTAL POWER DISSIPATION					Watts

FF11 → FF13
FF13 should be Icc in TTL array

Σ these #1.4 and compare to max current for gross check

use worst case Voltage

depends on Termination; duty cycle

3. SUM THE I_{EE} CURRENT

4. SUM THE I_{CC} CURRENT

- THESE SUMS ARE FOR MACRO DISSIPATION

5. COUNT THE NUMBER OF TTL INPUTS

6. IDENTIFY THE POWER SUPPLIES
   (+5V, -5.2V, -4.5V)

7. IDENTIFY THE CIRCUIT MODE
   (TTL, ECL, MIXED, TTL/+5ECL MIXED)

8. FIND THE OVERHEAD CURRENT FROM THE TABLE ON THE NEXT PAGE

- THE CHIP OVERHEAD IS A FUNCTION OF THE:
  - INTERNAL REGULATORS
  - REFERENCE GENERATORS
  - SELECTED I/O MODE

9. ADD THE I_{CC}/I_{EE} TO THE PREVIOUS TOTAL

SUM OF MACRO I_{CC} + $I_{CC|OVERHEAD}$

SUM OF MACRO I_{EE} + $I_{EE|OVERHEAD}$

Maximum worst-case current is found by multiplying the I_{CC} and I_{EE} subtotals by 1.4:

(SUM OF MACROS I_{CC} + overhead I_{CC}) * 1.4 = I_{CCwc}

(SUM OF MACROS I_{EE} + overhead I_{EE}) * 1.4 = I_{EEwc}

AMCC BIPOLAR ARRAYS OVERHEAD CURRENT DRAIN (mA)

AMCC
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V_{CC} = +5V, V_{EE} = -5.2V $V_{CC} = V_{EE}$
MAX = 1.4 * TYPICAL

CHIP	#TTL INPUTS	TTL MODE I_{CC},mA	ECL MODE I_{EE},mA	MIXED MODE I_{EE}/I_{CC},mA	+5V REF ECL/TTL I_{CC},mA
Q700	0	-	32	32/0	32
	1-10	39	-	32/13.5	45.5
	11-30	51	-	32/25.5	57.5
	31-40	63	-	32/37.5	69.5
	41-50	73	-	32/47.5	79.5
Q710	0	-	19	19/0	19
	1-10	27	-	19/12	31
	11-20	35	-	19/20	39
	21-30	41	-	19/26	45
	31-40	49	-	19/34	53
Q720	0	-	17	17/0	17
	1-10	24.5	-	17/12	29
	11-20	32.5	-	17/20	37
	21-30	38.5	-	17/26	43
	>30	46.5	-	17/34	51
Q1500	0	-	40	40/0	40
	1-10	47.5	-	40/12	52
	11-20	53.5	-	40/18	58
	21-30	62	-	40/26.5	66.5
	31-40	70	-	40/34.5	74.5
	41-50	78.5		40/43	83
QH1500	0	-	46	46/0	46
	1-20	61.5	-	46/24	70
	21-40	73.5	-	46/36	82
	41-60	90.5	-	46/53	99
	61-80	106.5	-	46/69	115
	81-100	123.5	-	46/86	132
	101-120	133.5	-	46/96	142
Q3500	0-120	50	83	83/11	92
Q2400	0-94	62	95	95/11	104
Q1300	0-76	42	75	75/11	84
QM1600	0-104	52	83	84/12	94

Q3500 revised 3/1/85

- WORST CASE VOLTAGE IS:

	MAXIMUM		
NOMINAL	COMMERCIAL	MILITARY	MIN
+5.0V	+5.05V	+5.5V	
-5.2V	-5.25V	-5.72V	
-4.5V	-4.6V	-4.8V*	-4.2V
		*N/A TO QH1500	

10. MULTIPLY THE WORST-CASE CURRENT WITH THE APPROPRIATE WORST-CASE VOLTAGE

$I_{EEwc} * V_{EEwc}$
$I_{CCwc} * V_{CCwc}$

11. SUM THESE TOGETHER

$$I_{EEwc} * V_{EEwc} + I_{CCwc} * V_{CCwc} = \text{POWER}$$

Next, ECL output power dissipation, if any, must be added. This is found from the termination values and computed as:

ECL STATIC POWER DISSIPATION = XXmA * 1.3V * number_of_ECL_outputs

where:

XXmA is the current, a function of the ECL output chosen:

TABLE 18
ECL OUTPUT CURRENT

200 ohm	3.4mA
100 ohm	6.8mA
50 ohm	13.5mA

If other ECL output load values are used, the actual current value must be computed for use in this equation.

EXERCISES:

1. GIVEN A Q700, 5 TTL INPUTS,
   SUM OF THE MACROS IS I_{EE} = 60.5
   SUM OF THE MACROS IS I_{CC} = 55.3

- FIND THE OVERHEAD CURRENT, COMPUTE THE POWER
  ASSUME +5V/-5.2V COMMERCIAL MIXED MODE CIRCUIT
  ASSUME NO ECL OUTPUTS

2. GIVEN A Q1500, 42 TTL INPUTS

SUM I_{EE} = 482.85 mA

SUM I_{CC} = 98.30 MA

- ASSUME +5V SINGLE POWER SUPPLY,
  MIXED TTL/ECL CIRCUIT
  13 ECL 50ohm OUTPUTS
  FIND THE OVERHEAD CURRENT, COMPUTE THE POWER

MAXIMUM CURRENT SPECIFICATION - INTERNAL CELLS

The Q700, Q1500 and Q3500 series arrays all provide either power (P) options or high-speed (H) options on many of their I/O and internal logic macros. These arrays have a maximum current specifictions for the internal matrix (L and B cell area).

MAXIMUM INTERNAL CURRENT SPECIFICATION

Array:	Maximum Current (mA)
Q700	-TBS-
Q720	-TBS-
Q710	-TBS-
Q1500S	600
QH1500S	630
Q3500A	788
Q2400A	612
QM1600A	~~TBS~~ 352
Q1300A	378

these need to be multiplied by 1.4

MAXIMUM CURRENT SPECIFICATION - BY ROW

If preplacement is being done external to AMCC, then the designer needs to be aware of the restrictions on macro placement. One of these is the maximum row current, derived from the maximum internal current on the previous page.

MAXIMUM INTERNAL CURRENT SPECIFICATION

Array:	Maximum Row Current (mA)
Q700	-TBS-
Q720	-TBS- } no limit
Q710	-TBS- no restrictions
Q1500A	30
	90 Rows 1, 16
QH1500A	30
	90 Rows 1, 17
Q3500S	36
Q2400S	36
QM1600S	-TBS-
Q1300S	-TBS- can be 100% H option

This is the basis of the 30% H/P option guideline given to designers.

QM1600S 160mA TYP for ½ of RAM