AMCC

APPLIED MICRO CIRCUITS CORPORATION

# AMCC Bipolar Array Design Submission

TEGAS V

AMCC LOGIC ARRAYS

DESIGN SUBMISSION
TEGAS V NETLIST

## SUBMITTING A LOGIC ARRAY DESIGN TO AMCC

The following document has been designed to insure you, the customer, of a successful transition from concept to finished part. It is a summary of the items required for the submission of an array design to AMCC, when the netlist and test vector generation have been performed. These items should be submitted to AMCC for use in the acceptance design review prior to committing the design to layout.

This list was prepared for those customers who design with TEGAS V.

These are the critical information transfer areas which, if not completed, could delay the acceptance of your circuit.

## AMCC ARRAY DESIGN SUBMISSION CHECKLIST (REQUIRED)

Attached to this document is the AMCC TEGAS DESIGN SUBMISSION CHECKLIST. It must be filled in and submitted with the design documentation.

The AMCC ERC software checks a large number of the possible design/schematic errors that can be made. There are a number of other checks that must be done by the customer prior to submission, including checks for test vector generation and submission.

For reference, the individual design guides contain a design rules and guidelines summary for the particular array series. A more detailed listing of the design rules and guidelines, including the requirements for test vector generation, is included in the AMCC DESIGN VALIDATION REVIEW document.

Where an ERC report satisfies the required check requested in the validation review it is indicated by [ERC]. When an ERC report does not satisfy the required check, the check must be made by the designer and is indicated by [MANUAL]. AMCC will re-run the ERC software against the submitted design to ensure that all current design rules are being checked.

The design submission checklist is a summary of the documentation produced on completion of the design validation review.

## MACRO LIBRARY VERSION

A macro library version must be submitted as part of the hardcopy documentation. The version number of your library will be on the label on the release media (currently on a VAX tape.).

## SCHEMATICS (REQUIRED)

When a design is complete, the schematics must be included in the design submission package. Schematics should be commented as to I/O mode (ECL, TTL, etc., for each input and output) and simultaneously switching outputs must be labeled.

Occurance names for macros must follow AMCC conventions and must be consistant with the TEAGS V netlist.

## SIMULTANEOUSLY SWITCHING OUTPUTS (REQUIRED)

Simultaneously switching outputs MUST be clearly identified and the designer must review the design to determine if the array requires additional $V_{CC}$ and GROUND pins.

## ERC FILES (REQUIRED)

The AMCC ERC software is available for TEGAS netlists. It runs the same ERC checks that are performed for EWS (DAISY, MENTOR, VALID) designs. AMCC will rerun the ERC software against all submitted designs as normal operating procedure. The documentation required from the customer is the documentation for those checks that must be performed manually.

## CRITICAL PATH SPECIFICATION (REQUIRED)

Maximum frequency of operation for the circuit required is related to the expected performance of the critical path(s) and should be clearly stated.

All paths that are critical in terms of timing margins (between calulated and specified delay) must be identified. The designer must supply the calculated worst-case timing for such critical path(s) and specify any additional performance or placement restrictions.

## PREPLACEMENT/PREROUTE REQUESTS (OPTIONAL)

Preplacement/preroute requests can be submitted to AMCC for critical paths in a circuit if necessary. Preplacement and preroute requests will be evaluated by AMCC and the designer will be notified if they can or cannot be met.

## PIN-OUT REQUESTS (OPTIONAL)

I/O placement may be of concern in a design and the designer may wish to specify a pin-out request to AMCC. Pin-out is driven by layout requirements and AMCC will notify the customer if the desired pin-out can or cannot be achieved.

## SUBMITTING FUNCTIONAL SIMULATION VECTORS (REQUIRED)

The size and complexity of circuits now requested make accurate and unambiguous simulation input and expected output pattern essential to the understanding and validation of the logic conversion of those circuits.

This data must be available at NRE design submission. It must be on machine readable media (tape) and a hardcopy listing must also be submitted to assure complete and correct data transfer.

Functional logic patterns are the time-independent sequential state description of the logic after any input change has propagated through and all outputs have fully settled to their stable states.

A complete functional pattern for all circuit input signals and all circuit output signals is the minimum simulation pattern required for logic verification and for generation of the test software for sorting actual parts.

Care must be taken to eliminate simultaneous changes of clock and data signals controlling flip/flops. In cases where the clock is generated by combinative gating of two (2) or more inputs, simultaneous changes of those signals is NOT allowed. This eliminates the possibility of false clocking due to logic race "glitches".

Logic patterns on inputs must contain only 1's and 0's; bidirectional inputs may have the high-Z state specified as applied while in input mode.

Non-Boolean or technology-dependent states are not allowed. Outputs must be Boolean 1 or 0, unless uninitialized.

Uninitialized outputs should be represented by a consistently chosen symbol (AMCC prefers X or U). Since the functional simulator represents the well-settled machine states, non-Boolean output levels (other than high-Z for three-state TTL outputs) are not allowed.

The pattern must initialize all internal nodes of the circuit as soon as possible. Circuits and test patterns requiring hundreds of sequential vectors to initialize are strongly discouraged. Initialization should be within 100 steps, and must be repeated at a minimum every 1000 steps or between each modular test, whichever is smallest.

Bidirectional I/O signals require some identification of their directional state at all times in the pattern. If this cannot be accomplished with a single unidirectional I/O signal (preferred), then an appropriately labeled internal or auxiliary signal must be specified.

The signal or states controlling the bidirectional signal(s) must be clearly defined. Two steps are required to change the direction of a bidirectional signal, one to change direction and one to send a signal.

All simulation input data must be organized in a "test pattern" (i.e., TESTPATT) format. This is a rectangular format with signals as the horizontal axis and regular sequential states (increasing time) as the vertical axis. The submitted file(s) should show expected output.

Signal names may be specified either as a separate order list or in totem pole format over their column of 1's and 0's.

Test patterns must be no longer than 4096 (4K) vectors (including the dummy vector required for each change of direction for any bidirectional signal). Longer patterns must be built in independently initializable segments of length less than or equal to 4K. Initialization at the 1K interval is required for any test.

## SUBMITTING "AT SPEED" SIMULATION REQUIREMENTS TO AMCC (REQUIRED)

All circuits must undergo "at speed" verification or exercise of the simulator model of the converted circuit. Any unique variation of the functional logic pattern, if required, must be provided.

Care must be taken to insure adequate set-up and hold between clock and data input vector transitions as well as any combinatorial logic that might produce race conditions between multiple input vectors.

If the "at speed" exercise can be accomplished by simply running the functional pattern at a faster vector rate, that rate must be specified.

The customer should be aware that the output states may not be well settled within the available vector period, and that the apparent "phase delay" of some outputs relative to others makes the evaluation of "at speed" simulation results a non-trivial exercise.

AMCC is prepared to assist the customer in interpreting and understanding the results of such simulation.

## REQUESTING HARDWARE TESTING (OPTIONAL)

There is no routine hardware at-speed testing.

For speeds up to 50MHz, an HP test can be arranged. For speeds up to 125MHz, simple path (4 input limit) testing can be arranged (bench test) and may require the customer to provide a mutually agreeable test fixture.

Final at-speed verification is the customer's responsibility.

## REQUESTING PROPAGATION DELAY TESTING (OPTIONAL)

Propagation path measurement can be arranged. For each path, the input and output must be specified, and the worst-case maximum propagation delay computed (see the appropriate design guide). The list of paths and their documentation must be supplied if this test is desired.

Note: propagation delay testing requirements are subject to the limitations of the standard AMCC testers.

## AMCC TEGAS DESIGN SUBMISSION CHECKLIST

PO # _____

DATE: _____

COMPANY NAME:_____

DESIGNER:_____ PHONE #:_____

AMCC ASSIGNED CIRCUIT NAME (IF KNOWN):_____

ARRAY:_____

MACRO LIBRARY VERSION/DATE:_____

STIMULUS INPUT CHANGE NAME:_____ NOM COM MIL

FILES ON TAPE MEDIA: see attached format instructions.

- [] TEGAS NET LIST
- [] TEGAS CHANGE FILE
- [] FUNCTIONAL SIMULATION SUBMISSION
  - [] EXPECTED OUTPUTS
- [] AT SPEED SIMULATION SUBMISSION

HARDCOPY ENCLOSURES:

REQUIRED:

- [] CIRCUIT FUNCTIONAL SPECIFICATION
- [] CIRCUIT BLOCK DIAGRAM
- [] CIRCUIT SCHEMATICS
- [] CRITICAL PATH SPECIFICATION
- [] ERC REPORTS
- [] SIMULTANEOUSLY SWITCHING OUTPUTS
- [] TEGAS NET LIST
- [] TEGAS CHANGE FILE
- [] SIMULATION OUTPUT FILE(S)
- [] FUNCTIONAL SPECIFICATION (CUSTOMER'S)
- [] updated NRE CHECKLIST

OPTIONAL:

- [] PIN-OUT REQUESTS
- [] PREPLACEMENT/PREROUTE REQUESTS
- [] TESTING DOCUMENTATION
- [] PROPAGATION DELAY TEST DOCUMENTATION

## AMCC Tape Format

The tape format that AMCC will accept for text files is as follows:

1. The tape must be an unlabelled, 9 track, 1600 bpi tape.

2. Each text file must correspond to a single tape file.

3. Each tape file must consist of ASCII characters.

4. Each tape file must meet the following requirements:
   a) One logical record contains 132 bytes.
   b) Each logical record contains only one line of text
   c) A physical record contains 50 logical records (ie. blocking factor = 50).
   d) All physical records must be 6600 (50 * 132) bytes long.

5. The first file must contain a list of file names. There is one file name per line and each file name can be no more than 8 characters. The first file name corresponds to the second file on the tape, the second file name corresponds to the third file, and so on.

6. Legible file names must be listed on an adhesive label affixed to the tape casing.

7. ~~The name~~ and phone number of person to contact in case of problems must also be on an adhesive label affixed to the tape casing.

8. Tapes not conforming to this specification cannot be processed.

AMCC
APPLIED MICRO CIRCUITS CORPORATION

# PACKAGING

CHAP 17 - PACKAGING BIPOLAR ARRAYS

# PACKAGING

1. **WHY PACKAGE**
   a. To protect the die
   b. To translate die function to the system

2. **VLSI LEAD COUNT**
   a. 24 -148 I/O today
   b. 200 and up tomorrow

3. **3 REASONS FOR GOOD PACKAGE SELECTION AT CHIP DESIGN**
   a. Fits customers'needs
   b. Eliminates "afterthought" packaging problems
   c. Makes ME's life easier

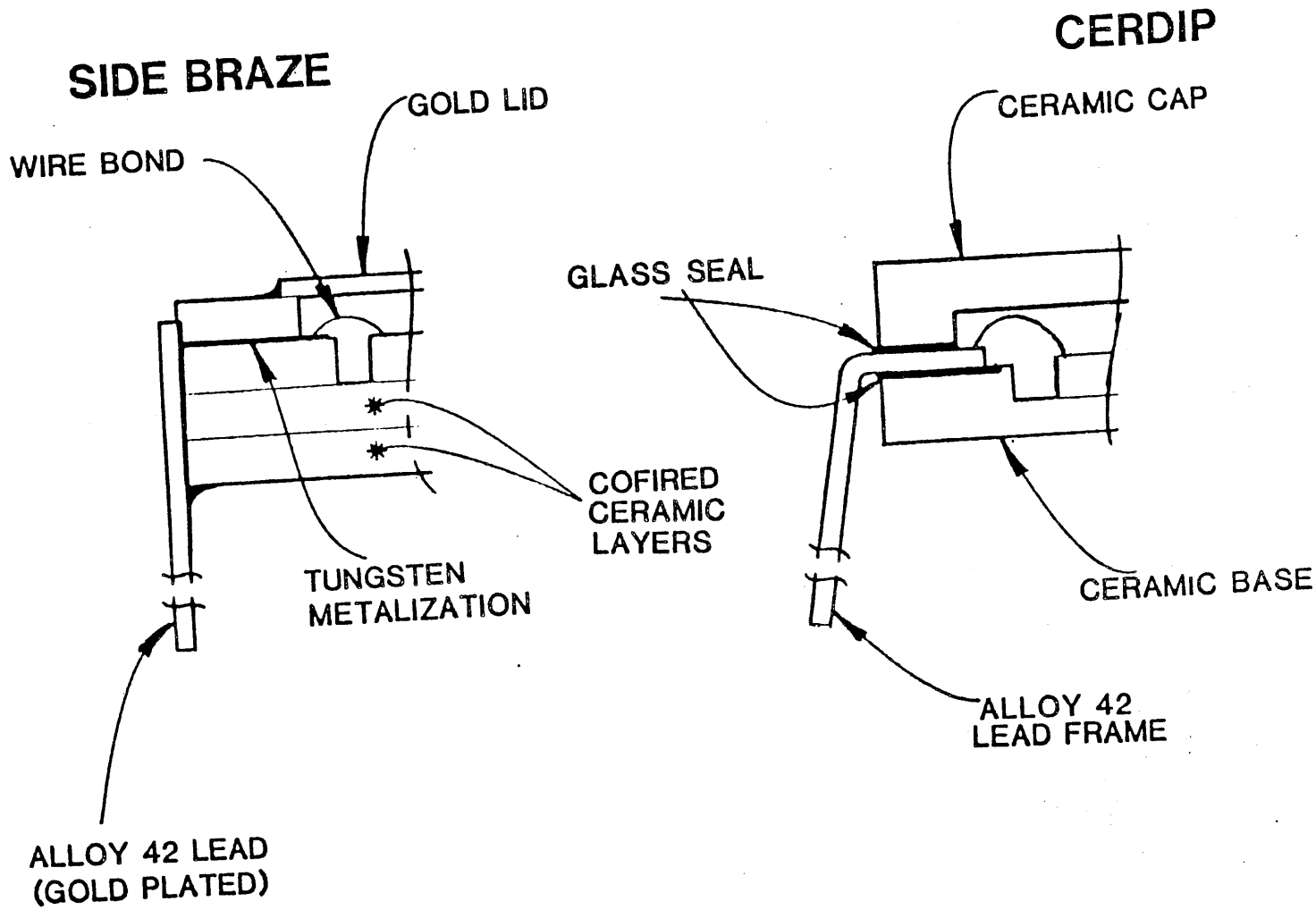
4. **AMCC "STANDARD" PACKAGES**
   a. Test hardware/ software available
   b. Assembly handling and shipping methods in place
   c. Packages qualified and characterized

## 5 CONSIDERATIONS FOR GOOD PACKAGE DESIGN

1. **MECHANICAL**-Form, Fit, and Function
   -Through Hole vs. Surface Mount board technology
   -Organic vs. Ceramic board material
   -Real Estate constraints (64 lead DIP vs. 68 LLCC)
      a. Chip Carriers
         1. "A" vs. "C" construction
         2. 84 LLCC "Combination B"
         3. Dynamic Thermal Management ( >28 LLCC -.450 per side): Solution - Leaded Chip Carriers of Flat Packs.
      b. Construction differences between Leaded Chip Carriers and Flat Packs.
2. **ELECTRICAL**-Resistance (R)
      a. Noise
   -Capacitance (C)
   -Inductance (L)
      a. "Cross-Talk" (leakage between signal lines)
   -In-house measurement lab now established
3. **THERMAL**-Tj< 150, lower the better (longer life)
      a. "Tj-Tc=Pd($\theta$jc)"- Military applications where Tc=125 C max.
      b."Tj-Ta=Pd($\theta$ja)"- Commercial applications where Ta=70-85 C max.
         1. $\theta$jc is a constant and can be mathematically modelled.

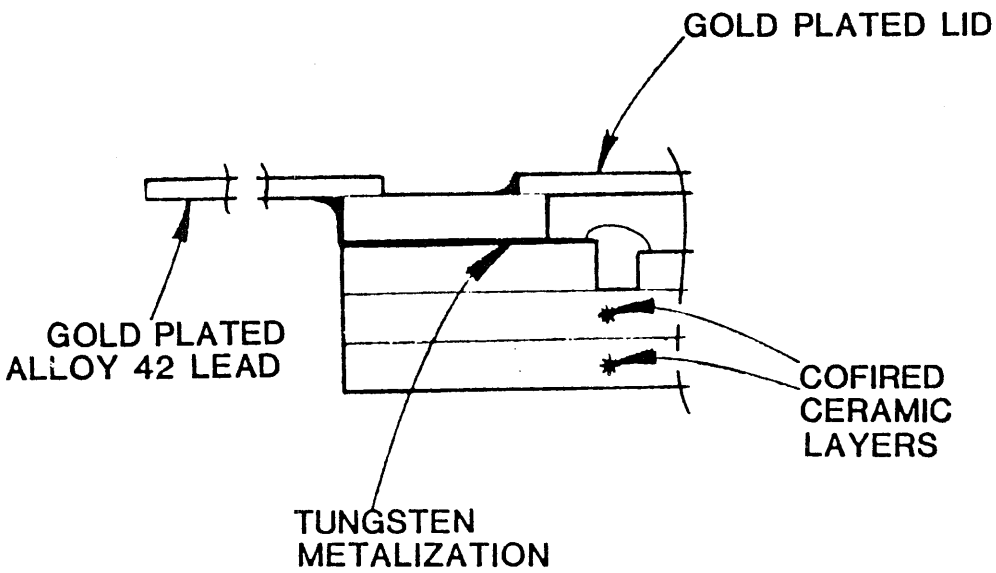
# PACKAGE CONSTRUCTION

(CROSS SECTION OF THICKNESS)

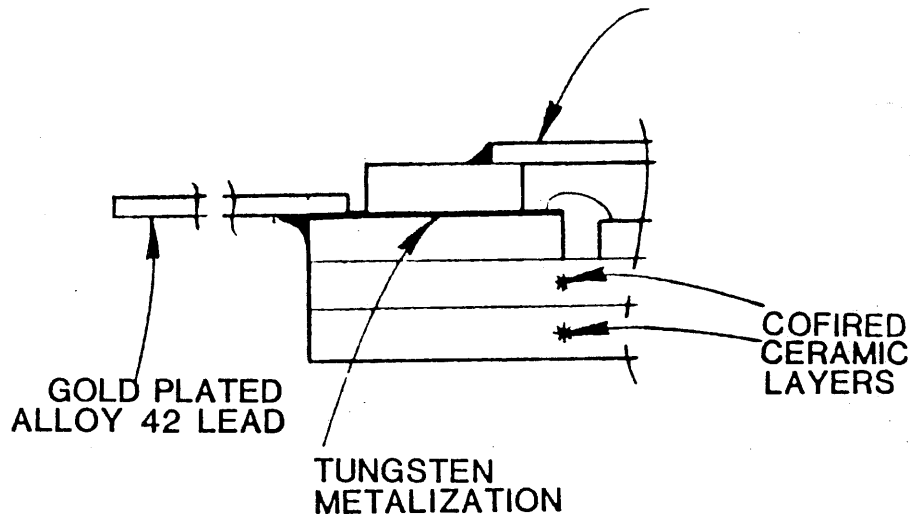


# PACKAGE CONSTRUCTION
(CROSS SECTION OF THICKNESS)

## LEADED CHIP CARRIER

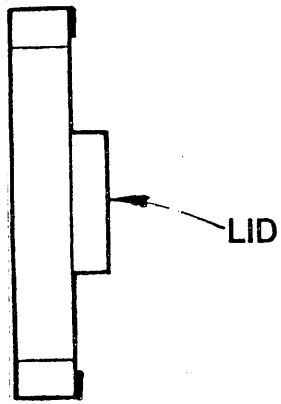


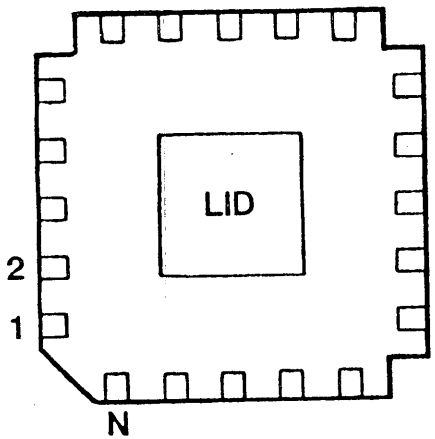

## FLATPACK



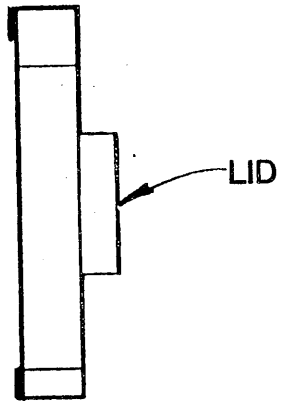
# PACKAGE CONSTRUCTION
(JEDEC STD OUTLINES)

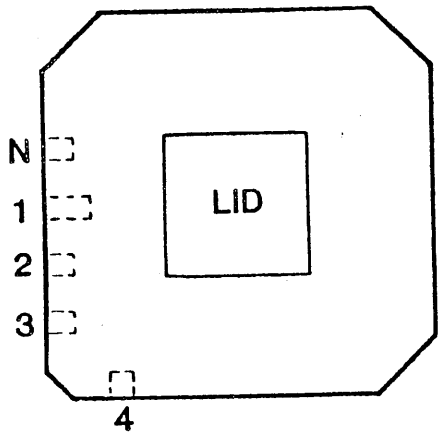
## JEDEC A



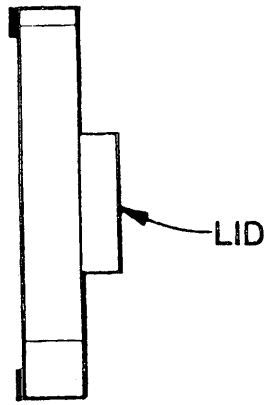



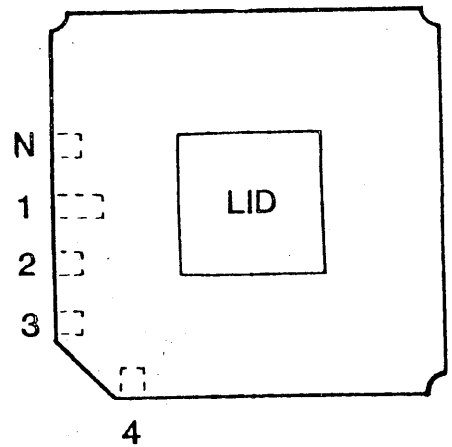

## JEDEC C




## JEDEC .040



## HEATSINKING

TWO MAJOR USAGES

- MILITARY (ZERO AIRFLOW SYSTEMS, ADDS MASS AND SPREADS HEAT (CONDUCTION)
- COMMERICAL AIRFLOW SYSTEMS INCREASES SURFACE AREA/VISIBILITY TO MOVING AIR (CONVECTION) "HEAT EXCHANGER"

TYPES OF HEATSINKS

- FLAT (HEATSPREADING, MINIMAL CONVECTION, FOR LIMITED BOARD SPACE APPLICATIONS)
- FINNED (DIRECTIONAL AIRFLOW)
- OMNIDIRECTIONAL (MULTIPURPOSE) "TOWER, PAGODA"

HEATSINK ATTACH

- THERMALLY CONDUCTIVE, ELECTRICAL INSULATING EPOXY (OVEN CURE).

2. $\theta$ja is different for every application and must be measured for accuracy (environment)

-Thermal Measurement Lab in place now.

4. **"-ILITIES"**-Reliability
   a. All AMCC ceramic packages are guaranteed to MIL-STD-883, method 5005.

-Testability/ Socketability
   a. Choose a package that is easy to socket/ test and has BI/ production sockets available.

-System Repairabilty

-Manufacturability
   a. Component/ board cost increases as the system becomes harder to manufacture.

5. **COST**-Plastic vs. Ceramic Power Dissipation < 1 Watt
   a. Pd<1 for plastic applications (CMOS)

-Cerdip, Cerlid vs. Solder Seal
   a. Cerdip is available up to 40 lead DIP only.
   b. As cost goes down, so does reliability
   c. AMCC recommends and uses solder seal only for highest reliability.

AMCC
APPLIED MICRO CIRCUITS CORPORATION

PROPRIETARY

18-1

AMCC
APPLIED MICRO CIRCUITS CORPORATION

# THE HIGH PERFORMANCE SEMICUSTOM LEADER

CHAP 18 - NEW AND FUTURE PRODUCTS
— handout —

PROPRIETARY