AMCC
APPLIED MICRO CIRCUITS CORPORATION

# Design Validation Review Bipolar Arrays

BIPOLAR

# DESIGN VALIDATION

The following is a listing of the design checks that must be made prior to submitting a design to AMCC for the final design review. A design validation review is required for all designs done with the aid of the DAISY, MENTOR, VALID, CAE, etc. or TEGAS V EWS systems.

The AMCC design validation software, also known as the ERC software, performs many of these checks and creates various output files that list the flagged errors and supply valuable design documentation. In many cases, the process of reviewing the ERC output files and redesigning to remove errors flagged will increase the probability of a buildable, testable, successful circuit. AMCC recommends that the designer review this list before starting a design.

On the following pages, [ ERC ] is used to indicate that a check is performed by the AMCC proprietary design validation software. [ FUTURE ERC ] is used for those checks that must be performed manually at present, but which will be automated within the next quarter.

Where an ERC check is not available (usually due to the design-dependence of the problem area), then the check cannot be programmed. The flag [ MANUAL ] is used to indicate when a check must be performed by the designer.

o ERC sofware is available for the DAISY engineering workstations. While it is currently executed on the VAX due to 8086 limitations on the LOGICIAN, it will soon be available on the DAISY 80286-based LOGICIAN.

o ERC software is available for the MENTOR and the VALID engineering workstations where it is system-resident.

o ERC software is available for TEGAS V netlist designs.

A special file called AGIF (AMCC Generic Interface File) is used to transfer a design from the EWS to the VAX for ERC support, test development (TEGAS), fault-grading and layout. This file is created by AMCC support software on the individual workstation and the EWS-VAX interface is unique to each workstation.

Reference: Internal array resources, cell utilization, pin count limits for routability, array I/O resources as listed in the design guide.

CELL COUNT

o CELL COUNT (POPULATION) MUST NOT EXCEED THE ARRAY LIMITS FOR ANY CELL TYPE
(I,O,I/O,L,B). [ ERC ]

o THE CELL UTILIZATION (L, B CELLS) MUST NOT EXCEED THE ARRAY LIMITS. [ ERC ]

INTERNAL PIN COUNT

o THE PIN COUNT (NUMBER OF INTERNAL PINS THAT MUST BE ROUTED) MUST NOT EXCEED THE LIMIT FOR THE ARRAY [ ERC ]

o COMPUTE THE ACTUAL OR ESTIMATE THE PIN COUNT - refer to the design guide if you are estimating the pin-count. Q700: the designer must temporarily add the threshold generator connections to the pin count generated by ERC.
[ ERC OR MANUAL CHECK ]

o BY EWS CONVENTION, UNUSED MACRO INPUT PINS ARE GROUNDED ON THE SCHEMATIC (THEY FLOAT IN REALITY) [ ERC ]

o BY EWS CONVENTION, UNUSED MACRO OUTPUT PINS ARE TERMINATED (DO NOT WIRE-OR THE TERMINATED OUTPUTS TOGETHER) [ ERC ]

Reference: Macro summary section of the appropriate design guide.

PIN RESTRICTIONS (ANY)

o ANY MACRO WITH AN ASTERISK HAS A PIN-RESTRICTION OR NOTATIONAL COMMENT IN THE DESIGN GUIDE - HAVE THESE BEEN HONORED? [ ERC ]

NAMING

o SEE THE AMCC SCHEMATIC RULES [ ERC ]

I/O PLACEMENT (CUSTOMER GENERATED) (OPTIONAL)

o HAS A PLACEMENT REQUEST BEEN SUBMITTED TO AMCC FOR APPROVAL?

BONDING DIAGRAM (OPTIONAL)

o HAS ONE BEEN COMPLETED AND SUBMITTED TO AMCC FOR APPROVAL?

MACRO CHECK (REQUIRED)

o WAS A MACRO LIST TURNED OVER TO AMCC? [ ERC ]

o ARE ALL OF THE MACROS USED IN THE DESIGN APPROVED BY AMCC, i.e., FROM AN OFFICIAL RELEASE OR PATCH? [ ERC AT AMCC AFTER DESIGN SUBMISSION ]

Reference: I/O interface sections of the appropriate design guide.

I/O

o THE I/O SIGNAL COUNT MUST NOT EXCEED THE LIMITS FOR THE ARRAY. [ ERC ]

o I/O SIGNAL, POWER AND GND COUNT MUST NOT EXCEED THE ENTIRE PACKAGE LIMIT. [ MANUAL CHECK ]

o TO IMPROVE NOISE MARGIN AND OPERATIONAL RELIABILITY, ADDITIONAL I, O OR I/O CELLS MUST BE USED AS $V_{CC}$ AND GROUND PADS UNDER CERTAIN CONDITIONS. HAS THE APPROPRIATE DESIGN GUIDE BEEN REFERENCED FOR THESE CONDITIONS? [ MANUAL CHECK ]

o EACH TTL OUTPUT MACRO WITH DIFFERENTIAL INPUTS MUST BE DRIVEN BY TRUE AND COMPLEMENT OUTPUTS COMING FROM THE SAME MACRO. ARE THEY? [ MANUAL CHECK ]

o ANY LOADING ON THESE DIFFERENTIAL LINES SHOULD BE BALANCED. IS IT? [ MANUAL CHECK ]

o DRIVING MACROS FOR THESE DIFFERENTIAL INPUTS SHOULD NOT HANDLE MORE THAN THREE ADDITIONAL LOADS. [ MANUAL CHECK ]

o Q700: TTL AND TTLMIX INPUT BUFFERS: ALL INPUTS MUST BE USED (NO INPUTS MAY BE GROUNDED) [ ERC ]

o DIFFERENTIAL ECL INPUT IS ACCOMPLISHED WITH TWO INPUT MACROS AND ONE DIFFERENTIAL BUFFER. HAS THE PROPER BUFFER BEEN USED?
[ MANUAL CHECK ]

o ECL 10K AND ECL 100K CANNOT APPEAR ON THE SAME ARRAY
[ ERC ]

o HAVE ALL I/O SIGNALS BEEN IDENTIFIED AS TO TYPE (ECL, TTL)?
[ MANUAL CHECK ]
ECL: SPECIFY TERMINATION (50ohm, 100ohm, 200ohm)
TTL: SPECIFY IF 3-STATE, OPEN-COLLECTOR, BIDIRECTIONAL

o DO THE MACROS SELECTED MATCH WHAT IS DOCUMENTED ABOVE?
[ MANUAL CHECK ]

Reference: Macro summary section of the appropriate design guide.

THRESHOLD GENERATORS

o USE THE CORRECT THRESHOLD GENERATORS WHERE APPLICABLE (VTA FOR THE BIXX MACROS, Q1500 AND Q3500 SERIES) [ ERC ]

o FOR THE Q700 SERIES, Q1500 SERIES, DO NOT EXCEED THE VTI LOADING WHEN USING TTL HIGH-SPEED INPUT MACROS [ ERC ]

o THRESHOLD GENERATOR PINS WHICH DO NOT APPEAR ON THE MACRO GRAPHIC SYMBOL ARE TO BE COUNTED IN THE ARRAY PIN COUNT FOR THE Q700 SERIES. AT PRESENT, REFER TO THE DESIGN GUIDE.
[ FUTURE ERC ]

ECL OUTPUT BUFFERS

o USE THE CORRECT DRIVE CAPABILITY FOR THE ECL OUTPUTS (50, 100, 200 OHMS) [ MANUAL CHECK ]

o DO NOT EXCEED THE ECL OUTPUT BUFFER LIMIT FOR THE I/O MODE AND ARRAY (Q700, Q1500 SERIES) - ECL OUTPUTS ARE LIMITED BY B CELLS AND PINS AVAILABLE [ MANUAL CHECK ]

Reference: Cell utilization, I/O interface sections of the appropriate design guide.

BUFFERS - GENERAL

o BUFFERS REQUIRED FOR INPUT (OR OUTPUT) MUST BE CONSIDERED WHEN MAKING A CELL COUNT. [ ERC ]

o CHECK THE MATCH OF THE TTL INPUTS AND THE TTL BUFFERS (PIN RESTRICTIONS) FOR THE Q700 SERIES IN PARTICULAR [ ERC ]

o MAKE CERTAIN THAT THE I/O MACROS DRIVE THE CORRECT BUFFER, AND THAT THE BUFFERS ARE DRIVEN BY THE CORRECT I/O MACROS [ ERC ]

Reference: Macro summary section of the appropriate design guide.

CIRCUIT I/O MODE

o USE A BORDER ON ALL SCHEMATICS [ ERC ]

o CHECK FOR MACRO COMPATIBILITY - ARE YOU MIXING TYPES (TTL, TTLMIX, ECL 10K, ECL 100K, +5V REF ECL) WHEN YOU ARE NOT SUPPOSED TO BE DOING SO? [ ERC ]

Reference: Fanout tables for maximum and derated loading on macros by option and classification; tpd+ and tpd- tables in the design guide section on computing propagation delay.

FANOUT

o OBSERVE FANOUT RULES FOR THE MACROS SELECTED [ ERC ]

o CLOCK AND OTHER DISTORTION/SPEED SENSITIVE PATHS WILL USE MACROS WITH 20% DERATED LOADING LIMITS [ MANUAL CHECK ] (REFER TO MACROCCUR TABLE GENERATED BY THE ERC PROGRAM)

Reference: Wire-OR tables for maximum wire-OR loading on macros by option and classification; tpd+ and tpd- tables in the design guide section on computing propagation delay.

WIRE-ORS

o WIRE-ORS MAY NOT HAVE MORE THAN 4 INPUTS - IF THEY DO, RE-DESIGN THEM. [ ERC ]

o NEVER CASCADE WIRE-ORS (FEED THE OUTPUT OF ONE INTO THE INPUT OF ANOTHER) [ ERC ]

o DO NOT WIRE-OR DRIVER MACROS (THREE-STATE ENABLE DRIVERS OR HIGH FANOUT DRIVERS) [ FUTURE ERC ]

o DO NOT WIRE-OR LATCH OUTPUTS UNLESS THEY ARE SPECIFICALLY ALLOWED [ ERC ]

o DO NOT WIRE-OR MACROS WHOSE FANOUT LOADING IS RESTRICTED TO 1 (SUCH AS UNBUFFERED INPUT MACROS, OUTPUT BUFFER MACROS) [ ERC ]

o DO NOT GROUND ANY WIRE-OR INPUT PINS (AND ALL INPUT PINS MUST BE USED) [ ERC ]

o USE COMPONENT WIRE-ORS. THEY INCLUDE tpd+ and tpd- PARAMETERS. MENTOR, VALID, TEGAS V ALSO SUPPORT PARAMETRIC WIRE-ORS. [ MANUAL CHECK ]

o DO NOT USE DAISY PARAMETRIC WIRE-ORS. (THEY DO NOT SUPPORT THE TIME PARAMETERS.) [ MANUAL ]

Reference: Macro summary section of the appropriate design guide.

THREE-STATE ENABLE - THREE-STATE ENABLE-DRIVER

o DRIVE THE THREE-STATE ENABLE PIN ON THREE-STATED MACROS BY A SPECIAL THREE STATE ENABLE DRIVER.

o USE ONE THREE-STATE ENABLE-DRIVER MACRO FOR LOADS UP TO 8 [ ERC ]

o USE MULTIPLE "INTERNALLY" SOURCED THREE-STATE ENABLE-DRIVER MACROS FOR HIGHER LOADS OR WHERE THE SIGNAL IS INTERNALLY GENERATED. [ ERC ]

o CAN INTERNALLY-GENERATED THREE-STATE ENABLES BE MONITORED DURING TEST? CAN THEY BE DISABLED AND THE ENABLE SIGNAL DRIVEN EXTERNALLY DURING TEST?

MASTER-SLAVE F/F - Q700

o USE THE SPECIAL CLOCK DRIVER (EF370, EF371 OR EF372) FOR THE MASTER-SLAVE FLIP/FLOP (EF720, EF730) ON A Q700 DESIGN [ ERC ]

o USE A COMMON CLOCK FOR THE MASTER AND SLAVE F/F IMPLEMENTATION LATCHES. [ MANUAL CHECK ]

Reference: Appropriate design guide.

CLOCK [ MANUAL CHECK ]

o MACRO SELECTION, MACRO PREPLACEMENT, AND PREROUTING OF WIRING IS DEPENDENT ON THE CRITICAL PATHS AND/OR THE MAXIMUM FREQUENCY REQUIREMENTS.

o ALL CRITICAL AND SENSITIVE PATHS IN A CIRCUIT MUST BE IDENTIFIED AND THE CRITICAL PATH(S) TIMING COMPUTED.

o CALCULATE THE CRITICAL PATHS UNDER WORST-CASE CONDITIONS, FOR BOTH RISING AND FALLING EDGE INPUT

o COMPUTE ASYMMETRICAL (RISING EDGE, FALLING EDGE) PROPAGATION

o DESIRED SET-UP AND HOLD TIMES MUST BE LISTED

o PERFORMANCE AT MAXIMUM FREQUENCY MUST BE LISTED.

o KEEP THE MAXIMUM CLOCK FREQUENCY WITHIN LIMITS FOR THE ARRAY AND I/O MODE

o INVERT THE MACRO OUTPUTS (SWITCH POLARITY OF THE SIGNAL) TO MINIMIZE PULSE SHAPING (PULSE STRETCH AND PULSE SHRINK) - BALANCE THIS AGAINST ASYMMETRICAL INPUT MACROS IN A TTL DESIGN

CLOCK (CONTINUED) [ MANUAL CHECK ]

o CHECK FOR RACE CONDITIONS IN THE DESIGN (USE DAISY DTA, DTV, TEGAS V OR OTHER SIMULATOR RUNNING AT SPEED WITH TIMING CHECKS ENABLED. AUGMENT WITH ADDITIONAL CALCULATIONS.)

o SIMULATE THE DESIGN FOR BOTH NORMAL AND WORST CASE CONDITIONS AND COMPARE THE RESULTS (THERE SHOULD BE A FUNCTIONAL MATCH)

o AVOID CLOCK SKEWING BY PRE-PLACEMENT AND BALANCED LOADING

o DERATE THE LOADING LIMITS ON ALL MACROS IN A CLOCK PATH

o SPECIAL REQUIREMENTS, SUCH AS UNUSUAL LOADING AND SIGNAL BALANCING MUST BE REQUESTED IN WRITING.

Reference: Section on power dissipation, maximum current specification in the appropriate design guide.

POWER CONSIDERATIONS

- o COMPUTE THE WORST-CASE POWER (ERC AND MANUAL EFFORT)

- o COMPUTE THE WORST CASE MAXIMUM CURRENT FOR THE INTERNAL ARRAY (L, B CELLS) [ FUTURE ERC ]
  - o DURING LAYOUT MAXIMUM ROW AND HALF-ROW CURRENT SPECIFICATIONS APPLY AND ARE CHECKED BY DESIGN RULES CHECKING SOFTWARE [ DRC ]

- o HAS THE MAXIMUM CURRENT BEEN EXCEEDED FOR THE INTERNAL PART OF THE ARRAY? [ FUTURE ERC ]
  - o UNUSED CELLS DRAW NO CURRENT
  - o THE FULL CURRENT IS DISSIPATED FOR A MACRO EVEN IF IT IS ONLY PARTIALLY USED
    - CURRENT SOURCE REDUCTION IS A CUSTOM OPERATION

TESTABILITY CHECKS [ MANUAL CHECK ]

o CAN ALL SEQUENTIAL CIRCUITS BE INITIALIZED? (100 STEPS MAX; PREFER FASTER SET-UP) USE RESET/SET LOGIC ELEMENTS WHENEVER POSSIBLE; LATCHES FOR TRANSPARENCY; ETC.

o ARE ANY COUNTERS > 8 BITS LONG? LIMIT COUNTER CHAINS TO 256 STEPS MAXIMUM OR BREAK THEM UP.

o ARE ANY UNUSED PADS/PINS AVAILABLE TO IMPROVE CONTROLLABILITY OR OBSERVABILITY? HAVE THESE BEEN USED FOR TEST POINTS?

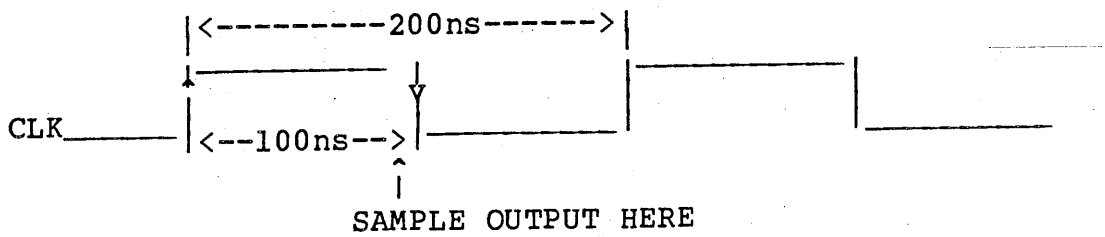
o HAS THE COMBINATIONAL LOGIC BEEN MINIMIZED TO REMOVE REDUNDANCY? (REDUCES FAULT MASKING IF CIRCUIT IS MINIMIZED)

o ARE INTERNAL SIGNALS NAMED FOR INCLUSION IN THE FORMAT FOR THE TEST FILE AS DESIRED?

SIMULATION VECTOR CHECKS [ MANUAL ]

FUNCTIONAL SIMULATION

o 100ns CLOCK EDGE IS THE MINIMUM. THE FAIRCHILD SENTRY TESTER IS USED WITH A MAXIMUM FREQUENCY OF 5MHz STEP THROUGH RATE.




o THE SIMULATION "PAGE" CANNOT EXCEED 4000 STEPS - CONCATENATED FROM SMALLER SIMULATION VECTOR SETS.

  o SENTRY TESTER MEMORY SIZE LIMIT

o EACH "PAGE" MUST BEGIN WITH INITIALIZATION

o EACH "PAGE" MUST CONTAIN INITIALIZATION EVERY 1000 STEPS, AT A MINIMUM

  o HP TESTER MEMORY SIZE LIMIT
    (FOR THE HP TESTER SHOULD DEBUG BE REQUIRED
    THE HP PAGE IS 1200 VECTORS)

o ALL INPUTS MUST BE SET TO "1" OR "0" ON THE FIRST TIME STEP (CLOCK = 0)
  (SET BIDIRECTIONALS TO HIGH-Z - THE TESTER CANNOT ACCEPT "X" - HIGH-Z MAY BE USED ON INPUTS)

o THE FIRST PAGE SHOULD BEGIN WITH A SIMULATION SEQUENCE THAT SWITCHES EACH INPUT AND EACH OUTPUT FROM 0-1 AND FROM 1-0. - THIS REQUIREMENT IS FROM TEST AND IS FOR CONNECTIVITY CHECKING PRIOR TO OPERATIONAL TESTING.

o UNINITIALIZED OUTPUTS SHOULD BE SHOWN AS "X" OR "U"; NON-BOOLEAN OUTPUTS (EXCEPT HIGH-Z FOR THREE-STATED OUTPUTS) ARE NOT ALLOWED.

o THE SIGNAL OR STATES CONTROLLING BIDIRECTIONAL SIGNALS MUST BE CLEARLY DEFINED - ARE THEY?

o BIDIRECTIONAL I/O IS TESTED WITH TWO STEPS TO ASSURE TIME TO ACHIEVE THE DIRECTIONAL SWITCH - TWO STEPS ARE REQUIRED TO CHANGE THE DIRECTION OF A BIDIRECTIONAL SIGNAL - ONE FOR DIRECTION, ONE FOR THE SIGNAL

o IF A THREE-STATE ENABLE SIGNAL IS GENERATED INTERNALLY, IT MUST BE NAMED AND LISTED IN THE DAISY FORMAT FILE (MENTOR, VALID, TEGAS FILES) SO THAT THE OUTPUT PORTION OF THE SIMULATION VECTORS SHOW THE PROPER STATE FOR THE ENABLE(S). IF IT IS DESIREABLE TO CONTROL THIS SIGNAL, APPROPRIATE DEGATING LOGIC AND INPUT MACROS MUST BE ADDED.

o FOR FILES WITH LONG SIMULATION SEQUENCES (IN EXCESS OF 1000 STEPS):

- THESE SHOULD BE PLACED AT THE END OF THE TEST FILE, IF POSSIBLE, TO ALLOW MODULAR BREAKDOWN OF THE TEST SET AND TO MINIMIZE POTENTIAL DEBUG PROBLEMS.

o HEAVY SWITCHING I/O

- SHOULD BE RUN AT THE END OF THE SIMULATION.

o HAVE SIMULTANEOUS CHANGES OF CLOCK AND DATA BEEN ELIMINATED?

o MULTIPLE-SIGNAL-GENERATED CLOCKS - HAVE SIMULATANEOUS CHANGES OF THESE SIGNALS BEEN ELIMINATED?

o HAS THE METHOD FOR THE SIMULATION FILE(S) GENERATION BEEN DOCUMENTED? (VIEW, RUN, START, ETC. FOR THE DAISY FOR EXAMPLE, COMPRABLE PROCEDURES FOR THE OTHER EWS SYSTEMS.)

o WAS THE PRINT_ON_CHANGE (DAISY) OR COMPRABLE OUTPUT FILE REQUESTED FOR EVERY SIMULATION RUN?

o WAS THE SAME FORMAT FILE USED FOR ALL SIMULATION VECTORS? (ALL VECTORS SHOW BIT 1 IS THE SAME SIGNAL, ETC.)

o WAS 100ns THE STEP AND DOES THE SAMPLE START AT 99ns (i.e., for DAISY, VIEW 999 1000) SO THAT THE SIMULATION VECTORS ARE PAIRED WITH THEIR EXPECTED OUTPUT? (THE BIT VECTORS ARE USED TO FORM STAND ALONE TEST PATTERNS)

o ARE THE FILES COMMENTED WITH COMPANY, DESIGNER, CIRCUIT NAME, DATE, AND A DESCRIPTION OF THE TESTING BEING PERFORMED? (STRUCTURED PROGRAMMING)

o ARE THE FILES ON AMCC-READABLE MEDIA?

AT SPEED SIMULATION REQUIREMENTS [ MANUAL CHECK ]

o HAS A SIMULATION BEEN PERFORMED "AT SPEED"?

o IS THE SCALING CORRECT FOR THE ARRAY?
(THERE ARE TWO SCALES IN USE; 1 = 0.1ns (1000 = 100ns) FOR THE Q700 AND Q1500 SERIES ARRAYS; 1 = 0.01ns (10000 = 100ns) FOR THE Q3500 SERIES ARRAYS)

o THE SAME RULES APPLY AS FOR FUNCTIONAL SIMULATION

The customer should be aware that the output states may not be well settled within the available vector period, and that the apparent "phase delay" of some outputs relative to others makes the evaluation of "at-speed" simulation results a non-trivial exercise.

AMCC is prepared to assist the customer in interpreting and understanding the results of such simulation.

OTHER TESTING (OPTIONAL) [ MANUAL CHECK ]

o ARE ADDITIONAL TESTS REQUIRED?

STANDARD AC TEST (PACKAGED PARTS ONLY)

o PROPAGATION DELAY ONLY, MEASURED FROM ONE INPUT TO ONE OUTPUT

o HAVE THE PATHS BEEN SPECIFIED?

o SIMULATION VECTORS MUST BE IN THE PROPER FORMAT FOR AMCC SIMULATOR AND THE "CARE" (AS OPPOSED TO "DON'T CARE") VECTORS MUST BE DEFINED

o VECTORS FOR EACH PATH MUST BE SELF-INITIALIZING (STAND-ALONE)

o LIMITED TO TEN PATHS (20 MEASUREMENTS) FOR ARRAYS WITH LESS THAN 2,000 EQUIVALENT GATES; TO 20 PATHS (40 MEASUREMENTS) FOR ARRAY WITH MORE THAN OR EQUAL TO 2,000 EQUIVALENT GATE DENSITY.

o FOR EACH PATH, HAS THE INPUT AND OUTPUT BEEN IDENTIFIED AND HAS THE EXPECTED WORST-CASE MAXIMUM PROPAGATION DELAY BEEN COMPUTED?

o PROPAGATION DELAY MEASUREMENTS REQUIRED: BACK-ANNOTATION PATH DELAYS MUST BE SUPPLIED (BY IMPLEMENTATION ENGINEERING AT PRESENT)

o TESTS ARE DONE AT MINIMUM AND MAXIMUM SUPPLY VOLTAGES

o STANDARD RESISTOR/CAPACITOR LOAD ONLY (REFERENCE SPECIFICATION TS154)

SPECIAL AC TEST (PACKAGED PARTS ONLY)

o ATE

o UP TO 20MHz RATE (STANDARD RATE IS 10MHz)

o $t_s/t_h$ TEST VECTOR REQUIREMENTS ARE THE SAME AS FOR DELAY TESTS

BENCH TESTS

o ARE BENCH TESTS REQUIRED? - THESE TESTS ARE CHARACTERIZATION ONLY

o CLOCK: $f_{max}$ OF UP TO 350MHz WITH A MAXIMUM OF FOUR (4) DYNAMIC SIGNALS AND A MAXIMUM OF FIVE (5) CRITICAL PATHS.

o MEASURE $t_r$, $t_f$

o MEASURE $t_w$ MINIMUM DOWN TO 2ns WITH THE SAME REQUIREMENT AS THE $f_{max}$ TESTS.

o BIASING CONDITIONS TO ESTABLISH CRITICAL PATHS MUST BE DEFINED

TEGAS5 PROGRAM RESTRICTIONS [ MANUAL ]

o NON-HIERARCHICAL MODULE NETLIST ONLY

o ALL STATEMENTS MUST END WITH A $

o SIGNAL NAMES MUST BE <= 7 CHARACTERS

o NO COLONS SHOULD APPEAR ANYWHERE IN THE PROGRAM

o NO BLANK LINES SHOULD APPEAR ANYWHERE IN THE PROGRAM

o COMMENTS ARE CREATED WITHIN DOUBLE QUOTES
"THIS IS A COMMENT"

o A DESCRIPTION SECTION MUST BE INCLUDED TO IDENTIFY THE DESIGNER AND THE DATE THAT THE PROGRAM WAS CREATED/MODIFIED, THE COMPANY NAME AND THE CIRCUIT NAME (AMCC REQUIREMENT)

o ANY STATEMENT IN THE DEFINE SECTION THAT IS NOT

```
GND = GRND $
```

MUST HAVE ALL SIGNALS EXPLICITLY CONNECTED TO PINS

```
B01(PO_560=Z,PO_32=ZN ) =
GT36(LOADN=A,PO_12=B,PO_13=GND) $
```

o THE EXCEPTION TO THE ABOVE, IF A PIN IS CONNECTED TO AN OUTPUT TERMINATOR, THEN THAT PIN AND ITS SIGNAL MUST BE OMITTED FROM THE STATEMENT

```
B01(PO_560=Z,PO_32=ZN ) =
GT36(LOADN=A,PO_13=GND) $
```

o IF OUTPUT SIGNALS ARE CONNECTED (WIRE-OR) THEN A WIREOR STATEMENT MUST REFLECT THIS CONDITION.

```
component(signal) = WIREOR#(signal=A,signal=B[,
                            signal=C,signal=D,
                               signal=E]) $

WO3(CALK=Z) = WIREOR4(SIG1=A,SIG2=B,SIG3=C,FRM=D) $
```

Reference: AMCC packaging guide

PACKAGE SELECTION

o REFER TO THE PACKAGING DOCUMENTATION FROM AMCC FOR THE LATEST SELECTION OF PACKAGES.

o VARIOUS STANDARD PACKAGES ARE AVAILABLE. SPECIAL PACKAGING NEEDS CAN BE EVALUATED ON REQUEST.

o CONTACT AMCC FOR PACKAGING DETAILS.

AMCC SUMMARY OF CONVENTIONS FOR SCHEMATICS

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- Use 4-6 Alphanumeric characters (A-Z, 0-9) for all macro names and for all wire names
- All macros must be named
- Do not use macro pin names as macro or wire names
- All names must be unique within a circuit
- All inter- and intra- page connections and all off-chip connections must be named - name the wire and NOT the connector
- All inter- and intra- page connections must be commented as to the pages to which they go to/come from
- All I/O macros must be commented as to type and use (ECL, TTL, TTLMIX, +5V ECL, simultaneously switching, etc.)
- All unused inputs are grounded (except AND inputs) - tie them to an inverter whose input is grounded
- Ground is a global name
- All unused outputs are terminated
- Terminators are not named
- All pages must be numbered, should be named for EWS
- WIREORx macros are named
- Follow AMCC naming conventions:

| | | |
|---|---|---|
| A____ | = | Adder |
| B____ | = | Buffer |
| G____ | = | Gate |
| EX___ | = | Exclusive or/nor |
| M____ | = | Mux |
| DE___ | = | Decoder |
| F____ | = | Flip flop |
| L____ | = | Latch |
| MM___ | = | Memory module |
| MI___ | = | MSI macro |
| SP___ | = | Special cell |
| LS___ | = | Inputs |
| D____ | = | Outputs |
| BD___ | = | Bidirectional I/O |
| W____ | = | Wireors |
| X____ | = | None of the above |

AMCC

APPLIED MICRO CIRCUITS CORPORATION

# AMCC Bipolar Array Design Submission

DAISY

**AMCC** reserves the right to make changes to any products herein to improve the reliability, function or design. **AMCC** does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.

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APPLIED MICRO CIRCUITS CORPORATION

AMCC BIPOLAR LOGIC ARRAYS

DESIGN SUBMISSION
DAISY LOGICIAN EWS

## SUBMITTING A BIPOLAR LOGIC ARRAY DESIGN TO AMCC

The following document has been designed to insure you, the customer, of a successful transition from concept to finished part. It is a summary of the items required for the submission of a bipolar array design to AMCC, when the schematic capture and test vector generation has been performed. These items should be submitted to AMCC for use in the acceptance design review prior to committing the design to layout.

This list was prepared for those customers who design with the DAISY engineering workstation (EWS).

These are the critical information transfer areas which, if not completed, could delay the acceptance of your circuit.

## AMCC BIPOLAR ARRAY DESIGN SUBMISSION CHECKLIST (REQUIRED)

The AMCC ERC software checks a large number of the possible design/schematic errors that can be made. There are a number of other checks that must be done by the customer prior to submission, including checks for test vector generation and submission. Attached to this document is the AMCC BIPOLAR ARRAY DESIGN SUBMISSION CHECKLIST. It must be filled in and submitted with the design documentation.

For reference, the individual design guides contain a design rules and guidelines summary for the particular array series. A more detailed listing of the design rules and guidelines, including the requirements for test vector generation, is included in the AMCC DESIGN VALIDATION REVIEW document.

Where an ERC report satisfies the required check requested in the validation review it is indicated by [ERC]. When an ERC report does not satisfy the required check, the check must be made by the designer and is indicated by [MANUAL]. AMCC will re-run the ERC software against the submitted design to ensure that all current design rules are being checked.

The design submission checklist is a summary of the documentation produced on completion of the design validation review.

## MACRO LIBRARY VERSION AND DATE OF CREATION

A macro library version and date of drawing creation must be submitted as part of the hardcopy documentation. The version number of your library will be on the label on the release media (currently either floppy or tape).

## DRAWING PAGES (REQUIRED)

When a design is complete, the n.DRAW files are to be copied to floppydisks. The final version of the drawings are to be submitted. Make two sets minimum, one for submission and one for your own vaulting.

## ERC FILES (REQUIRED)

The AMCC ERC software is not system resident on the DAISY LOGICIAN (8086 or 80286) at this time. The software is currently run on the VAX. Hardcopies of the ERC run for the final design must be submitted.

## CRITICAL PATH SPECIFICATION (REQUIRED)

Maximum frequency of operation for the circuit required is related to the expected performance of the critical path(s) and should be clearly stated.

All paths that are critical in terms of timing margins (between calulated and specified delay) must be identified. The designer must supply the calculated worst-case timing for such critical path(s) and specify any additional performance or placement restrictions.

## PREPLACEMENT/PREROUTE REQUESTS (OPTIONAL)

Preplacement/preroute requests can be submitted to AMCC for critical paths in a circuit if necessary. Preplacement and preroute requests will be evaluated by AMCC and the designer will be notified if they can or cannot be met.

## PIN-OUT REQUESTS (OPTIONAL)

I/O placement may be of concern in a design and the designer may wish to specify a pin-out request to AMCC. Pin-out is driven by layout requirements and AMCC will notify the customer if the desired pin-out can or cannot be achieved.

## SIMULTANEOUSLY SWITCHING OUTPUTS (REQUIRED)

Simultaneously switching outputs MUST be clearly identified and the designer must review the design to determine if the array requires additional TTL $V_{CC}$, TTL GROUND or ECL GROUND pins.

## SUBMITTING FUNCTIONAL TEST VECTORS (REQUIRED)

AMCC requires copies of EACH SOM control file (SOM_MCF.SING) and its related DATA or INPUT file (if any). Hardcopies of these files must be submitted in addition to the copies submitted on floppy disks. These files must be commented as to company name, designer, circuit name (AMCC generated name for your design) and the date AT A MINIMUM. Additional comments as to tests performed or other information which documents the circuit are also required.

The SOM control file must reference the accompanying data file. The SOM control file MUST contain a PRINT_ON_CHANGE outputs section and the signals monitored MUST include:

a. ALL INPUTS
b. ALL OUTPUTS
c. ALL INTERNAL THREE-STATE ENABLE CONTROL LINES

The data (or input) file must reference its SOM control file and it must also describe the tests being performed.

The FORMAT file used in the simulation(s) must be included in the media submission. **All test vectors must be generated using the same FORMAT file.** DAISY software does not currently permit a hardcopy output of the FORMAT file with its accompanying sections on MODE, ACQUIRE, etc. When it is possible to do so, this file must also be submitted as part of the hardcopy documentation.

## SIMULATION RESULTS

The simulation output file must be included in the submitted media documentation. A hardcopy of the simulation output is also required.

AMCC requires a copy of the PRINT_ON_CHANGE output file for each simulation. The AMCCSIMFMT output file is also required.

The SIFT file name must be supplied (to identify the array, and the designer's selection of NOMINAL, COMMERCIAL or MILITARY timing parameters).

Any %SUBMIT procedures written by the customer to run the simulation must be included on the floppy disk containing that simulation. If none were used, a log of the VIEW, RUN and other step commands must be submitted (i.e., all commands used during the simulation file creation).

## SUBMITTING "AT SPEED" TEST REQUIREMENTS TO AMCC (REQUIRED)

To verify that the array will operate at the required system dynamic frequency, a simulation of the array must be exercised at the required speed. This is currently a separate set of simulation vectors, with one line per clock change, scaled for actual time of change.

For example:

For the Q700, Q1500 on the DAISY LOGICIAN EWS, the simulation step is 0.1ns, so that a clock that changes at 10ns intervals has a vector at time = 0, 100, 200, 300, etc.

For the Q3500 series arrays on the same system, the scaling is different. The simulation step in this case is 0.01ns and the same clock, changing at 10ns intervals, would have a vector at time = 0, 1000, 2000, 3000, etc.

Scale the vectors according to the desired speed and the array involved.

The customer should be aware that the output states may not be well settled within the available vector period and that the apparent "phase delay" of some outputs relative to others makes the evaluation of "at speed" simulation results a non-trivial exercise.

AMCC is prepared to assist the customer in interpreting and understanding the results of such simulation.

## AT SPEED SIMULATION DOCUMENTATION

The same basic documentation procedures must be followed for at-speed simulation submission as for functional simulation submission. The SOM control file must be commented, the data file (if any) must be commented, the FORMAT file must be supplied, the SIFT file name must be supplied (preferably by a comment in the SOM control file). The SIFT file identifies the design as COMMERCIAL or MILITARY.

The SOM control file must reference the accompanying data file. The SOM control file MUST contain a PRINT_ON_CHANGE outputs section and the signals monitored MUST include:

a. ALL INPUTS

b. ALL OUTPUTS

c. ALL INTERNAL THREE-STATE ENABLE CONTROL LINES

The data (or input) file must reference its SOM control file and it must also describe the tests being performed.

The at-speed simulation is run under DLS. There is no restriction on the VIEW and RUN commands as there is for the functional test vector simulation. A log of those commands as run must be submitted. The same FORMAT file must be used for all at speed simulations.

AMCC requires a copy of the PRINT_ON_CHANGE output file for each at speed simulation. The AMCCSIMFMT output file is also required.

## AMCC AT SPEED PROCEDURE

AMCC will rerun the at speed simulation against the current DAISY library to verify operation.

## REQUESTING HARDWARE TESTING (OPTIONAL)

There is no routine hardware at-speed testing.

For speeds up to 50MHz, an HP test can be arranged. For speeds up to 125MHz, simple path (4 input limit) testing can be arranged (bench test).

Final at-speed verification is the customer's responsibility.

## REQUESTING PROPAGATION DELAY TESTING (OPTIONAL)

Propagation path measurement can be arranged. For each path, the input and output must be specified, and the worst-case maximum propagation delay computed (see the appropriate design guide). The list of paths and their documentation must be supplied if this test is desired.

Note: propagation delay testing requirements are subject to the limitations of the standard AMCC testers.

PO #:_____
DATE:_____

# AMCC DAISY DESIGN SUBMISSION CHECKLIST

COMPANY NAME:_____

AMCC ASSIGNED CIRCUIT NAME (IF KNOWN):_____

ARRAY:_____

MACRO LIBRARY VERSION/DATE:_____

SIFT FILE NAME:_____ NOM COM MIL

FILES ON FLOPPY DISK(S):

- [] DRAWING PAGES

- [] FUNCTIONAL TEST SUBMISSION:
  - [] SOM CONTROL FILE(S) WITH DATA INPUT FILE(S)
  - [] FORMAT FILE (ONLY ONE FOR ALL FUNCTIONAL TEST VECTORS)
  - [] SIMULATION OUTPUT FILE(S)
  - [] PRINT_ON_CHANGE OUTPUT FILE(S)
  - [] %SUBMIT PROCEDURES
    OR
  - [] LOG OF SIMULATION RUN(S)

- [] AC TEST SUBMISSION:
  - [] SOM CONTROL FILE(S) WITH DATA INPUT FILE(S)
  - [] FORMAT FILE (ONLY ONE FOR ALL AT-SPEED TEST VECTORS)
  - [] SIMULATION OUTPUT FILE(S)
  - [] PRINT_ON_CHANGE OUTPUT FILE(S)
  - [] %SUBMIT PROCEDURES
    OR
  - [] LOG OF SIMULATION RUN(S)

HARDCOPY ENCLOSURES:

REQUIRED:
- [] ERC REPORTS
- [] CRITICAL PATH SPECIFICATION
- [] SIMULTANEOUSLY SWITCHING OUTPUTS
- [] SIMULATION OUTPUT FILE(S)

- [] DESIGN VALIDATION REVIEW HAS BEEN COMPLETED AND SUPPORTING DOCUMENTATION ENCLOSED
- [] updated NRE CHECKLIST

OPTIONAL:
- [] PIN-OUT REQUESTS
- [] PREPLACEMENT/PREROUTE REQUESTS
- [] HARDWARE TESTING DOCUMENTATION
- [] PROPAGATION DELAY TEST DOCUMENTATION