AMCC
APPLIED MICRO CIRCUITS CORPORATION

January 15, 1989

Dear AMCC Customer:

Enclosed you will find the latest (812) software library release of AMCC's BiCMOS Q14000 Series. In addition to updated macros, we've added new low power I/O macros including 8 mA TTL output drivers. Please disregard previous 807 version of your Q14000 Design Manual and replace it with the enclosed update documentation.

There are written directions for software installation with your update packet. Should you have any questions or need help, please feel free to contact any of AMCC's applications engineers at (619) 450-9333.

Thank you for your support.

Sincerely,

Allyn Pon
Product & CAD Marketing Manager

AP:

Enclosures

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Volume I
Q14000 Series

BiCMOS Logic Arrays

Applied MicroCircuits Corporation

Q14000
BiCMOS Series
Design Manual

Includes: Q2100B, Q9100B
BiCMOS Logic Arrays

The material in this document
supercedes all previous
documentation issued for the
Q14000 BiCMOS Series Logic Arrays

M1401-0388

Section 1:

Introduction

INTRODUCTION

This design manual provides a summary of the AMCC (Applied Micro Circuits Corporation) Q14000 Series BiCMOS Logic Arrays. Volume 1 is composed of the following sections:

- Section 1: Introduction
- Section 2: Design Methodology
- Section 3: Timing Analysis
- Section 4: External t_{su}, t_h
- Section 5: Power/Packaging
- Section 6: Macro Library Documentation
  - Section 6-1: TTL Interface
  - Section 6-2: TTLMIX Interface
  - Section 6-3: ECL Interface
  - Section 6-4: Internal Logic Macros
  - Section 6-5: MSI Macros
  - Section 6-6: Special Macros
- Section 7: Quicksheets
- Section 8: Index

It also includes information on:

- Product features
- Performance specifications
- Design Interface and support

and contains a listing of the macros currently available. The AMCC Packaging Brochure should also be referenced for further information on packaging.

The Q14000 Series supports the following arrays:

TABLE 1-1
SUPPORTED ARRAYS

Q14000B	sea-of-cells
Q9100B	channelled array
Q6000B	sea-of-cells
Q2100B	channelled array

Volume 1 of this design manual is intended as a self-contained design aid to allow the proper selection of an array for a particular design, to indicate the packaging available for that array, and to provide the designer with a better understanding of the capabilities of the Q14000 Series BiCMOS Logic Arrays.

Section 2 contains design rules specific to this array series. Interconnect rules and testing requirements are included in this section.

The macro summary and detailed macro specifications are presented in reference manual format in Section 6 with a rapid graphic reference provided via quicksheets in Section 7. Either a macro-conversion of an existing design, or the direct design of a circuit can be implemented using the available macros.

Volume 2 of this design manual is composed of the following sections:

- Section 1: Introduction
- Section 2: EWS-Specific Design Methodology
- Section 3: EWS Schematic Rules and Conventions
- Section 4: Vector Submission Rules and Guidelines
- Section 5: Design Validation
- Section 6: Design Submission
- Section 7: MacroMatrix Installation
- Section 8: MacroMatrix User's Guide
- Section 9: AMCC Glossary
- Section 10: Index

Volume 2, Section 2 of this design manual contains the Engineering-workstation (EWS) design methodology, covering both the EWS-specific operations and the AMCC MacroMatrix support software.

Section 8 contains the MacroMatrix User's Guide which details the Engineering Rules Check (AMCCERC, e.k.a., ERC) software checks and error messages and probable causes. It also includes the Vector Rules Check (AMCCVRC) user's guide. Section 9 contains the MacroMatrix Installation and Operations manual, which summarizes the EWS-specific commands required for operation of the AMCC support software.

The Design Validation document in Section 5 details the engineering rules checks that must be reviewed prior to design submission. It is the basic outline of the design review AMCC performs prior to circuit acceptance. Fill in or check off items as indicated and submit the entire document as part of the design submission package. Additional copies can be obtained from AMCC.

The Design Submission Document in Section 6 is to be completed and submitted along with the design submission package. Additional copies can be obtained from AMCC.

The following trademarks are recognized by AMCC throughout this dasign manual:

- LASAR Version 6 - Teradyne
- LOGICIAN - Daisy Systems Corp.
- GATEMASTER - Daisy Systems Corp.
- Mentor Graphics
- MacroMatrix - AMCC
- Valid Logic

Q14000 SERIES DESCRIPTION

The AMCC Q14000 Series Logic Arrays provide an optimized systems approach to BiCMOS semi-custom applications. CMOS logic for low power is combined with bipolar drivers for high drive capability within each internal cell. Mixed-mode I/O is combined with an advanced, interactive CAD system-based design approach to provide a quick and cost-effective solution to discrete IC replacement. Manufacturing advantages gained from the use of the AMCC logic arrays include:

- Increased circuit density
- Increased system speed
- Reduced power
- Higher reliability
- Lower system cost
- Operation over both military and commercial temperature rangas

The AMCC Q14000 Series Logic Arrays Macro Library is supported on the Daisy, Mentor Graphics and Valid Logic EWS. The designer can usa any of these systems in conjunction with AMCC's MacroMatrix software package to perform schematic capture, Engineering Rules Checking (AMCCERC), simulation, automatic test pattern formatting (AMCCSIMFMT), AMCC Vector Rules Checking (AMCCVRC), Front-Annotation and Back-Annotation (AMCCANN). Simulation, AMCCERC error checking, AMCCVRC rules checking, Front-Annotation and Back-Annotation are also supported on VAX/VMS systems with LASAR 6.

The Q14000 Series arrays are BiCMOS arrays. They have the ability to externally interface to either Schottky TTL, ECL 10K or ECL 100K. ECL 10K or ECL 100K may be standard-reference or +5V reference ECL.

As an added feature, the Q14000 Series provides the ability to mix ECL 10K, CMOS and TTL or ECL 100K, CMOS and TTL on the same array. ECL 10K and ECL 100K outputs are also allowed on the same array, regardless of the ECL type used for input. For other combinations, please contact AMCC Marketing.

All of the interface options are realized through the choice of appropriate macros, and personalized with the metal masks only.

AMCC describas the density of its logic arrays in terms of equivalent gates (2-input NAND gates), which are a function of the density of the availabla macros and the number of cells available in any given array. The density of the Q14000 Series is described below.

TABLE 1-2
ARRAY DENSITY

Array	Equivalent Gates
Q14000B	13440
Q9100B	9072
Q6000B	5760
Q2100B	2160

The arrays in the Q14000 Series share a common macro function library which contains a wide selection of fully characterized logic functions varying from SSI to MSI densities. The higher functionality macros have correspondingly higher equivalent gate densities.

Examples of the basic logic functions include simple and complex gates, EXOR-nets, latches, decoders, MUXs, 4-bit counters, a 4-bit universal register, buffered input, high-speed ECL input, buffered and unbuffered output and ECL output macros which contain logic, buffers and output translation.

AMCC logic arrays are structured to allow the components spread across several cells to be interconnected into a single high-functionality MSI macro. These hard-wired MSI macros guarantee consistent and predetermined circuit performance. AMCC recommends that designers use the higher functionality MSI macros whenever possible.

Many interface macros in the Q14000 Series macro library have high-speed (H) options in addition to the standard (S) option of the macro. Several macros have low-power (L) options. These macro options allow a designer to selectively program critical I/O paths with high-speed operation while implementing the remainder of the I/O in lower power standard-option macros.

The AMCC BiCMOS Series arrays provide a higher performance I/O capability than do CMOS and other BiCMOS arrays. The AMCC BiCMOS Series arrays provide a bipolar drive capability on the macro outputs that drive internal nets. Intrinsic gate delays, when critical paths are implemented on pure CMOS arrays, can be 2-20 times longer.

The AMCC BiCMOS Serias arrays are similar to the AMCC Bipolar Series arrays in that the extrinsic dalay (fan-out and metal loading delay) accounts for a small portion of the overall path dalay. This reducas post-routing problems and allows a much higher performance to ba achieved.

TYPICAL APPLICATIONS

Typical applications include high-speed computers, graphics, communications, test aquipment and instrumentation. Designed to operate in the full MIL-SPEC temperature and voltage ranga, the Q14000 Series also has applications in radar, EW, avionics, guidance, flight simulation and other military systems.

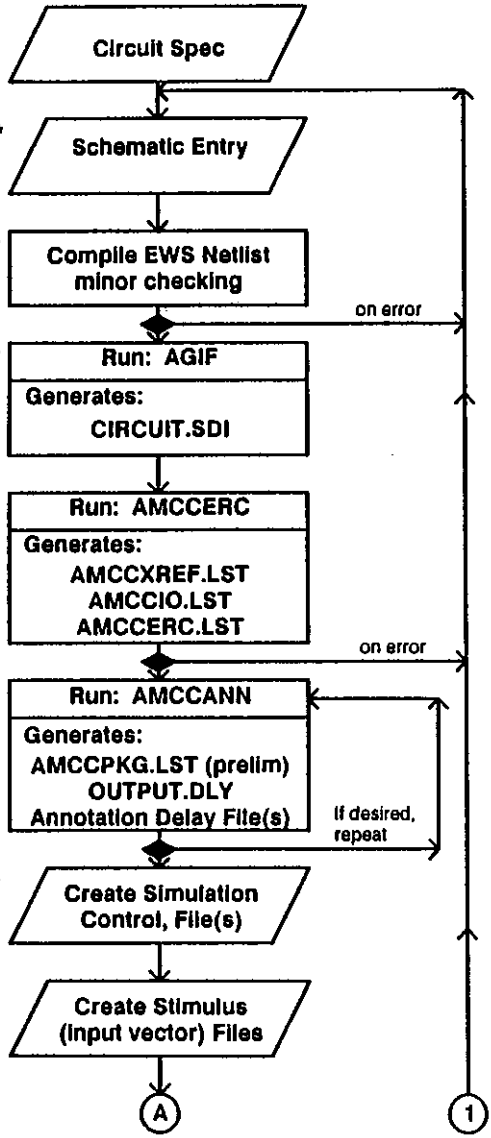
FEATURES

A summary of the features of the Q14000 Serles includes:

- 13440, 9072, 5760 and 2160 equivalent gate versions
- 1.5-micron Bipolar/CMOS technology - N-type epitaxial for both NPN oxide-isolated bipolar and CMOS
- 3-layer metal for sea-of-cells arrays (Q14000B/Q6000B)
- 2-layer metal to customize base array (all arrays)
- 100% autoplace and autoroute with up to 95% logic cell utilization

- System-level multiple-cell MSI macros
- Schottky TTL, low-power Schottky TTL, CMOS, ECL 10K and ECL 100K I/O compatibility
- Standard-reference ECL or +5V referenced ECL
- Speed/power programmable I/O macros
- On-chip translators for mixed mode interface
- Both ECL 10K and ECL 100K outputs may appear on the same array (placement restrictions apply)
- Lower overall worst-case multipliers than with CMOS
- Fast on-off chip delays
- Low fan-out degradation
- High internal noise immunity
- Unused cells do not dissipate power
- Internal core uses no DC current despite bipolar drivers
- Multiple power supply options available
- Full MIL operating renge (−55°C ambient to +125°C case, ± 10% power supply)
- Wide selection of packaging
- Supported on engineering workstations:
    - Daisy
    - Valid Logic
    - Mentor Graphics
- Supported on LASAR 6
- Full CAD support, including post-autoroute, worst-case timing enelysis

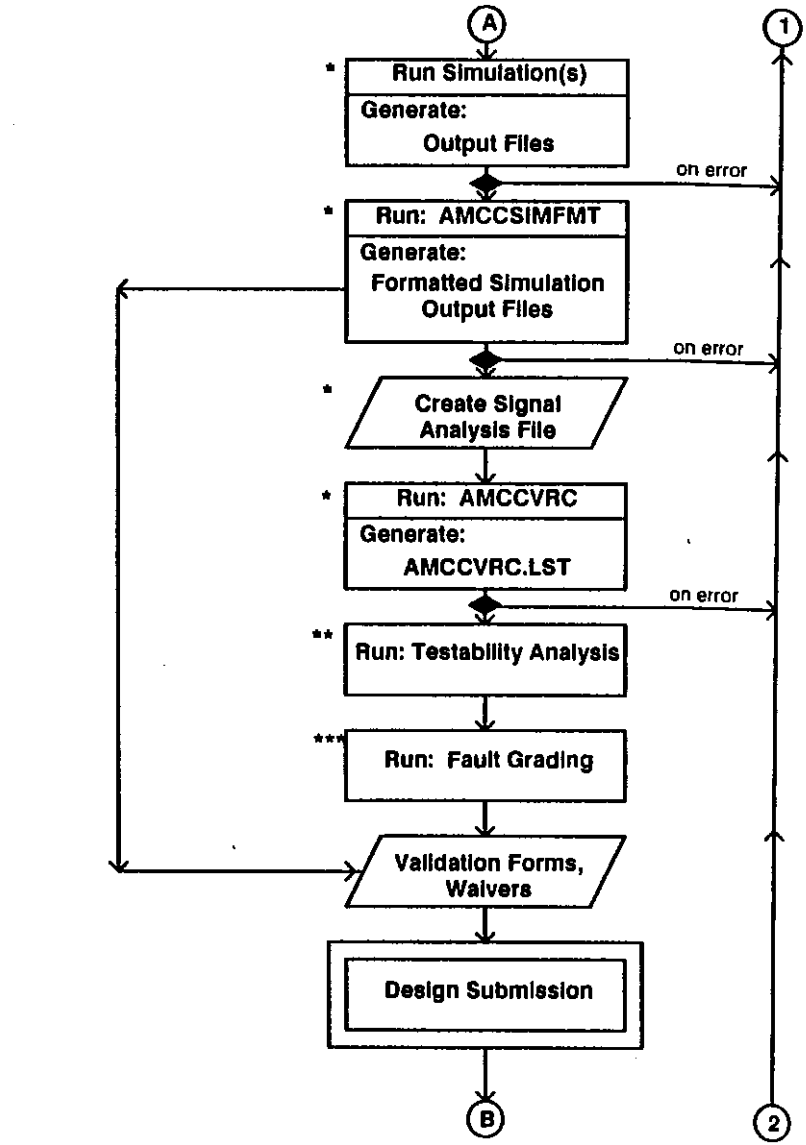
EWS DESIGN FLOW



*AMCC can be contracted to perform these steps.

Figure 1-1

EWS DESIGN FLOW (Continued)



* AMCC can be contracted to perform these steps.
** AMCC does not support this function at this time.
*** LASAR 6 only.

Figure 1-1

EWS DESIGN FLOW (Continued)

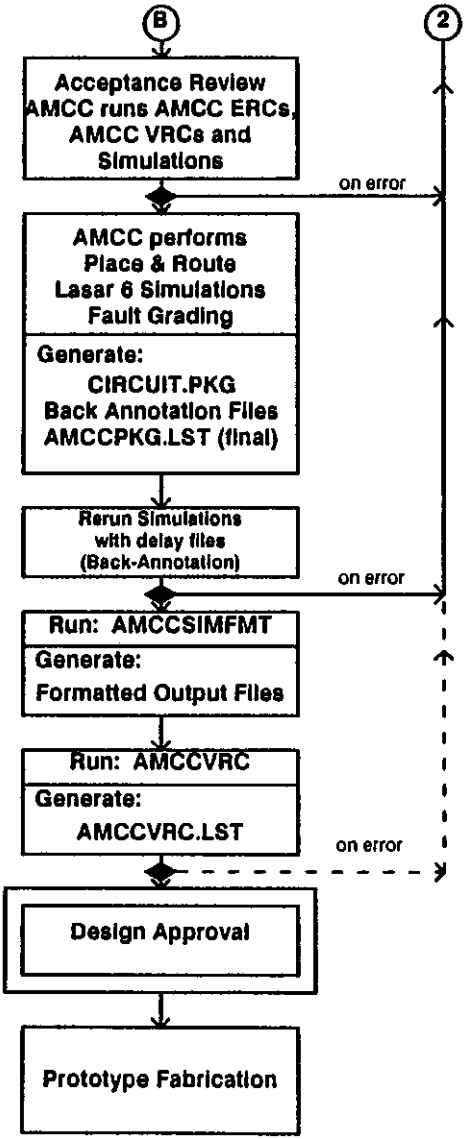


Figure 1-1

Section 2:

Design Methodology

Table of Contents 2-2

DEVICE ARCHITECTURE

The AMCC logic arrays are formed from e customer specified design added to an AMCC pre-processed silicon base array. The base array for the Q14000 Series BiCMOS arrays is composed of two types of cells, I/O and Basic cells. Each cell consists of a number of uncommitted transistors and resistors.

The basic cell layout of the arrays is demonstrated with the Q9100B, shown in Figure 2-1. Table 2-1 summarizes the cell resources and Table 2-2 summarizes the power-ground resources for the Q14000 logic array series.

Q9100B and Q2100B arrays are channeled arrays fabricated with double layer metal BiCMOS technology. Q14000B and Q6000B arrays are channel-less "sea-of-cell" arrays fabricated with triple- layer metal BiCMOS technology. In both cases, inter-cell routing takes place on two metal layers.

MACRO CONFIGURATION

A customer design is described via schematics using the macros contained in the released library for the array serias. Macros are individually configured in an array by interconnecting the components within a cell with the first layer metal to form the customer-selected macro functions. Macro placement is performed automatically by the AMCC proprietary CAD software.

Q14000B ARRAY LAYOUT
Industry's First Sea-of-Cells Architecture

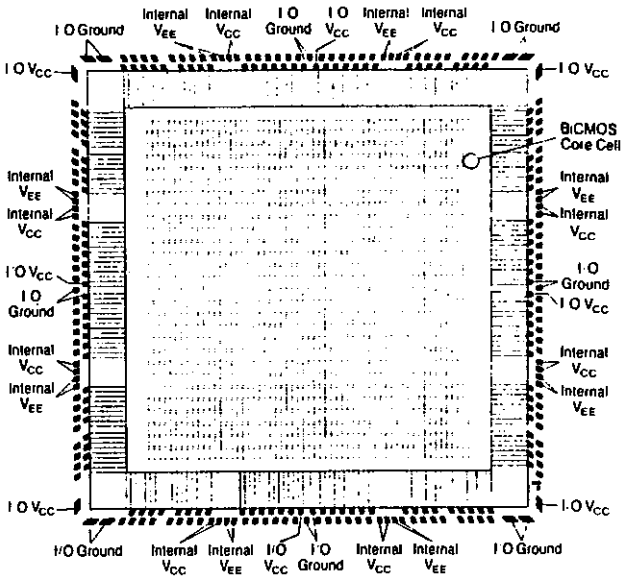


Figure 2-1a

TABLE 2-1
Q14000 SERIES CELL RESOURCE SUMMARY

Cell Type:	Quantity: Q14000B	Q9100B	Q6000B	Q2100B
Logic (Basic) cell	3360	2268	1440	540
Interface (I/O) cell	226**	160	132	80
Bidirectional I/O cell	-	40*	-	20*
Fixed power/ground pads	58	56	50	28
Total Array Pads:	282	216	182	108

* Single-cell bidirectional limit. Refer to "TTL Bidirectional Macros" and "ECL Bidirectional Macros".

** Because of tester limitations, only 224 of the 226 I/O pads can be used as signal I/O pads prior to July, 1989. Added power and grounds are not considered to be I/O signals.

TABLE 2-2
Q14000 SERIES POWER AND GROUND RESOURCES

MODE	DESCRIPTION	Q14000B	Q9100B	Q6000B	Q2100B
TTL	V_{CC} (+5V)	32	32	26	16
SYSTEM	GROUND	24	24	24	12
ANY ECL	V_{CC} **	40	40	34	20
SYSTEM	V_{EE} *	16	16	16	8
MIXED	V_{CC} (+5VDC NOM)	8	8	4	4
TTLMIX	V_{EE} *	16	16	16	8
and ECL	TTL GROUND	8	8	8	4
SYSTEM	ECL V_{CC} **	24	24	22	12
MIXED					
+5V	V_{CC} (+5VDC NOM)	32	32	26	16
SYSTEM	GROUND	24	24	24	12

* V_{EE} is –5.2V FOR STD-REF ECL 10K
–4.5V FOR STD-REF ECL 100K
0V FOR +5V REF ECL 10K OR ECL 100K

** V_{CC} is 0V FOR STD-REF ECL 10K
0V FOR STD-REF ECL 100K
+5V FOR +5V REF ECL 10K OR ECL 100K

INTERCONNECTIONS AND ROUTING

Interconnections between macros (routing) on the Q9100B and Q2100B arrays use both the first and second layers of metal, following specific routing tracks. Routing is done on the second and third layers of metal for the Q14000B and Q6000B arrays. Routing is performed automatically by AMCC proprietary CAD software.

To allow for a high logic cell utilization and an optimum layout for high-speed logic designs, a liberal allocation of first metal horizontal routing tracks and second matal vertical routing tracks have been incorporated into the architecture for the Q9100B and Q2100B arrays. For the Q14000B and Q6000B, these are sacond metal vertical and third metal horizontal tracks.

Additionally, the **AMCC CAD** software has been designed to automatically transform a logic design implemented in AMCC macros into an efficient high performance layout design. If there are sensitive timing and/or skew constraints, AMCC can optionally offer preplacement of the macros implementing these critical areas.

The customization of the array is performad by adding the 2-layer metal interconnect, representing the macros and their interconnaction, to the base array.

BASIC CELLS

The internal logic cells, called Basic cells, utilize both CMOS and bipolar devices. The internal logic is performed in CMOS while the bipolar device pairs provide necessary drive capability.

The Basic cells are organized to support high-level logic functions such as latches, multiplexors, decoders, etc. Simple and complex gates can also be made from these cells.

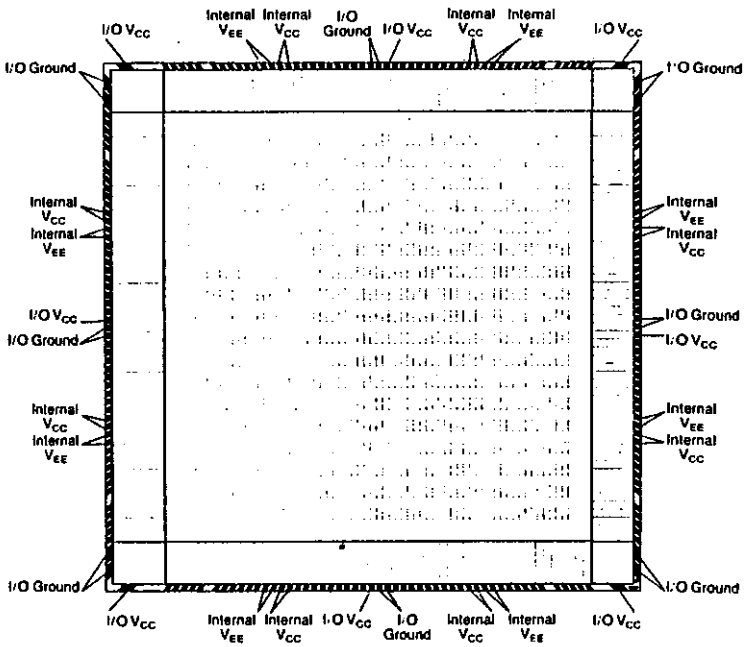
I/O CELLS

The interface to the arrays is accomplished in the mostly bipolar input/output cells on the Q14000 Series Logic Arrays. The I/O cells are located around the perimeter of the array. For all arrays, ECL- and TTL-translators and most of the required buffers are included in the I/O cells for external interfacing to both ECL and TTL. Each individual I/O cell is configurable to be either TTL, ECL 10K or ECL 100K.

On the Q9100B and Q2100B arrays, only certain I/O cells can support a single-cell bidirectional macro. These are on the left side of the arrays, across two quadrants. The Q9100B and Q2100B are limited to 40 and 20 single-cell bidirectional macros respectively.

No I/O cells on the Q14000B and Q6000B arrays will support single-cell bidirectional macros.

Q9100B DIE LAYOUT



Single cell bidirectionals can only be placed in the following cells. Other interface macros may use these I/O cells.

163 - 173

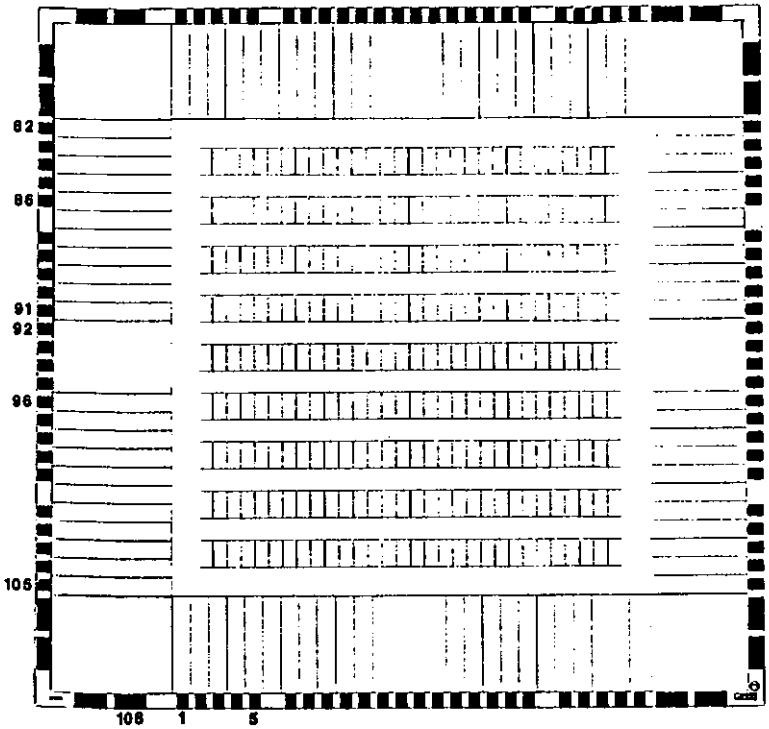
178 - 186

190 - 198

203 - 213

Figure 2-1b

Q2100B DIE LAYOUT



Single cell bidirectionals can only be placed in the following cells. Other interface macros may use these I/O cells.

82 - 91

96 - 105

Figure 2-1c

OVERHEAD CIRCUITRY

In addition to the cells, each array contains overhead circuitry: bias generators, voltage references and voltage regulators. Overhead circuitry is predefined by AMCC for the Q9100B and Q2100B. For the Q1400B and Q6000B arrays, the number of voltage generators used (VRB and VTA10K or VTA100K) will depend on final placement.

INTERFACE OPTIONS

The array itself can be configured to be 100% TTL, 100% ECL 10K, 100% ECL 100K, TTL/ECL 10K or TTL/ECL 100K, with either dual power supplies or a single +5V supply available for either the 100% ECL or mixed mode I/O circuits. (See Table 2-3.) In addition, both ECL 10K and ECL 100K outputs may be used on any given array. Only one type of ECL is allowed for input.

TABLE 2-3
POWER SUPPLY OPTIONS*

	SINGLE POWER SUPPLY			DUAL POWER SUPPLY	
	+5V	-5.2V	-4.5V	+5V/-5.2V	+5V/-4.5V
100% TTL	o	-	-	-	-
100% ECL 10K	o	o	o	-	-
100% ECL 100K	o	o	o	-	-
ECL 10K/TTL	o	-	-	o	o
ECL 100K/TTL	o	-	-	o	o

* ECL 10K can be operated at ECL 100K voltages and visa versa

INTERFACE GUIDELINES

A summary of the interface guidelines for the four I/O modes of operation are shown in Figure 2-2. Most of the I/O macros for the Q14000 Series include buffer functions, to simplify I/O selection. The designer should review the I/O options to determine where these options would enhance the circuit efficiency.

MACRO SUMMARY

Refer to the macro summary and index (Section 6) for a list of the macros available for the Q14000 Series Logic Arrays. The library and its summary sheets are for use during macro conversion or when creating a new design directly from the available functions. If other macro functions are desired, please consult AMCC.

The macro summary in Section 6 is divided into six segments: TTL Interface, TTLMIX Interface, ECL Interface, Basic Logic Macros, MSI Macros and Special macros. The macros are in alphabetical order within those sections.

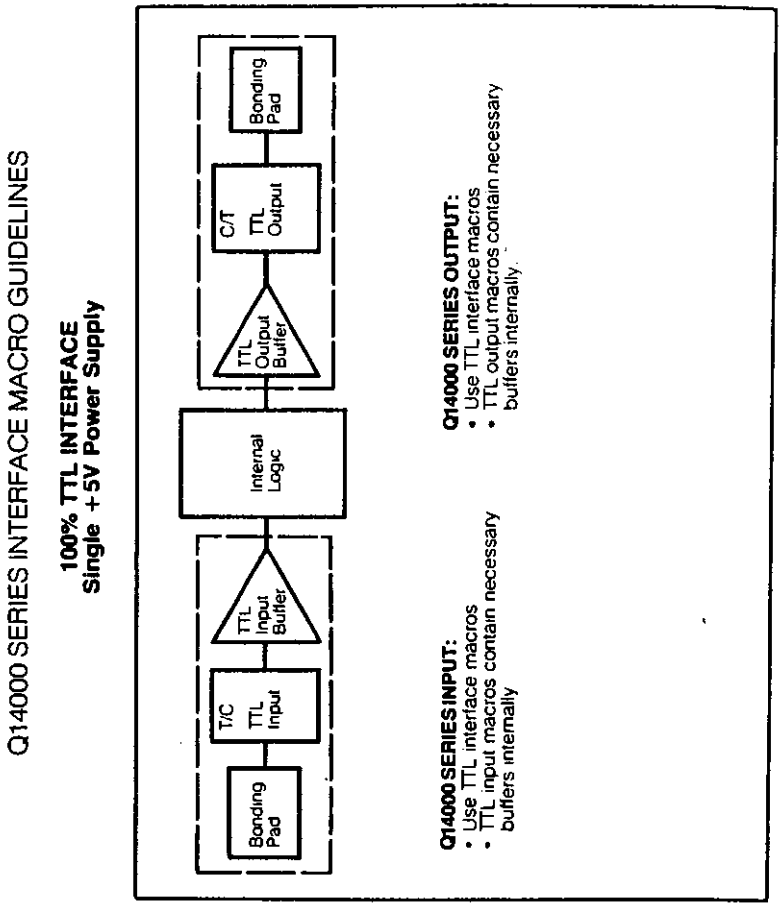
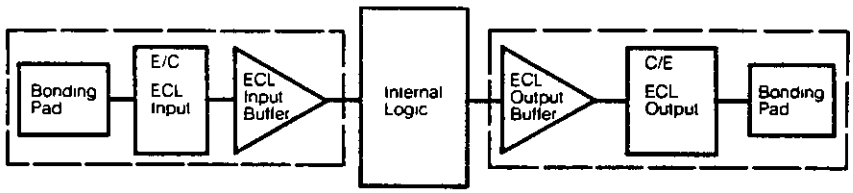

Q14000 SERIES INTERFACE MACRO GUIDELINES
100% TTL INTERFACE
Single +5V Power Supply
Bonding Pad
T/C TTL Input
TTL Input Buffer
Internal Logic
TTL Output Buffer
C/T TTL Output
Bonding Pad
Q14000 SERIES INPUT:
• Use TTL interface macros
• TTL input macros contain necessary buffers internally
Q14000 SERIES OUTPUT:
• Use TTL interface macros
• TTL output macros contain necessary buffers internally.

Figure 2-2a

Q14000 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

100% ECL INTERFACE
Single −5.2V, −4.5V
or +5V Power Supply



Q14000 SERIES INPUT:
- Use ECL interface macros (IExx)
- ECL input macros contain necessary buffer internally.
- Same macro for either +5V, −5.2V or −5.4V supply

Q14000 SERIES OUTPUT:
- Use ECL interface macros
- ECL available in 50 ohm terminations only
- ECL output macros contain necessary buffers internally
- Supports both ECL 10K (OExx) and ECL 100K (OKxx)
- Same macro for either +5V, −5.2V or −4.5V supply
- No limit on number of 50 ohm outputs

Figure 2-2b

Q14000 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

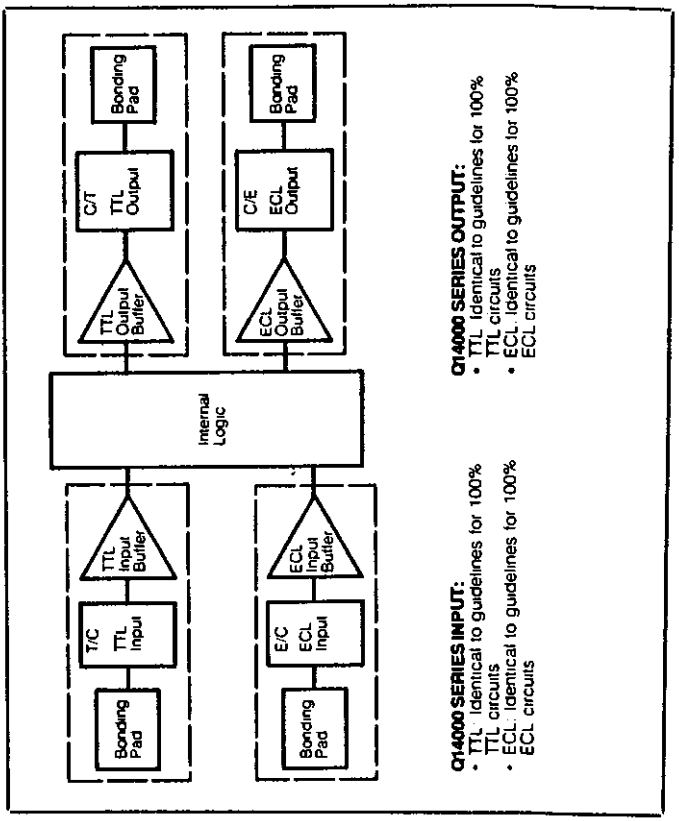


Figure 2-2c

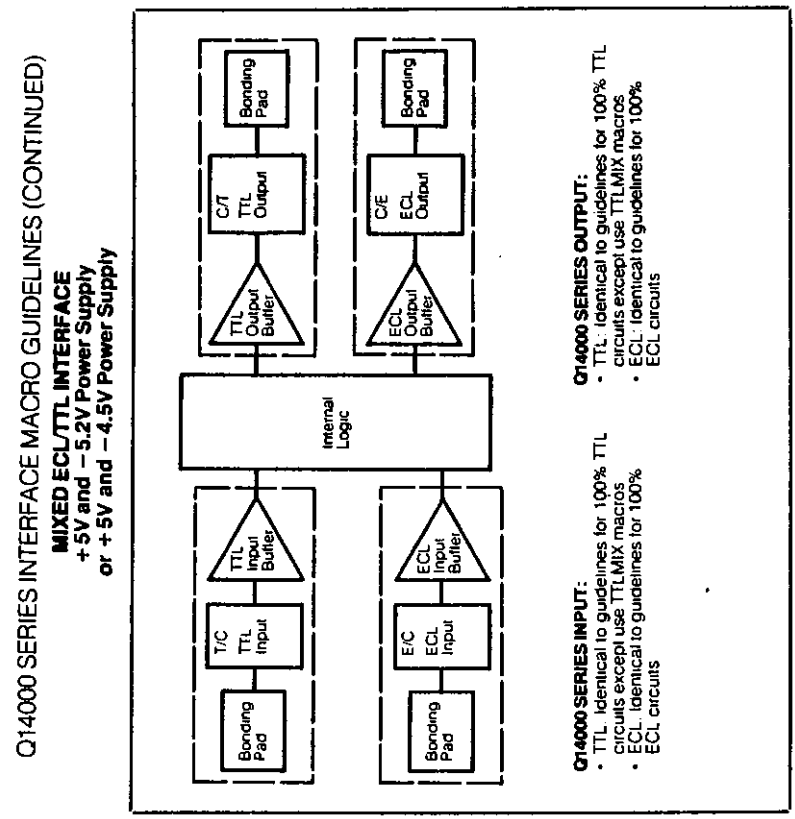

Q14000 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)
MIXED ECL/TTL INTERFACE
+5V and −5.2V Power Supply
or +5V and −4.5V Power Supply
Bonding Pad
T/C TTL Input
TTL Input Buffer
E/C ECL Input
ECL Input Buffer
Internal Logic
TTL Output Buffer
C/T TTL Output
ECL Output Buffer
C/E ECL Output
Q14000 SERIES INPUT:
• TTL: Identical to guidelines for 100% TTL circuits except use TTLMIX macros
• ECL: Identical to guidelines for 100% ECL circuits
Q14000 SERIES OUTPUT:
• TTL: Identical to guidelines for 100% TTL circuits except use TTLMIX macros
• ECL: Identical to guidelines for 100% ECL circuits

Figure 2-2d

I/O MACROS

Interface macros are documented in Sections 6-1, 6-2 and 6-3. All signals going on or off the chip require the use of an appropriate interface macro.

TABLE 2-4
I/O MACRO DOCUMENTATION INDEX

Section	Interface Macro Type
6-1	TTL for 100% TTL TTL for ECL/TTL with +5V
6-2	TTL for ECL/TTL, dual power supplies
6-3	ECL, any

For +5V only circuits, the TTL macros are selected from the TTL section, Section 6-1. For dual power supply circuits, the TTL macros are selected from the TTLMIX section, Section 6-2. The ECL macros are selected from the ECL section, Section 6-3. The same ECL macros are available for use with standard reference voltage or for +5V reference voltage circuits.

TTL INPUT (ITxx macros)

Q14000 Series TTL input macros contain input buffers. TTL level detection is performed in this input macro. For circuits with a single +5V power supply, the buffer provides the signal buffering required to drive internal circuits. For dual power supply circuits, the buffer also provides signal translation from TTL input levels to tha internal CMOS signal level needed by the array, which operates between ground and the negative power supply.

TTL OUTPUT (OTxx macros)

The Q14000 Series arrays provide 20mA current sink, 1mA current source capability. The TTL output is differentially driven by the buffered logic that is part of the TTL output macro.

The Q14000 Series arrays handle TTL totem-pole, open-collector and 3-stated output options. The 3-state output macro enable pin may be driven by any internal-level logic signal (the output of an input or internal logic macro). The signal driving the enable pin must be named on the schematic and must be listed in the simulation signal format.

BIDIRECTIONAL TTL (UTxx macros)

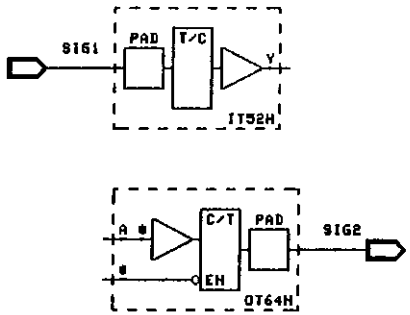
The I/O cell for the Q9100B and Q2100B arrays supports bidirectional I/O. The input and output functions follow the same design methodology as the ITxx and OTxx macros. The bidirectional macro enable pin may be driven by any internal- level logic signal (the output of an input or internal logic macro). The signal driving the enable must be named on the schematic and must be listed in the simulation signal format.

Bidirectional macros are placed in specifically designed I/O cells, limited to 20 on the Q2100B and 40 on the Q9100B arrays.

For the Q14000B and Q6000B arrays, a bidirectional I/O macro requires two I/O cells.

When a bidirectional TTL macro is required, either for the Q14000B or Q6000B arrays or when the number of single-cell bidirectionals on the Q9100B or Q2100B arrays are inadequate, use one input macro and one 3-stated output macro (TTL) combined and tied together outside of the package.

For example, use IT12 with OT24 or IT52H with OT64H (Q9100B/Q2100B examples). See Figure 2-3.



FOR BIDIRECTIONALS BEYOND THE RESTRICTED UT27, UT67
USE ONE INPUT AND ONE OUTPUT (3-STATE) MACRO

STRAP TOGETHER OUTSIDE THE PACKAGE

IF AN INTERNAL STRAP IS REQUIRED (LESS PACKAGE PINS)
CONSULT AMCC FOR A CUSTOM PATCH

THIS APPROACH REQUIRES A PAR

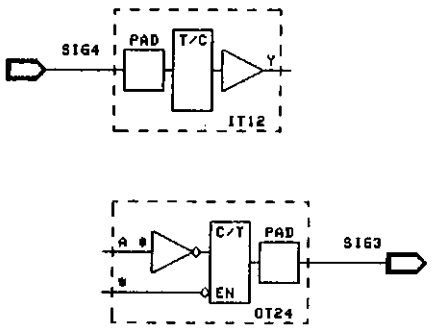


Figure 2-3

ECL INPUT (IExx macros)

ECL input macros contain an RC compensation network and an input buffer. ECL inputs function in the same manner on circuits which have +5V referenced ECL input with a single +5V power supply.

ECL OUTPUT (OExx, OKxx macros)

All ECL outputs require a buffer, and the buffer is included in the output macro. The Q14000 Series ECL output buffers drive 50 ohm ECL outputs. If an output is designad for a different termination, it is referenced in the macro documentation. ECL output macros are grouped by logic function in Section 6. A specific version of the macro (OExx or OKxx) is selected based on ECL type.

TABLE 2-5
ECL MACRO SELECTION

Q14000 Series	ECL 10K		ECL 100K	
	+5V REF	GND REF	+5V REF	GND REF
INPUTS	IExx	IExx	IExx	IExx
OUTPUTS	OExx	OExx	OKxx	OKxx
Bi-direc.	UExx	UExx	UKxx	UKxx

BIDIRECTIONAL ECL (UExx, UKxx macros)

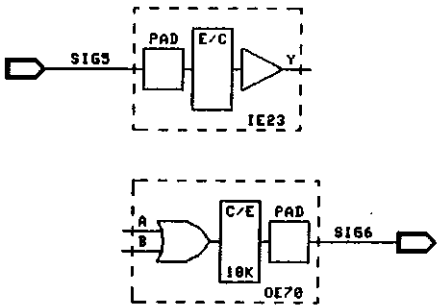
The Q9100B and Q2100B array I/O cells support bidirectional ECL I/O. The input and output functions follow the same design methodology as the IExx and OExx/OKxx macros. The macro enable pin may be driven by any internal-level logic signal (the output of an input or internal logic macro). The signal driving the enable pin must be named on the schematic and must be listed in the simulation signal format.

Bidirectional macros are placed in specifically designed I/O cells, limited to 20 on the Q2100B and 40 on the Q9100B arrays.

For the Q14000B and Q6000B arrays, a bidirectional I/O macro requires two I/O cells.

When a bidirectional ECL macro is required, use one input macro and one output macro combined and tied together outside of the package.

For example, use the IE23 with the OE70 (Q9100B/Q2100B example). See Figure 2-4.



FOR ECL, ONE METHOD IS A WIRE-OR NET
AGAIN, TIE TOGETHER OUTSIDE THE PACKAGE

Figure 2-4

+5V REFERENCED ECL/TTL

AMCC offers the option of having ECL 10K or ECL 100K available with the use of a single +5V power supply. The ECL logic threshold levels are shifted, but retain their high-speed characteristics. This +5V referenced ECL mode allows the partitioning of a high-speed TTL design into multiple AMCC devices using a single +5V supply, while providing high-speed ECL I/O between the arrays on the same PC board and full system TTL compatibility.

ALTERNATIVE ECL TERMINATIONS

The standard ECL termination is 50 ohms tied to V_{TT}, where V_{TT} = -2.0V for standard reference ECL. An alternative termination is 80ohms to ground with 130 ohms to V_{EE} where V_{EE} = -5.2V. For other termination configurations, consult AMCC.

CHARACTERIZING THE ARRAY - THE CHIP MACROS

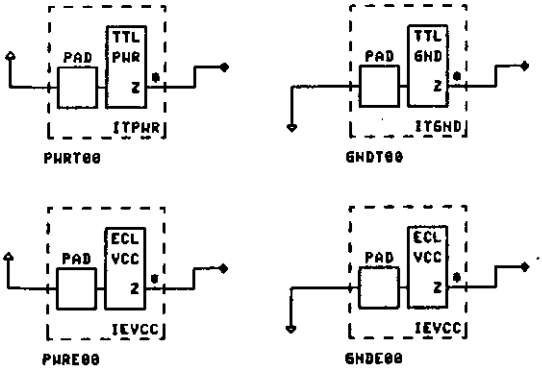
The AMCC EWS schematic convention for the specification of the array and its I/O mode, power supply, product grade, and circuit identification (MILitary or COMmercial) is through the use of a CHIP MACRO. The chip macros carry additional array-specific information used by AMCC MacroMatrix software in processing the design.

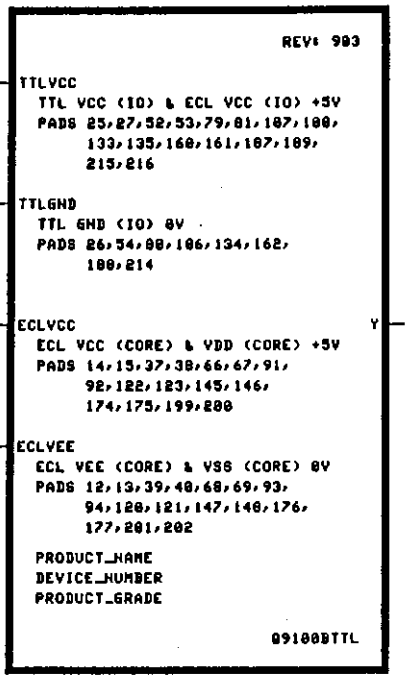
The chip macro POWER_SUPPLY parameter allows the user to specify –5.2V, –4.5V or +5V for 100% ECL circuits and –5.2V or –4.5V for V_{EE} for dual-power supply mixed ECL/TTL circuits.

Refer to EWS Schematic Rules and Guidelines (Section 3 in Volume II) for placement and hook-up procedures. Volume I, Section 6-6 also documents the chip macros and their parameters.

AMCCERC TECHNOLOGY CHECK

The AMCC MacroMatrix ERC technology ERC report will list errors due to improper selection of macros based on the I/O mode selected via the chip macro.





CHIP-POWER/GROUND

Figure 2-5

FIXED POWER AND GROUND PLACEMENT

The chip macro graphics include the pads designated for use by the fixed power (V_{CC}) and ground (V_{EE}) pads required for that particular array and the specified I/O mode. Any power and ground pads added by the user are in addition to the fixed power and ground requirements. The information on the chip macro graphic is commentary. **AMCCIO.LST** and **AMCCPKG.LST** provide a detailed listing of the fixed power and ground pad usage.

Signals cannot be placed on the pads designated as being fixed power or ground pads. All fixed power and ground pads must be used. Fixed power and ground pads provide the minimum number of power and grounds for the array.

POWER BUSSES

The power busses supporting the internal array are isolated from the busses supporting the peripheral I/O cells to minimize the effect of noise coupling between the core and the I/O. The TTL and the ECL ground busses are kept isolated on the chip.

When necessary, there are macros available to provide extra TTL power (ITPWR), TTL ground (ITGND), and ECL power or ground (IEVCC), depending on tha reference voltage.

SIMULTANEOUSLY SWITCHING OUTPUT MACROS

For output macros, TTL outputs are considered to be simultaneously switching if they switch within 3ns of each other. ECL outputs are considered to be simultaneously switching if they switch within 2ns of each other.

- ECL - 2ns
- TTL - 3ns

ADDING EXTRA TTL V_{CC} - TTL GROUND PAIRS (ITPWR-ITGND)

As a design guideline for 100% TTL circuits and for mixed mode ECL/TTL circuits, the designer should allocate a minimum of one additional TTL V_{CC} pad and one TTL GROUND pad to any quadrant of the chip that has more than eight (8) simultaneously switching TTL outputs.

An additional pair is required for each additional eight (8) simultaneously switching outputs in that same quadrant. (See Table 2-6.)

ADDING EXTRA ECL IO V_{CC} (IEVCC)

As a design guideline for any standard reference or +5V reference ECL circuit, the designer should allocate a minimum of one additional ECL V_{CC} pad to any quadrant of the chip that has more than eight (8) simultaneously switching ECL outputs.

An additional ECL V_{CC} (IEVCC) pad is required for each additional eight simultaneously switching ECL outputs in that same quadrant. (See Table 2-6.)

TABLE 2-6 ADDITIONAL POWER/GROUND Q14000 SERIES		
# OF SIMULTANEOUSLY SWITCHING TTL OUTPUTS PER QUADRANT	ADD TTL Vcc - TTL GROUND ADDED ITPWR - ITGND PAIRS	
0 - 8	0	
9 - 16	1	(2 pads)
17 - 24	2	(4 pads)
25 - 32	3	(6 pads)
33 - 40	4	(8 pads)
41 - 46	5	(10 pads)
# OF SIMULTANEOUSLY SWITCHING ECL OUTPUTS PER QUADRANT	ADDED IEVCC	
1 - 8	0	
9 - 16	1	(1 pad)
17 - 24	2	(2 pads)
25 - 32	3	(3 pads)
33 - 40	4	(4 pads)
41 - 48	5	(5 pads)
49 - 50	6	(6 pads)

There is a MAXIMUM of 56 I/O cells per quadrant in the Q14000B. The SSO limit in a quadrant for TTL is 46 TTL SSO + 5 power-ground pairs (10 pads). The SSO limit in a quadrant for ECL is 50 + 6 IEVCCs.

SPECIFYING ADDITIONAL POWER AND GROUND

When additional power and ground pads are desired, the power macros, ITPWR or IEVCC, and the ground macros, IEVCC or ITGND, are placed on the schematic in the quantity desired. IEVCC will be considered a power pad for +5V REF ECL circuits and a GROUND pad for STD REF ECL circuits.

The added power and ground macros each occupy one I/O cell and use its pad. Inclusion of the requirements for extra power and ground is part of the required design submission documentation.

SWGROUP PARAMETER

When the added power and ground is for simultaneously switching circuits, use the macro parameter **SWGROUP** to tag these macros to the group to which they belong. AMCCERC cannot issue error or warning messages on insufficient power or ground if the parameter is not used.

ADDED POWER AND GROUND PLACEMENT

Added ground and power pads must be interspersed with the simultaneously switching signals during placement.

They should be placed on pads that allow connection to the an internal package power or ground plane whenever physically possible, to avoid the use of an external package pin for these macros.

AMCCERC.LST: TOTAL SIGNAL PADS REQUIRED

The AMCC MacroMatrix Population ERC check will correctly reflect the cell count and the total pad count for the design independent of the package selected. The population ERC will report this number as the number of TOTAL ARRAY PADS used by a circuit, the sum of all fixed power and ground, all added power and ground and all interface signals. For a package with no internal power/ground planes, this number is used to select the correct package size.

The number of signal pins that must be available on a package that has internal power/ground planes is the sum of all I/O signals plus any of those added power and grounds that could not be placed to connect to an internal package plane (i.e., that will require a package pin).

AMCCERC.LST will also report on the SUM_TOTAL_I/O which is the sum of all I/O pads used by I/O signals and added power and grounds. Prior to placement, this number can be used as a guideline in selecting a package.

MACRO PIN FAN-IN LOADING

Any macro input pin with a fan-in load greater than one has an asterisk (*) and the fan-in value is listed in the macro documentation in Section 6. The fan-out load of a macro is the sum of the fan-in loads of the macros it drives.

INTERNAL FAN-OUT

Each internal macro output pin is specified to drive a maximum fan-out load. Maximum fan-out limits are specified for individual macros in the macro documentation in Section 6. The fan-out ERC checks for excessive fan-out loading.

DERATING FAN-OUT LIMITS

For clock or distortion-sensitive paths, at speeds up to 100MHz, the maximum fan-out for each macro output pin in the path must be derated by 20%. For clock paths at speeds equal to or greater than 100MHz, the maximum fan-out should be derated by 40%. The fan-out ERC will check for a derated fan-out load limit if the FOD net parameter has been used.

AMCC requires the use of the FOD parameter on all clock nets.

TABLE 2-7
DERATING GUIDELINE

OPERATING SPEED:	DERATE BY:	FOD VALUE
< 100MHz	20%	20
≥ 100MHz	40%	40

STATIC SIGNALS

When an internal macro has an unused pin or it is desired to tie an internal macro input pin to "1" or to "0", the pin is tied to global VSS ("0") or VDD ("1"), not to global GROUND.

When an output or bidirectional macro has an unused input pin that has no hook-up restriction, the pin is tied to global GROUND and not to VSS or VDD. Global GROUND is a logic zero. To tie one of these pins to logic "1", they must be driven by a macro.

VDD and VSS are connected to the internal VDD and VSS busses but are not counted in the internal pin count. Global GROUND is not connected to anything, i.e., it is allowed to float. It is not counted in the internal pin count.

To help the designer, the AMCC MacroMatrix ERC Hook-up check will detect improper interconnects made with global GROUND, VSS and VDD .

INTERNAL CELL UTILIZATION

To insure routability, the recommended maximum internal cell utilization (cell population) for arrays in the Q14000 Series is 95%. Starting designs should target ~70% internal cell utilization to allow for ~20% design expansion during debug, re-design, enhancement, and testing logic additions.

Designs in excess of 95% internal cell utilization for these arrays are considered risky if their internal pin count also exceeds recommended limits or if other placement requirements exist that could cause conflicts.

Compute actual internal cell utilization by first summing the number of Basic cells used by the circuit, and then by dividing that sum by the number of Basic cells available for the particular array.

TABLE 2-8
RECOMMENDED MAXIMUM
INTERNAL CELL UTILIZATION
BASIC CELLS

ARRAY	%
Q14000B	95
Q9100B	95
Q6000B	95
Q2100B	95

AMCC MacroMatrix ERC software computes the internal cell utilization. The software generates a warning if cell utilization exceeds recommended limits and an error if it exceeds 100%.

ODD-CELL UTILIZATION RESTRICTION

BiCMOS odd-sized macros (requiring 3, 5, 7, etc. cells) cannot be reversed in placement (flipped) as most macros can be. As a result, a further utilization check must be made to insure that placement can be achieved.

Compute the internal odd-cell utilization check as follows:

- Count the number of odd-cell macros. This is the number of odd-sized internal macros excluding those macros of size one (1). Use the BiCMOS/Bipolar Macro Occurrence report as a worksheet. Enter the number of cells per macro in one column and the number of occurrences into the second column. This new occurrences column only contains entries for macros with a cell size of 3, 5, 7, 9, etc. Sum this column.

- Count the number of one-cell macros. In a third column, enter the number of occurrences of one-cell macros. Sum this column.

- Compute the number of vacant cells where:

$$\text{vacant cells} = \text{number of Basic cells available} + \text{number of Basic cells used}$$

  The Population ERC report provides the SUM_LOGIC entry which is the sum of internal logic (Basic) cells. The number used is listed under CIRCUIT; the number available is listed under AVAILABLE. Subtract used from available.

- The number of odd-cell occurrences must be less than or equal to the sum of the vacant cells and the number of one-cell occurrences.

$$\text{number of odd-cell occurrences} \leq \text{vacant cells} + \text{number of one-cell occurrences}$$

  If the equation is not met, placement may not be possible. Consult AMCC.

  The MacroMatrix ERC software will be expanded to perform this additional cell utilization check.

INTERNAL PIN COUNT

The internal pin count is another measure of the routability of a circuit on a given array.

- Prior to schematic capture, the internal routable pin count should be estimated and used in the selection of the required array. A guideline for estimate limit is 20% of the captured circuit limit. See Table 2-9.
- After capture, the AMCC MacroMatrix ERC software provides a detailed report on the internal pin count of the circuit. For a captured circuit, refer to the limits in Table 2-9.

TABLE 2-9
MAXIMUM INTERNAL PIN COUNT
I/O AND BASIC CELLS

ARRAY	ACTUAL LIMIT	ESTIMATED LIMIT
Q14000B	11511	9208
Q9100B	7781	6224
Q6000B	4986	3988
Q2100B	1915	1532

- A circuit with an actual internal pin count that is less than the limit is routable.
- A circuit with an actual pin count that is 1-10% over the limit is considered risky (may have problems).
- A circuit with an actual pin count of 11-18% over the limit is considered very risky and may not successfully route.
- A circuit with an actual pin count of 18% or more over the limit is considered unroutable and a redesign is required if a larger array cannot be used.

Q14000 SERIES BASIC DESIGN RULES AND GUIDELINES

Once the macros have been selected, and the basic circuit defined, the designer should review the circuit prior to submission to AMCC to verify that basic design rules have not been violated. Some of these rules and design checks are listed below.

Guidelines are suggestions to help ensure first-design success; rules are design requirements that cannot be violated. For further information, refer to the Design Submission and Design Validation documents, Section 6 and Section 5 of Volume II of this design manual.

- Create a schematic following EWS Schematic Rules, Section 3, Volume II.
- Fan-out - no macro drives more than its rating
- Fan-out derating - critical clock or distortion sensitive paths have derated clock loading: 20% up to 100MHz; 40% for ≥ 100MHz. Use the FOD net parameter/property.
- Fan-out - no macro output pin is to drive more than one input pin of an SSI gate within a macro. Driving multiple inputs on a MUX is allowed.
- Fan-in - any macro with en asterisk on an input pin has been checked for fan-in > 1.
- Pin-restrictions - any macro with an asterisk has been cross-checked to be certain that it is connected to or driven from a legal macro connection.
- Unused macro input pins - INTERFACE MACROS EWS convention is to ground any unused inputs unless the macro documentation indicates that a pin cannot be grounded. (Grounded signals assume low level logic and physically float.)

- Unused macro input pins - INTERNAL MACROS EWS convention and design requirements dictate that unused internal macro input pins be tied to VDD or VSS.
- Pin connections - Make certain that input and output pins are properly connected, including PAD connections.
- Bidirectional signals - Be certain that bidirectional macro pins have been connected to a bidirectional connector (EWS convention). Refer to Volume II, Section 7 for additional information.
- Grounded output pins - These are not allowed.
- Terminated input pins - These are not allowed.
- Macro type - Check that the proper TTL I/O macros were chosen based on the circuit type.
- Macro type - Check that the proper ECL versions of the ECL macros were chosen based on the circuit type.
- Signal names - Check that all connections - intra-pege, inter-page, off-chip and 3-state and bidirectional enables - have been properly named. Refer to Volume II, Section 3 for naming conventions and rules.
- Cell utilization - Do not violate the internal cell utilization limit without AMCC approval.
- Internal pin count - Do not exceed the array limit.
- Additional power end ground - Provide additional power and ground pins as needed by using the ITPWR, ITGND and IEVCC macros on the schematic.
- Simultaneously switching outputs - Use the SWGROUP macro parameter/property to allow the simultaneously switching output ERC check.
- When leaded chip carriers are to be used, care should be taken to supply sufficient ground pins to allow separation of any signals where cross-talk may be of concern, e.g., between input and output signals. Spare pins should be grounded.

- Total PAD count - Do not exceed the maximum pad count limit for the array. ITGND, IEVCC, and ITPWR macros use cells and pads and are counted.
- Overhead Current - Estimate overhead current based on I/O type and usage. See Section 5.
- Powar - Compute the maximum worst case DC power. Include any ECL static output power.
- Power - Compute the AC component of the worst-case power. Combine the DC power dissipation of the interface macros with the power computed for the internal macros.
- Packaging - Verify that the package selected is appropriate for the environment and junction temperature (compute based on power).
- Packaging - Verify that the number of I/O signal pads, including any added power and grounds that cannot use an internal package power-ground plane, is less than or equal to the signal pins available on the package.
- Packaging - Verify that the selected heatsink is available for this array and package.
- Critical paths - Complete the description of and clearly identify the critical paths.
- AC Tests - Clearly identify path(s) to be tested with an AC test.
- AMCCERC.LST, AMCCIO.LST, AMCCPKG.LST and several (renamed) AMCCVRC.LST reports must be submitted. Refer to Design Submission, Section 6, Volume II.
- Complete simulation documentation must be submitted with the design, including source files.
- For guidance in constructing simulation vectors, refer to the AMCC document:
  Vector Submission Rules and Guidelines.
  Refer to Section 4, Volume II.
- Placement - Consult with AMCC Applications prior to attempting a pre-placement file. Review restrictions for dual-cell I/O macros, simultaneously switching outputs and packaging-power/ground plane added power and ground macro placement.

POWER BUS DISTRIBUTION AND DECOUPLING

Optimal Power Bus Distribution and Decoupling is dependent on a number of interactive device and system variables, including the package design used, the number of simultaneous switching outputs on the device, output loading, the amount of switching noise contributed by other system components, the number of power busses and the design of the system and module power distribution.

AMCC recommends the use of multi-layer PC boards that provide dedicated low impedance power and ground planes. Besides maintaining a constant characteristic impedance for transmission lines, the planes provide for a low impedance return path to the ECL or TTL circuitry and act as an electromagnetic shield for the signal lines. The distributed capacitence will also improve noise margins by minimizing "ground bounce" and crosstalk.

The 2-layer PC boards, on the other hand, may require successive approximations to optimize the system noise margins and reduce externel noise from being fed back into the chip through the power and ground pins. This approach should only be ettempted in lower performance systems.

The I/O ECL V_{CC} and the Internal V_{CC} package pins should be tied together es close to the chip es possible, using good high frequency practices. When mixed I/O is combined with multiple power busses, the TTL GND and ECL V_{CC} (0V) cen be tied directly together at the chip on multi-layer boards.

For 2-sided boards, the location will be system dependent and may require some experimentation. The primary considerations are the amount of simultaneous switching, the signal/ground pin ratio and the isolation between the TTL and ECL signal lines (and return paths).

Low frequency (bulk) decoupling is generally provided in the range of 0.5 to 2.0 μf/WATT, while high frequency by-passing should be 100 to 1,000 pF/quadrant. The by-pass capacitors are generally placed as close to the chip as possible using high frequency techniques to minimize the inductance in the leads, traces, feed-throughs and componants.

The AMCC Q14000 performance boards use a 1μf tantalum capacitor in parallel with a 470pf ceramic chip capacitor for each of the Internal V_{EE}/V_{CC} pairs. This same combination is used for any V_{CC} or additional V_{CC} package pins with excellent results.

TESTABILITY

Concepts of testing and testability must be considered from the beginning of any circuit design. AMCC encourages: (1) the use of testability techniques in circuit design; (2) the use of testebility analysis early in the design process so that testability problems can be corrected by design; (3) the use of fault grading to assess test vector fault coverage; and (4) an understanding of the capabilities of today's advanced test equipment in the development of semi-custom circuits.

STRUCTURED DESIGN

Structured approaches to ensure circuit testability such as LSSD, Scan Path and BILBO are generally driven by an overall system philosophy to testing. While AMCC does not promote one structured technique over another, other measures during design can improve circuit testability. AMCC does promote the use of overall structured design procedures, including functional modularity, bus architectures and clear documentation.

TESTABILITY ANALYSIS

All testability measures have one common goal: to enhance controllability and observability of the circuit. It is a grade on the logic design itself. Controllability is a measure of the ease in setting a particular node to a logic level of zero or one, while observability determines the ease of propagating the node's state to one or more primary outputs.

After a netlist has been created and logic simulation has verified correct functional performance, testability can be verified by running testability analysis programs such as DTA (DAISY) or COPTR (TEGAS). (These programs are currently not supported by AMCC.)

FUNCTIONAL SIMULATION

The object of functional testing is to detect a single SA1 or SA0 fault in the circuit if one exists. This ideally requires sufficient vectors to "cover" all possible fault locations. The percent of coverage is the fault grade of the vector set. To this end, one approach is to cycle all inputs and outputs through 1-0 and 0-1 transitions as a first check after initialization. (This should cycle all internal nodes as well.) This 2^n (n = number of inputs) brute force approach is not necessary. Minimum vector test sets and minimum vector test sequences will cover 100% of all observable faults.

Functional simulation vector fault-grading can be performed using the TEGAS simulator. Fault-grading is used to verify that the simulation bit vectors sufficiently exercise nodes within the circuit to assure that the outgoing product matches the customer specification. Insufficient fault coverage as determined in a fault grading run may require the addition of vectors to the set developed to evaluate logical functionality.

AMCC recommends the creation of a sufficient number of vectors to achieve a fault coverage of 90% or higher, and is prepared to perform the fault grading task upon request.

For guidelines in performing functional simulation, refer to Vector Submission Rules and Guidelines in Section 4, Volume II of this design manual.

AMCCVRC Vector Rules Checker must be run against any AMCCSIMFMT (AMCC Simulation Format) maximum worst-case sampled simulation output file.

AT-SPEED SIMULATION

In addition to functional simulation, the customer must perform an at-speed simulation and timing analysis for all critical (i.e., timing-sensitive) paths in the circuit. Refer to the above referenced document.

AC TESTS SIMULATION

AC path propagation delay tests require simulation vectors to initialize the circuit path to be measured and to support the measurement of the path. Provided the start and stop addresses are clearly documented, all AC tests may be grouped in one simulation file. Each AC test path must be clearly documented. A test path is defined as a single input to a single output.

AMCCVRC is run against any sampled, maximum worst-case AC test simulation output file in accordance with the rules listed in Section 4, Volume II.

If the path propagation delay to be measured is less than 10ns typical, consult AMCC.

PARAMETRIC TESTING

Parametric testing for V_{IOH}, V_{IOL} is optional and can be realized in saveral different ways. AMCCVRC can be run to partially chack parametric testing simulations written with (809) MacroMatrix software. Future releases will expand the testing performed.

DESIGN FOR TESTABILITY

Some specific design suggestions for improved circuit testability are:

- Become familiar with the macro library BEFORE beginning the macro conversion or design.
- Use synchronous rather than asynchronous circuits whenever possible - functional tests are synchronous.
- Partition the design (use structured design techniques) into smaller, testable sections, usually along a functional boundary.
  - Use degating logic to isolate modules for test.
  - Use modular architecture, bus structures.
  - Break up long counters (>8).

- Don't bury states.
- Use transparent latches instead of flip/flops where possible and use I/O latches instead of flip/flops.
- Use macros, especially flips/flops end latches, with RESET or SET controls where possible to simplify initialization.
- Avoid feedback loops.
- If unavoidable, provide a means to break up feedback loops during test (degating, enables).
- Avoid redundant logic - minimizel - or add test points to unmask masked faults.
- Avoid derived clocks - they complicate testing.
- Design in test points, especially in sequential logic. Add test points to improve controllability and observability. Perform testability analysis.
- If I/O pins are limited, use demultiplexors to control and multiplexors to observe internel nodes with otherwise poor observability (buried states).
- Any 3-state enable control signal that is internally generated must be externally observable, and should be externally controllable during test.
- Add parity trees for error detection. Or use Scan Path Design to simplify test sequence generation or use Level Sensitive Scan Design to simplify test sequence generation. Keep test generation in mind while designing the circuit.

DESIGN FOR RELIABILITY

Some specific design suggestions for improved circuit reliability are:

- Become familiar with the macro library BEFORE beginning the macro conversion or design.
- Be aware of "glitch" circuits. Do not use potential glitch circuits to drive clock inputs.
- Avoid one-shot pulse generators.
- Avoid gated and derived clocks.
- Avoid race and hazard conditions. (PRINT_ON_CHANGE files can help identify these.) These are generated by having a signal follow two or more paths to a common circuit element (a.k.a. reconvergent fan-out.)
- Avoid feedback loops.
  - If unavoidable, provide a means to break up feedback loops during test (using degating, enables).
- Avoid feedback paths between registers. If present, compute the worst-case set-up and hold times and verify operation. (Feedback from the ECL output macros must be handled with care if used to input to internal latches and flip/flops.)
- Add sufficient GROUND for the number of simultaneously switching outputs and distribute among these outputs (similar to distributed ground in a ribbon cable). Add additional extra ground if there ara extra I/O pins available.
- Add extra V_{CC} as needed for the number of simultaneously switching outputs.
- Properly derate fan-out on all distortion-sensitive paths and all clock paths. Keep clock path loading balanced.

- Avoid floating nodes on internal 3-state busses or external bidirectional busses.
- Use Johnson (a.k.a. Mobius, Ring or Twisted-tail) counters or separate flip/flops to decode terminal counts. The loading on the Q outputs is identical, eliminating the loading skew (not the metal skew), and the outputs are a Gray code - only one output changes state per clock cycle. (Binary counter decoding can cause glitches.)
- Compensate for rising and falling edge loading skews and the reversed TTL input translator rising and falling edge skews by inversion as needed to reduce pulse stretch and pulse shrink phenomena.

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The following tables are taken from the Q14000 Series data sheet and define the operating conditions, maximum chip ratings, DC parametrics and TTL load circuits.

RECOMMENDED OPERATING CONDITIONS – COMMERCIAL

PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE}) V_{CC} = 0				
10K Mode	-4.94	-5.2	-5.45	V
100K Mode	-4.2	-4.5	-4.8*	V
ECL Input Signal Rise Fall Time	-	1.5	5.0	ns
TTL Supply Voltage (V_{CC})	4.75	5.0	5.25	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	0 (ambient)		70 (ambient)	°C
Junction Temperature			130	°C

RECOMMENDED OPERATING CONDITIONS – MILITARY

PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE}) V_{CC} = 0				
10K Mode	-4.7	-5.2	-5.7	V
100K Mode	-4.2	-4.5	-4.8*	V
ECL Input Signal Rise Fall Time	-	1.5	5.0	ns
TTL Supply Voltage (V_{CC})	4.5	5.0	5.5	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	-55 (ambient)		125 (case)	°C
Junction Temperature			150	°C

* 5.7V is possible. Consult AMCC for ECL 100K DC parametrics operating at this voltage

ABSOLUTE MAXIMUM RATINGS

ECL Supply Voltage V_{EE} (V_{CC} = 0)	-8.0 VDC
ECL Input Voltage (V_{in} = 0)	GND to V_{EE}
ECL Output Source Current (continuous)	-50 mA DC
TTL Supply Voltage V_{CC} (V_{EE} = 0)	7.0 V
TTL Input Voltage (V_{EE} = 0)	5.5 V
Operating Temperature	-55°C (ambient) to +125°C (case)
Operating Junction Temperature T_J	+150°C
Storage Temperature	-65°C to +150°C

ECL 10K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -5.2V$[1]

	$T_{ambient}$				T_{case}	
	−55°C	0°C	25°C	75°C	125°C	UNIT
$V_{OH\,max}$	V_{CC}− 850	V_{CC}− 770	V_{CC}− 730	V_{CC}− 650	V_{CC}− 575	mV
$V_{IH\,max}$	V_{CC}− 800	V_{CC}− 720	V_{CC}− 680	V_{CC}− 600	V_{CC}− 525	mV
$V_{OH\,min}$	V_{CC}−1080	V_{CC}−1000	V_{CC}− 980	V_{CC}− 920	V_{CC}− 850	mV
$V_{IH\,min}$	V_{CC}−1255	V_{CC}−1145	V_{CC}−1105	V_{CC}−1045	V_{CC}−1000	mV
$V_{IL\,max}$	V_{CC}−1510	V_{CC}−1490	V_{CC}−1475	V_{CC}−1450	V_{CC}−1400	mV
$V_{OL\,max}$	V_{CC}−1655	V_{CC}−1625	V_{CC}−1620	V_{CC}−1585	V_{CC}−1545	mV
$V_{OL\,min}$	V_{CC}−1980	V_{CC}−1980	V_{CC}−1980	V_{CC}−1980	V_{CC}−1980	mV
$V_{IL\,min}$	V_{CC}−2000	V_{CC}−2000	V_{CC}−2000	V_{CC}−2000	V_{CC}−2000	mV
$I_{in}H\,max$[2]	30	30	30	30	30	µA
$I_{in}L\,max$[2]	− 5	− 5	− 5	− 5	− 5	µA

ECL 100K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -4.5V$[3]

SYMBOL	PARAMETER	TEST DC CONDITIONS	COMM'L 0° / +70°C			MIL −55° / +125°C			UNIT
			V_{EE} = −4.2V to −4.8V			V_{EE} = −4.2V to −4.8V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	Output Voltage HIGH	Loading is 50 Ohms to − 2V	V_{CC}-1035		V_{CC}- 850	V_{CC}-1080		V_{CC}- 835	mV
V_{OL}	Output Voltage LOW	Loading is 50 Ohms to − 2V	V_{CC}-1830		V_{CC}-1605	V_{CC}-1880		V_{CC}-1595	mV
$V_{IH\,min}$	Input Voltage HIGH	Maximum input voltage HIGH	V_{CC}-1145		V_{CC}- 800	V_{CC}-1145		V_{CC}- 800	mV
$V_{IL\,max}$	Input Voltage LOW	Maximum input voltage LOW	V_{CC}-1950		V_{CC}-1475	V_{CC}-1950		V_{CC}-1475	mV
I_{IH}[2]	Input Current HIGH	$V_{IN} = V_{IH\,max}$			30			30	µA
I_{IL}[2]	Input Current LOW	$V_{IN} = V_{IL\,min}$			− 5			− 5	µA

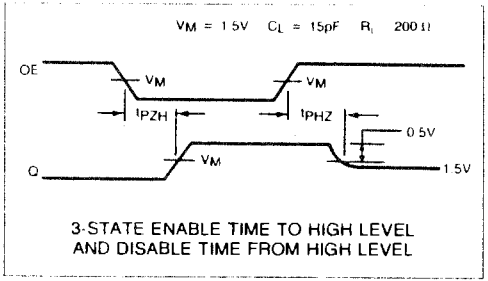
TTL INPUT/OUTPUT DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST DC CONDITIONS		COMM'L 0°/+70°C			MIL −55°/+125°C			UNIT
				MIN	TYP[4]	MAX	MIN	TYP[4]	MAX	
V_{IH}[5a]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs		2.0			2.0			V
V_{IL}[5b]	Input LOW voltage	Guaranteed input LOW voltage for all inputs				0.8			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = −18mA			−.8	−1.2		−.8	−1.2	V
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = −1mA		2.7	3.4		2.4	3.4		V
V_{OL}	Output LOW voltage	V_{CC} = Min	I_{OL} = 8mA			0.5			0.5	V
			I_{OL} = 20mA			0.5			0.5	V
			I_{OL} = 48mA			0.6			0.6	V
I_{OZH}	Output "off" current HIGH (3-state)	V_{CC} = Max, V_{OUT} = 2.4V		−50		50	−50		50	µA
I_{OZL}	Output "off" current LOW (3-state)	V_{CC} = Max, V_{OUT} = 0.4V		−50		50	−50		50	µA
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7V				50			50	µA
I_I	Input HIGH current at Max	V_{CC} = Max V_{IN} = 5.5V				1			1	mA
I_{IL}	Input LOW current	V_{CC} = Max, V_{IN} = 0.5V				50			50	µA
I_{OS}	Output short circuit current	V_{CC} = Max V_{OUT} = 0V		−25		−100	−25		−100	µA

1. Data measured with V_{CC} = +5.2 ± .1V (or V_{CC} = +5.0 ± .1V for +5V ref. ECL 10K) assuming a +50°C rise between ambient (T_A) and junction temperature (T_J) for −55°C, 0°C, +25°C and +70°C and a +25°C rise for +125°C. Specifications will vary based upon T_J. See AMCC Packaging and Design Guides concerning V_{CC} and V_{EE} adjustments associated with T_J for packages and operating conditions.
2. Per fanout.
3. Data measured at thermal equilibrium with maximum T_J not to exceed recommended limits. See AMCC Packaging Guide to compute T_J for specific package and operating conditions. For +5V ref. ECL 100K V_{CC} and V_{EE} specifications will vary based upon power supply. See AMCC Design Guide for adjustment factors.
4. Typical limits are at 25°C, V_{CC} = +5.0V.
5a. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
5b. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using V_{IL} = 0.4V and V_{IH} = 2.4V for functional and AC tests.

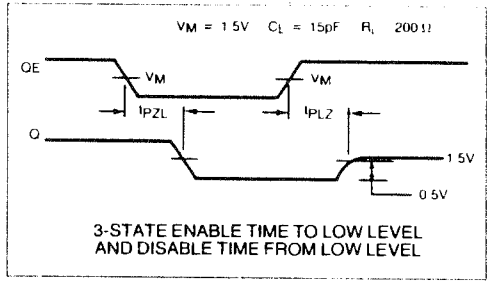
FIGURE 6

FIGURE 7



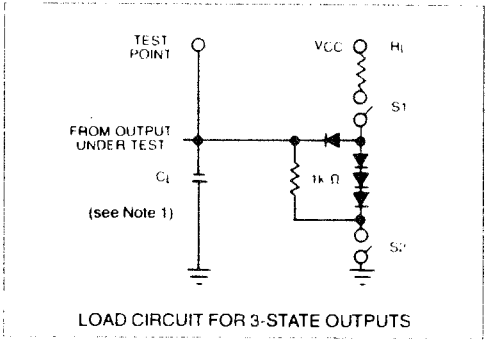
3-STATE ENABLE TIME TO HIGH LEVEL
AND DISABLE TIME FROM HIGH LEVEL

FIGURE 9



3-STATE ENABLE TIME TO LOW LEVEL
AND DISABLE TIME FROM LOW LEVEL

FIGURE 10



LOAD CIRCUIT FOR 3-STATE OUTPUTS

3-STATE TEST CIRCUIT SWITCH TABLE

TEST FUNCTIONS	S1	S2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

NOTES:

1. Standard TTL load circuit used for macro specification, see Figures 2 and 7
   CL includes probe, jig and package capacitance
2. V_{IN} = 0 to 3.0 volts

Section 3:

Timing Analysis

Table of contents 3-2

COMPUTING PROPAGATION DELAY

The macros selected, the options of those macros, the loading on the macros, and the final layout of the circuit are all factors in the propagation delay of any path. The loading may be the interconnact capacitance or the external load capacitance due to system loading and package pin capacitance.

There are two approachas that can be usad to compute propagation delay: Front-Annotation, where a statistical estimate (averaged value) of matal delays based on net sizes is used; and Back-Annotation, where the actual metal delay is used in the computation.

- **PRELIMINARY COMPUTATION - PRIOR TO CAPTURE**

The path propagation delays can be estimated using the statistical wire delay tables (L_{net}), fan-out loading (L_{fo}) and the appropriate k-factors (k) for the macros chosen. The equation for the typical extrinsic (load) delay for a single internal net is shown below and discussed in detail on the following pages.

$$t_{ex} = k \bullet (L_{fo} + L_{net})$$

The equation for the typical extrinsic (load) delay for a single output net is shown below and discussed in detail on the following pages.

$$t_{ex} = k \bullet (C_{system} + C_{package})$$

The sum of all typical intrinsic macro delays in the path (t_{in}; specified as Tpd in the macro documentation) and all extrinsic loading (t_{ex}) is then multiplied by the proper ANNOTATED worst-case timing multiplication factor.

- **FRONT-ANNOTATION - AFTER CAPTURE**

After schematic capture, Front-Annotation software is available to provide the designer with a file of rising and falling edge delays per net (expressed as NOM, MIN and MAX). By incorporating this file into the simulation database, the designer can obtain a statistical estimate of circuit performance.

Front-Annotation uses a metal load delay computed as the average of metal delays that might be expected for the specific net size on a specific array. Front-Annotation uses the actual electrical load delay. Front-Annotation cannot be guaranteed.

- **BACK-ANNOTATION - AFTER LAYOUT**

The most accurate method of computing a circuit propagation delay requires that the circuit be completed through layout. Back-annotation software adds the actual metal delay and fan-out delays into the path. Back-annotation must be run and accepted as final prior to the generation of the actual silicon arrays. The Back-Annotation program provides a file which includes the ACTUAL metal delays in a net along with the actual electrical load delays.

AMCC guarantees that the silicon will match (will not be slower than) the results of the Back-Annotation.

• TYPICAL INDIVIDUAL MACRO PROPAGATION DELAY

AMCC macro documentation specifies typical, unloaded macro path propagation delays (Tpd) for each path through a macro. Some macro specifications include a different delay for a rising edge (Tpd−+) than for a falling edge (Tpd+−). Three-state macros have specifications for high-Z representative switching delays T_{PHZ}, T_{PZH}, T_{PZL} and T_{PLZ}.

The actual macro path delay will be a function of: state of the input data (low data may have different set-up and hold times than high data); multiple inputs changing state (e.g., when several OR/NOR inputs change simultaneously on an internal macro, the delay increases).

To account for some of these path delay variations, the AMCC macro specifications have been expanded to show the model behavior in more detail. The specifications are interpreted as follows:

Non-inverting:
- Tpd++ rising edge input; rising edge output
- Tpd−− falling edge input; falling edge output

Inverting:
- Tpd+− rising edge input; falling edge output
- Tpd−+ falling edge input; rising edge output

All AMCC EWS simulation models are accurate to within 10ps (two decimal place accuracy when measured in ns).

AMCC macro specifications, as documented in the Design Guides and Design Manuals for the individual array series, show the typical propagation delay for a path through a macro for nearly all of the possible conditions. Multiplexer specifications are simplified.

- **INTRINSIC SET-UP AND HOLD TIMES**

The intrinsic set-up and hold times for the latches, flip/flops and MSI macros that include one or more of these types of devices, are specified in the macro summary in Section 6. The parameters represent the behavior of the macro as observed at its input and output nodes. Set-up time (Tsu) is the time that a signal must be stable prior to the active clock edge. Hold time (Th) is the time that a signal must be held after the active clock edge.

- **RECOVERY TIME**

Recovery time (Trec) is specified for any latch or flop/flop which has a set or reset. It is the length of time that a reset/set signal has to have been inactive prior to an active clock edge. Clocking within the recovery time period will result in unpredictable behavior.

Note: Set-up time, hold time, recovery time and minimum pulse width are all specified as typical values and must be multiplied by the appropriate worst-case delay multiplication factor.

- **COMPUTING THE LOADING DELAY FOR AN OUTPUT NET**

ECL and TTL output macros are specified with no capacitive loading on the macros. The method for manual computation of the effect of load units on the propagation path is:

For each output net:

$$t_{ex} = k \cdot (C_{system} + C_{package})$$

where

k = the k-factor for output macro as listed in Section 6
C_{system} = the system capacitive load as seen by the pin
$C_{package}$ = the package pin capacitance for that pin

TABLE 3-1
OUTPUT MACRO k-FACTORS

	ns/pF
TTL	0.055
ECL	0.045

- For TTL or ECL output loads up to but less than 100pf, use Table 3-1.
- For TTL or ECL output loads over 100pf, consult AMCC.

The AMCCANN user interface on the workstation allows the specification of the package, the package pin capacitance and the system load. Both package pin and system load capacitances may be specified as default values (all pins identical) or on an individual pin or group of pins basis. The output loading delay is automatically computed and added to the annotation files. All simulations are performed with annotation delay files.

- **COMPUTING THE LOADING DELAY FOR AN INTERNAL NET - FRONT ANNOTATION**

The method for manual computation of the effect of load units on the propagation path is:

For each internal net:

$$t_{ex} = k \cdot (L_{fo} + L_{net})$$

where

k = the k-factor for the series and the macro option as listed in Section 6. An overview of k-factors is listed in Table 3-2. Refer to Section 6 for the actual k-factor of the macro in use.

L_{fo} = the sum of the electrical fan-out loads in a net. (Pins with a fan-in of 2 count as 2 electrical loads)

L_{net} = the estimated metal delay from Table 3-3, indexed by the sum of the number of pins in the net minus 1 (i.e., index by [net size - 1]) (Pins with a fan-in of 2 count as 1 physical load)

TABLE 3-2
TYPICAL k FACTORS - Q14000*

		ns/LU
INTERNAL MACROS:		
k_{up}	S-option	0.025-0.045
k_{down}	S-option	0.025-0.045
INTERFACE (I/O) MACROS:		
k_{up}	S-option	0.025
k_{down}	S-option	0.030
k_{up}	H-option	0.025
k_{down}	S-option	0.030
k_{up}	L-option	0.025
k_{down}	L-option	0.047

*Refer to Section 6 for the k-factors for a specific macro.

- **COMPUTING L_{net}**

Compute the statistical metal estimate by counting the physical pins in the net (driving or source pins and destination pins), subtracting one (1), and using this number as the index to the following table. The number listed under a specific array is the estimate for the load units due to metal in the net.

TABLE 3-3
FRONT-ANNOTATION
Q14000 SERIES
STATISTICAL WIRE LOADS
L_{net}

NET -1	Q14000B	Q9100B	Q6000B	Q2100B
1	1.20	1.18	1.10	1.00
2	2.27	2.20	1.92	1.58
3	3.30	3.17	2.65	2.06
4	4.30	4.11	3.33	2.50
5	5.28	5.02	3.99	2.89
6	6.24	5.92	4.61	3.26
7	7.19	6.80	5.22	3.61
8	8.13	7.67	5.81	3.94
9	9.06	8.53	6.38	4.26
10	9.98	9.37	6.94	4.57
11	10.90	10.21	7.49	4.87
12	11.80	11.04	8.03	5.16
13	12.71	11.87	8.56	5.44
14	13.60	12.69	9.08	5.71
15	14.49	13.50	9.60	5.97
16	15.38	14.31	10.11	6.23
17	16.26	15.11	10.61	6.49
18	17.14	15.91	11.11	6.74
19	18.02	16.70	11.60	6.98
20	18.89	17.49	12.08	7.22
21	19.75	18.28	12.57	7.46
22	20.62	19.06	13.04	7.69
23	21.48	19.84	13.51	7.92
24	22.33	20.61	13.98	8.15
25	23.19	21.38	14.45	8.37
26	24.04	22.15	14.91	8.59
27	24.89	22.91	15.36	8.80
28	25.74	23.68	15.82	9.02
29	26.58	24.44	16.27	9.23
30	27.42	25.19	16.71	9.44

Index using net size - 1.

TABLE 3-3
FRONT-ANNOTATION
Q14000 SERIES
STATISTICAL WIRE LOADS
L_{net}

NET -1	Q14000B	Q9100B	Q6000B	Q2100B
31	28.26	25.95	17.16	9.64
32	29.10	26.70	17.60	9.85
33	29.94	27.45	18.04	10.05
34	30.77	28.20	18.47	10.25
35	31.60	28.94	18.91	10.45
36	32.43	29.69	19.34	10.65
37	33.26	30.43	19.77	10.84
38	34.09	31.17	20.19	11.03
39	34.91	31.90	20.62	11.22
40	35.73	32.64	21.04	11.41
41	36.55	33.37	21.46	11.60
42	37.37	34.10	21.88	11.79
43	38.19	34.83	22.29	11.97
44	39.01	35.56	22.71	12.15
45	39.82	36.29	23.12	12.33
46	40.64	37.01	23.53	12.51
47	41.45	37.74	23.94	12.69
48	42.26	38.46	24.34	12.87
49	43.07	39.18	24.75	13.05
50	43.88	39.90	25.15	13.22
51	44.68	40.62	25.55	13.40
52	45.49	41.33	25.95	13.57
53	46.29	42.05	26.35	13.74
54	47.10	42.76	26.75	13.91
55	47.90	43.47	27.14	14.08
56	48.70	44.18	27.54	14.25
57	49.50	44.89	27.93	14.42
58	50.30	45.60	28.32	14.58
59	51.09	46.31	28.71	14.75
60	51.89	47.01	29.10	14.91

Index using net size - 1.

- **COMPUTING L_{fo}**

Compute L_{fo} by adding the sum of the electrical load of all loads driven. If a destination pin has a fan-in of 2, it counts as two electrical loads and as one physical pin. A destination may appear to have two physical loads internal to the macro. In these cases, the macro documentation will clearly identify the fan-in load represanted by that pin. Physical fan-out internal to the macro does not affact the physical pin count.

WORST-CASE DELAY MULTIPLICATION FACTORS

Once the sum of all of the intrinsic and extrinsic propagation delays in a path or path segment is computed and adjusted for any external high-capacitive loading (system load and package pin capacitance), then the result must be multiplied to obtain the worst-case delay as follows:

$$Tpd_{typical} * M.F. = Tpd_{worst-case}$$

Multiplication factors are shown in Table 3-4. The worst-case multipliers take into eccount the following:

- Process variations
- Temperature variations
- Voltage variations

TABLE 3-4
WORST-CASE DELAY MULTIPLICATION FACTORS
Q9100B and Q2100B ARRAYS
WORST-CASE MULTIPLIERS FOR FRONT- AND BACK-ANNOTATION
WCM

		INTERFACE	INTERNAL
MINIMUM	minimum	0.70	0.70
	typical	0.78	0.78
	maximum	0.86	0.86
NOMINAL	minimum	0.90	0.90
	typical	1.00	1.00
	maximum	1.10	1.10
COMMERCIAL (COM5)	minimum	1.11	1.27
	typical	1.23	1.41
	maximum	1.35	1.55
COMMERCIAL (COM4)	minimum	1.11	1.43
	typical	1.23	1.59
	maximum	1.35	1.75
MILITARY	minimum	1.19	1.59
	typical	1.32	1.77
	maximum	1.45	1.95

minimum represents .90% * typical
maximum represents 1.1% * typical
Commercial: $T_j \leq 130°$
Military: $T_j \leq 150°$

TABLE 3-4
(Continued)
WORST-CASE DELAY MULTIPLICATION FACTORS
Q14000B and Q6000B ARRAYS
WORST-CASE MULTIPLIERS FOR FRONT- AND BACK-ANNOTATION
WCM

		INTERFACE	INTERNAL
MINIMUM	minimum	0.70	0.70
	typical	0.78	0.78
	maximum	0.86	0.86
NOMINAL	minimum	0.90	0.90
	typical	1.00	1.00
	maximum	1.10	1.10
COMMERCIAL (COM5)	minimum	1.27	1.27
	typical	1.41	1.41
	maximum	1.55	1.55
COMMERCIAL (COM4)	minimum	1.27	1.43
	typical	1.41	1.59
	maximum	1.55	1.75
MILITARY	minimum	1.40	1.59
	typical	1.55	1.77
	maximum	1.70	1.95

minimum represents .90% * typical
maximum represents 1.1% * typical
Commercial: $T_j \leq 130°$
Military: $T_j \leq 150°$

TABLE 3-5
APPLICATION RULES FOR THE WORST-CASE DELAY MULTIPLIERS

- Set-up time, hold time, recovery time and minimum pulse width are multiplied by a worst-case delay multiplier.
- Macro intrinsic delays and extrinsic delays are multiplied by the worst-case delay multipliers.
- The worst-case multipliers used for the extrinsic net delays should be consistent with the macro type of the macro driving the net, i.e., nets driven by the input macros should use the interface macro worst-case delay multiplier.
- Commercial grade multipliers: The worst-case delay multiplier for the extrinsic delay caused by output load capacitance is the interface macro worst-case delay multiplier.
- COM4 multipliers apply when a power supply of -4.5V is used for ECL (-4.2V maximum) in a 100% ECL or a mixed ECL/TTL circuit. COM5 multipliers apply for all other cases. Front-Annotation and Back-Annotation multipliers will be correct as of the (809) release software but will be inaccurate for COM4 circuits in earlier release software.

The AMCCANN software on the workstations will produce annotation files using the correct multipliers.

SELECTING THE CORRECT WORST-CASE DELAY MULTIPLIER

COMMERCIAL SPECIFICATION

Circuit with a –4.5V supply: Commercial worst-case COM4 timing multipliers are for circuits operating in the 0°C ambient to 70°C ambient temperature range with a ±7% variation on a power supply of –4.5V (–4.2V to –4.8V) and a junction temperature maintained at **≤ 130°C.**

All other circuits: Commercial worst-case COM5 timing multipliers are for circuits operating in the 0°C ambient to 70°C ambient temperature range with a ±5% power supply variation and a junction temperature maintained at **≤ 130°C.**

For a junction tamperature that is > than 130°C, or for any other circuit specification that exceeds the commercial environment specification, use the Military worst-case timing data when computing path propagation delay or set-up and hold times.

MILITARY SPECIFICATION

Circuit with a –4.5V supply: Military worst-case timing multipliers are for circuits operating in the –55°C ambient to +125°C case temperature range with a ±7% power supply variation (–4.2V to –4.8V) and a junction temperature maintained at **≤ 150°C.**

All other circuits: Military worst-case timing multipliers are for circuits operating in the –55°C ambient to +125°C case temperature range with a ±10% power supply variation and a junction temperature maintained at **≤ 150°C.**

For a junction temperature that is > than 150°C, or for any other circuit specification that exceeds the military environment specification, consult AMCC.

MINIMUM PROPAGATION DELAY

AMCC does not specify minimum circuit delays. However, a guideline for minimum propagation delay is 70% of the typical path delay (the annotated worst-case minimum multiplier is 0.70). Note that both the interface and the internal macros use the same worst-case minimum multiplier.

Where the performance of a circuit would be affected by excessive speed in an array, the minimum performance requirements must be clearly documented in the design submission.

- **RESULT**

The interface macros, both input and output, use a different worst-case delay multiplier than the internal macros. The nets driven by interface macros use the interface macro worst-case delay multiplier. The nets driven by the internal macros use the internal macro worst-case delay multiplier.

To find path propagation delay, first, add the intrinsic (Tpdinterface) and extrinsic (tex-interface) delays of the interface macros for the path and multiply the sum by the correct interface worst-case delay multiplier (WCMinterface).

Second, total the intrinsic (Tpdinternal) and extrinsic (tex-internal) delays for all internal macros in the path and multiply the sum by the proper internal worst-case delay multiplication factor (WCMinternal). Sum this result with the one found for the interface macros to find the total path propagation delay.

Refer to Section 4 for external set-up and hold time analysis equations.

$$t_{path} = WCM_{Interface} \bullet (Tpd_{Interface} + tex_{Interface}) + WCM_{Internal} \bullet (Tpd_{Internal} + tex_{Internal})$$

where

$Tpd_{Interface}$ = sum of all interface macro Tpd delays

$tex_{Interface}$ = sum of all extrinsic net delays for nets driven by interface macros

$Tpd_{Internal}$ = sum of all internal macro Tpd delays

$tex_{Internal}$ = sum of all extrinsic net delays for nets driven by internal macros

$WCM_{Interface}$ = the worst-case delay multiplier for the interface macros and the nets they drive

$WCM_{Internal}$ = the worst-case delay multiplier for the internal macros and the nets they drive

ASYMMETRY IN THE WORST-CASE PATH

Each potentially critical path must be evaluated for worst-case conditions. Both the propagation delay of a rising edge input signal and that of a falling edge input signal must be computed and compared for pulse stretch and pulse shrink. For multiple-input macros, the worst-case specification may be with one or more inputs switching or not. The worst potential circuit behavior represented by the macro specifications must be reviewed.

Minimum pulse-width requirements must be verified and the minimum path delay adjusted as necessary to meet these requirements.

In some cases the minimum delay may be the worst case. AMCC MacroMatrix releases contain the NOMINAL, MAXIMUM-MILITARY, MAXIMUM-COMMERCIAL (COM5), MAXIMUM-COMMERCIAL (COM4) and MINIMUM timing libraries for the array series.

AMCC design submission requirements include the simulation of the circuit for both the maximum worst-case (MIL, COM4 or COM5) and the minimum worst-case for functional, at-speed and AC test simulations.

It is up to the designer to provide simulation vectors that will exercise the correct worst-case conditions for the macros in the critical path, whether it is for one input on a macro switching and the others remaining constant or for multiple simultaneously-switching inputs on a macro.

If there is a difference in the functional or AC test simulation results between the maximum and the minimum worst-case timing, hazard and race conditions are indicated and must be evaluated.

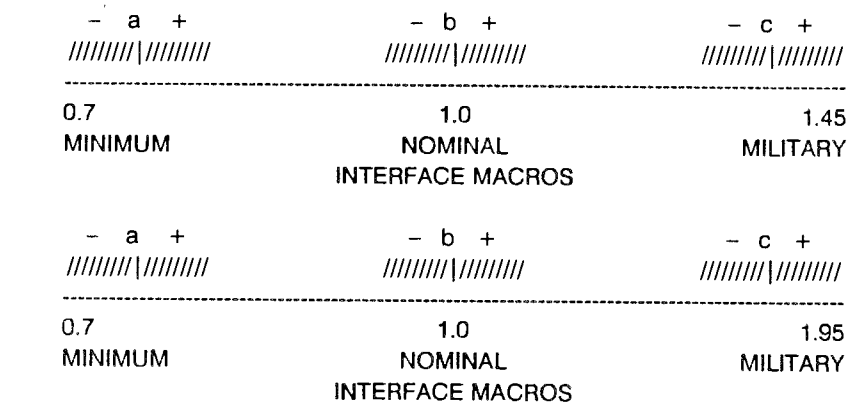
INTERNAL SIGNAL TRACKING GUIDELINE

Many factors affect the signal delay tracking within the array. These factors include such things as relative position within the device, process variations, power supply variations, operating temperature and the characteristics of the various macros. The following may be used as a guideline when signal tracking is being estimated.

In BiCMOS, for interface macros, a "like structure" is defined as a similar macro type with the same option and fan-out load limits. For internal macros on Basic cells, the macros must actually be identical to be considered a "like structure".

- For like structures, for the same edge (both rising or both falling), and with placement on adjacent rows or cells within a quadrant, the tracking will be ± 2.5%.
- For like structures, for the same edge (both rising or both falling), and with a random placement, the tracking will be ± 5%.
- For unlike structures, for the same edge (both rising and falling), and with a random placement, the tracking will be ± 10%. (See Table 3-4.)

EXAMPLE OF TRACKING FOR THREE OPERATING CONDITIONS:



From the diagram, for unlike structures, 1.1 * c = 1.45 for an interface macro, 1.1 * c = 1.95 for an internal macro.

SIGNAL BALANCING; DISTORTION MINIMIZATION

The case where two paths are required to be identical in performance is common. The best results are obtained when the macros are identical macros and are identically loaded, including wire load. Since placement cannot be assumed to be able to solve all problems in all cases, the judicious use of parallel structures (such as buffer trees) to reduce loading in a path and the use of pulse distortion minimization techniques, such as inversion of the signal at each macro, will help.

For ECL output operation at 100MHz and above, pulse distortion minimization methods should be used. These include: 1) signal inversion on alternating macros; 2) short interconnect, a function of fan-out and metal length; and 3) balanced rising-edge and falling-edge k-factors.

The final analysis for pulse stretch and shrink and balanced path delays must be performed using Back-Annotation.

MAXIMUM OPERATING FREQUENCY

The Q14000 Series is capable of supporting high I/O switching rates. The following is a summary of I/O and internal logic performance capabilities:

TABLE 3-6
MAXIMUM OPERATING FREQUENCY
PULSE WIDTH GUIDELINES
Q14000 SERIES BiCMOS ARRAYS

TYPE OF I/O:		COM MHz	COM PW-ns	MIL MHz	MIL PW-ns
TTL INPUT	S-OPTION	65	7.69	60	8.33
	L-OPTION	35	14.28	30	16.66
	H-OPTION	90	5.55	85	5.88
TTL OUTPUT	S-OPTION	50	10.00	45	11.11
(20mA)	H-OPTION	65	7.69	60	8.33
TTL OUTPUT	L-OPTION	35	14.28	30	16.66
(8mA)					
ECL INPUT	S-OPTION	110	4.54	100	5.00
	H-OPTION	180	2.77	165	3.02
ECL OUTPUT	S-OPTION	110	4.54	100	5.00
	H-OPTION	180	2.77	165	3.02

INTERNAL MACROS

TYPE	COM5 MHz	COM4 MHz	COM5 PW-ns	COM4 PW-ns	MILITARY MHz	MILITARY PW-ns
F/F FAST	180*	180	2.40	2.40	165	3.02
F/F SLOW	174	154	2.86	3.23	138	3.62
OTHER	165	146	3.02	3.41	130	3.84

* limited by maximum driver frequency

TTL macros operating above 50MHz and ECL macros operating above 100MHz should be documented on AMCCIO.LST via the AMCCANN user interface.

Flip/flop, latch, counter and shift register documentation includes typical pulse width specifications. Pulse width is computed based on a 50% duty cycle. Selected MSI macros (those with flip/flops or latches with feedback paths) also carry specifications for maximum operating frequency.

To achieve the maximum toggle frequency for the fast flip/flops, they must be directly driven by ECL interface macros.

Note: For macros other than flip/flops and latches, there are no timing errors generated by the timing analysis programs when a Q14000 macro is driven faster than its specified toggle frequency or when its minimum pulse width specification is violated. The most common violation is the use of L-option macros in paths that are operating above 35MHz.

FRONT-ANNOTATION LOAD UNITS

The Front-Annotation statistical wire load unit table was calculated using the following:

$$LU = a * (\text{fan-out loads})^{b}$$

TABLE 3-7
FRONT-ANNOTATION LOAD UNITS

	Q2100B	Q6000B	Q9100B	Q14000B
a	1.00	1.10	1.18	1.20
b	0.66	0.80	0.90	0.92

The Front-Annotation delay files are derived using this data.

BACK-ANNOTATION LOAD UNITS

The Back-Annotation delay files are derived using the following:

TABLE 3-8
BACK-ANNOTATION DELAY METAL LOAD UNITS

		LU/mm	
Q9100B,Q2100B:	first layer metal	1.20	C1
	second layer metal	3.00	C2
Q14000B, Q6000B:	third layer metal	2.0	C3
	second layer metal	3.0	C2

Q9100B, Q2100B:

$$LU = \frac{M1 * C1 + M2 * C2}{1000}$$

Q14000B, Q6000B:

$$LU = \frac{M3 * C3 + M2 * C2}{1000}$$

M1 = length of metal 1 in microns
M2 = length of metal 2 in microns
M3 = length of metal 3 in microns

Differences between the Front-Annotation simulations performed at the customer's site and the Back-Annotation simulations performed at AMCC include the differences between the estimated net delay due to estimated metal length and the actual delay due to actual metal length. Differences between the release macro library and the internal macro library at AMCC may also exist due to on-going development and refinement of the library. AMCC will perform Back-Annotation simulations using the internal library.

PREVENTING HOLD VIOLATIONS DUE TO CLOCK SKEW

INTRODUCTION

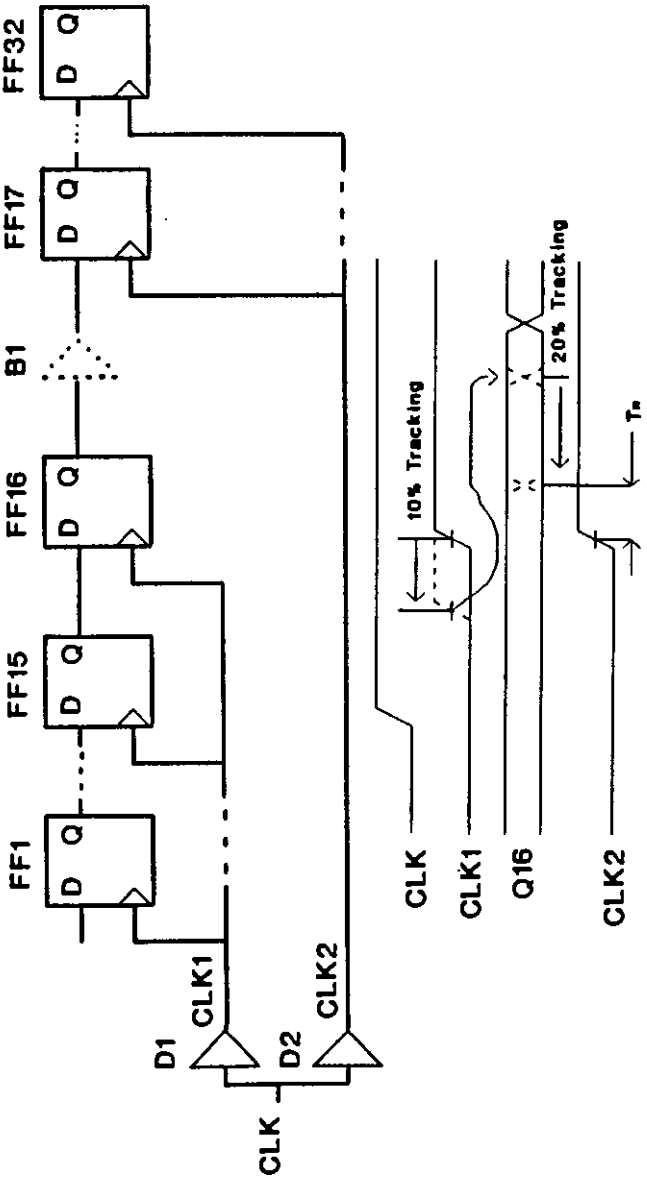
Hold Time violations are a concern wherever 2 storage elements interface with each other, and are clocked by different drivers. Any multiple clock organization or clock distribution tree is subject to this design hazard. The error typically shows up when the Q output of one F/F directly feeds the D input of another.

If the clock to the second F/F is delayed due to tracking or skew, the D input will change during the set-up/hold window. This can easily be avoided by using the guidelines and design checks described below.

HOLD TIME CONSIDERATIONS

Figure 3-A-1 shows a typical 32-Bit shift register being driven by two clocks. Virtually no considerations are needed to maintain hold time when the Q output and D input are on flip/flops that are driven by the same clock net, i.e., FF15/FF16 driven by CLK1.

If the clocks are different as in FF16/FF17, two paths need to be analyzed to determine if the required hold time has been satisfied. Path 1 flows through macros D1 and FF16 (CLK to Q) to the D input of FF17, while Path 2 is through D2 to the clock input of FF17. Differences in tracking, fan-out and metal lengths between the paths can be significant and cause enough delay in Path 2 to create a hold time error.



32-Bit Shift Register Driven by Two CLocks

$$M * [0.9 * Tpd_{D1} + 0.8 * Tpd_{FF16} - Tpd_{D2}] \geq Th_{FF17}$$

FIGURE 3-A-1

Two options are available to overcome the problem:

1. Add 1 or more gates in Path 1 to offset the delay. Generally, a single gate as shown in Figure 3-A-1 (B1) will suffice.

2. Minimize the differences to an acceptable level through macro selection, placement, load balancing and reduced metal lengths as follows.

* Use identical clock driver macros to improve tracking.

* Balance the clock fan-out loading (L_{fo}) to within 10%.

* Balance the clock loads (fan-out + metal) ($L_{fo} + L_{net}$) to within 30%.

* Add a buffer if computation still shows hold time violation

DESIGN CHECK

To compute the hold time of the design, the propagation delay of both paths needs to be determined while factoring in the effects of tracking.

For Like edges:

- If they are placed on adjacent cells on the same row or column, a 5% tracking should be used.

- If the two drivers are of the same macro type and they are placed within the same quadrant, a tracking of 10% should be used.

- If they are not the same macro but are placed within the same quadrant, 20% tracking should be used.

For unlike edges:

- If unlike edges and unlike structures but placed within the same quadrant, 20% tracking should be used.

Other placement options are not recommended.

Note: It is unlikely that two paths whose tracking in relation to each other is of concern, would be placed in different quadrants.

The worst-case tracking direction is to reduce the path propagation delay of both D1 and FF16 by the indicated amount. This includes both the intrinsic and extrinsic delays.

The general equation for the example is as follows:

$$WCMmax * [TRK_1 * Tpd_{D1} + TRK_2 * Tpd_{FF16} - Tpd_{D2}] > Th_{FF17}$$

The TRK_1 tracking factor applies to D1 in the example and is 0.9. This assumes identical driver macros that are placed within the same chip quadrent (10% tracking). For other options, this should be changed to 0.95 (5% tracking) or 0.8 (20% tracking) as applicable.

The TRK_2 tracking factor applies to FF16. In the example, FF16 should use a 20% tracking to account for the unlike edges and unlike structures between FF16 and D2. This assumes that the two macros (D2 and FF16) are both placed within the same chip quadrant.

The computation should be tested at the AMCC minimum test condition (WCMmax = 0.86) if the expression within the brackets results in a positive number. If the result is negative, then the worst-case maximum operating condition needs to be tested (WCMmax = 1.35 for Commercial, or 1.45 for Mil).

For the example, for a MILITARY circuit, the equation becomes:

$$0.86 * [0.9 * Tpd_{D1} + 0.8 * Tpd_{FF16} - Tpd_{D2}] > Th_{FF17}$$

or

$$1.45 * [0.9 * Tpd_{D1} + 0.8 * Tpd_{FF16} - Tpd_{D2}] > Th_{FF17}$$

whichever is worse.

Note: While success can be estimated using Front-Annotation, final calculations must be made after Back-Annotation using the actual metal delays. The layout and/or design must be changed if the appropriate test fails.

Section 4:

External Tsu, Th

EXTERNAL SET-UP and HOLD TIMES

When the input to the data or the clock or both pins on a flip/flop or a latch are supplied from an external signal, then the external set-up and hold times must be computed. The computations must be for worst-case and account for processing skew.

To meet design submission requirements, both the maximum worst- case (1.45, 1.95, etc.) and the minimum worst-case (0.70) equations may need to be computed to determine the worst-case window for external set-up and hold times. Both rising edge and falling edge input path propagation must be evaluated. For deeply-nested paths, consult AMCC applications.

Table 4-1 provides the external set-up and hold equations for the Q14000 BiCMOS Series Arrays for four defined operating conditions, MIL, COM5, COM4 and MIN. The equations are based on the 20% variation in on-chip signal variation discussed earlier in this design manual.

Figure 4-1 illustrates the delay paths. Table 4-2 provides the definitions for the terms used in the text, the equations and in the figure. For the worst-case multipliers, see Table 3-4.

For the BiCMOS arrays, the data and clock paths are broken down into the interface macro and its net (t_{DInput} or t_{CInput}) and the internal macros and the nets they drive (t_D or t_C). See Table 4- 2.

Results computed or derived from simulations using Front-Annotation data cannot be considered as the circuit specification.

SET-UP TIME - GENERIC EQUATION

When computing the set-up time, it is desirable to assume that the data propagation path delay is the worst-case maximum and that the clock path propagation delay is a worst-case minimum for the operating conditions. The generic equation is:

$$t_{su_{external}} = WCMmax * (t_D + Tsu_{macro}) - WCMmin * t_C$$

For the Q14000 Series and its dual multipliers, the equation becomes:

$$t_{su_{external}} = WCMmax_{interface} * t_{Dinput} + WCMmax_{core} * t_D - WCMmin_{interface} * t_{Cinput} - WCMmin_{core} * t_C + WCMmax_{core} * T_{su\ (macro)}$$

Use the MILITARY or COMMERCIAL equations for set-up time when
$t_D + t_{Dinput} - 0.82 * (t_C + t_{Cinput}) \geq 0$.

Use the MINIMUM equations for set-up time when
$t_D + t_{Dinput} - 0.82 * (t_C + t_{Cinput}) < 0$.

HOLD TIME - GENERIC EQUATION

When computing the hold time, it is desirable to assume that the data propagation path delay is the worst-case minimum and that the clock path propagation delay is a worst-case maximum for the operating conditions. The generic equation is:

$$th_{external} = WCMmax * (t_C + Th_{macro}) - WCMmin * t_D$$

For the Q14000 Series and its dual multipliers, the equation becomes:

$$th_{external} = WCMmax_{interface} * t_{Cinput} + WCMmax_{core} * t_C - WCMmin_{interface} * t_{Dinput} - WCMmin_{core} * t_D + WCMmax_{core} * T_{h\,(macro)}$$

Use the MILITARY or COMMERCIAL equations for hold time when
$t_C + t_{Cinput} - 0.82 * (t_D + t_{Dinput}) \geq 0$.

Use the MINIMUM equations for hold time when
$t_C + t_{Cinput} - 0.82 * (t_D + t_{Dinput}) < 0$.

TABLE 4-1
SET-UP AND HOLD EQUATIONS - BiCMOS Q14000 SERIES ARRAYS
Q9100B and Q2100B ARRAYS

MILITARY OPERATING RANGE	$t_{SU_{external}}$ =	1.45 • t_{Dinput} + 1.95 • t_D – 1.19 • t_{Cinput} – 1.59 • t_C + 1.95 • T_{su} (*macro*)
	$t_{h_{external}}$ =	1.45 • t_{Cinput} + 1.95 • t_C – 1.19 • t_{Dinput} – 1.59 • t_D + 1.95 • T_h (*macro*)
COMMERCIAL OPERATING RANGE	$t_{SU_{external}}$ =	1.35 • t_{Dinput} + 1.55 • t_D – 1.11 • t_{Cinput} – 1.27 • t_C + 1.55 • T_{su} (*macro*)
COM 5	$t_{h_{external}}$ =	1.35 • t_{Cinput} + 1.55 • t_C – 1.11 • t_{Dinput} – 1.27 • t_D + 1.55 • T_h (*macro*)
COMMERCIAL OPERATING RANGE	$t_{SU_{external}}$ =	1.35 • t_{Dinput} + 1.75 • t_D – 1.11 • t_{Cinput} – 1.43 • t_C + 1.75 • T_{su} (*macro*)
COM 4	$t_{h_{external}}$ =	1.35 • t_{Cinput} + 1.75 • t_C – 1.11 • t_{Dinput} – 1.43 • t_D + 1.75 • T_h (*macro*)
MINIMUM OPERATING RANGE	$t_{SU_{external}}$ =	0.86 • (t_D + t_{Dinput}) – 0.70 • (t_C + t_{Cinput}) + 0.86 • T_{su} (*macro*)
	$t_{h_{external}}$ =	0.86 • (t_C + t_{Cinput}) – 0.70 • (t_D + t_{Dinput}) + 0.86 • T_h (*macro*)

TABLE 4-1 Continued
SET-UP AND HOLD EQUATIONS - BiCMOS Q14000 SERIES ARRAYS
Q14000B and Q6000B ARRAYS

MILITARY OPERATING RANGE	$t_{SU_{external}}$ =	$1.70 * t_{Dinput} + 1.95 * t_D - 1.40 * t_{Cinput} - 1.59 * t_C + 1.95 * T_{su\ (macro)}$
	$t_{h_{external}}$ =	$1.70 * t_{Cinput} + 1.95 * t_C - 1.40 * t_{Dinput} - 1.59 * t_D + 1.95 * T_{h\ (macro)}$
COMMERCIAL OPERATING RANGE	$t_{SU_{external}}$ =	$1.55 * t_{Dinput} + 1.55 * t_D - 1.27 * t_{Cinput} - 1.27 * t_C + 1.55 * T_{su\ (macro)}$
COM 5	$t_{h_{external}}$ =	$1.55 * t_{Cinput} + 1.55 * t_C - 1.27 * t_{Dinput} - 1.27 * t_D + 1.55 * T_{h\ (macro)}$
COMMERCIAL OPERATING RANGE	$t_{SU_{external}}$ =	$1.55 * t_{Dinput} + 1.75 * t_D - 1.27 * t_{Cinput} - 1.43 * t_C + 1.75 * T_{su\ (macro)}$
COM 4	$t_{h_{external}}$ =	$1.55 * t_{Cinput} + 1.75 * t_C - 1.27 * t_{Dinput} - 1.43 * t_D + 1.75 * T_{h\ (macro)}$
MINIMUM OPERATING RANGE	$t_{SU_{external}}$ =	$0.86 * (t_D + t_{Dinput}) - 0.70 * (t_C + t_{Cinput}) + 0.86 * T_{su\ (macro)}$
	$t_{h_{external}}$ =	$0.86 * (t_C + t_{Cinput}) - 0.70 * (t_D + t_{Dinput}) + 0.86 * T_{h\ (macro)}$

TABLE 4-2
TERMINOLOGY DEFINITIONS

Defining a "memory macro" as a latch, a flip/flop or an MSI containing one or the other, the terms used in the equations are defined in Table 4-2.

t_D = NOMINAL data path propagation delay from the circuit input and up to the memory macro data input pin; EXCLUDING the interface macro intrinsic delay and the extrinsic net delay for the net driven by the interface macro, computed using Front-Annotation methodology prior to layout, Back-Annotation after layout.

t_{DInput} = NOMINAL delay due to interface macro intrinsic delay on data path plus the extrinsic net delay for the net driven by the interface macro, computed using Front-Annotation methodology prior to layout, Back-Annotation after layout.

t_C = NOMINAL clock path propagation delay from the circuit input and up to the memory macro clock input pin; EXCLUDING the interface macro intrinsic delay and the extrinsic net delay for the net driven by the interface macro, computed using Front-Annotation methodology prior to layout, Back-Annotation after layout.

t_{CInput} = NOMINAL delay due to interface macro intrinsic delay on clock path plus the extrinsic net delay for the net driven by the interface macro, computed using Front-Annotation methodology prior to layout, Back-Annotation after layout.

Tsu_{macro} = Tsu as specified in Section 6 (specified as typical)

Th_{macro} = Th as specified in Section 6 (specified as typical)

The specific worst-case multipliers (WCMmax and WCMmin) are based on the operating conditions and the type of macro involved. The bipolar interface macros use one multiplier and the CMOS core uses another.

WCMmax = MILmax, COM4max, COM5max, or MINmax
WCMmin = MILmin, COM4min, COM5min or MINmin
See Table 3-4

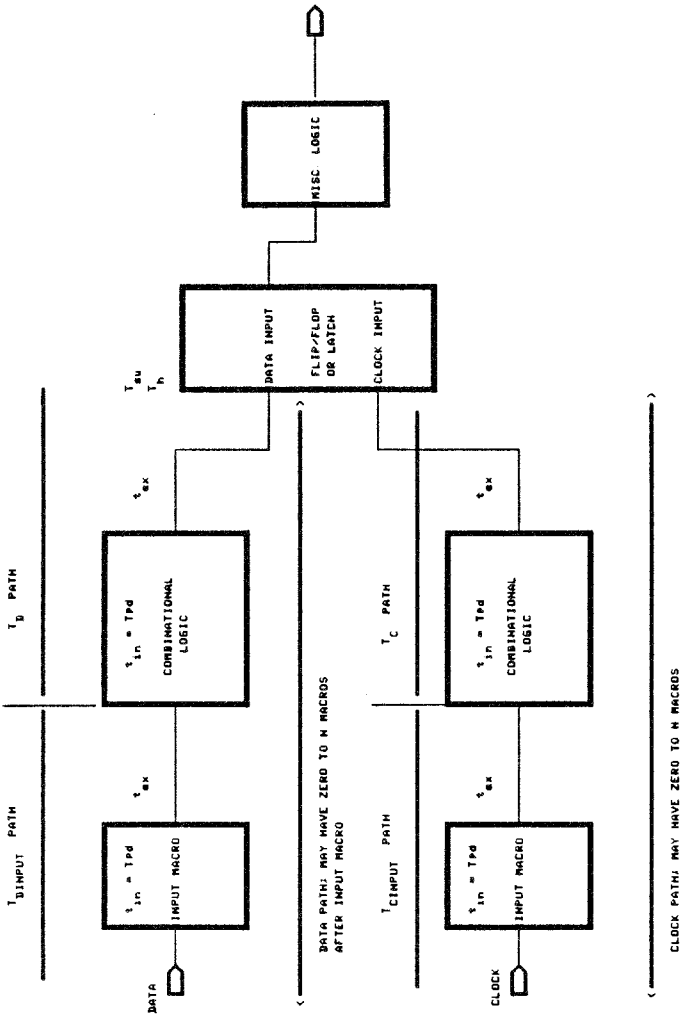

MISC LOGIC
DATA INPUT
FLIP/FLOP OR LATCH
CLOCK INPUT
T_{su}
T_h
T_D PATH
T_C PATH
T_{DINPUT} PATH
T_{CINPUT} PATH
t_{ex}
t_{in} = Tpd
COMBINATIONAL LOGIC
INPUT MACRO
DATA
CLOCK
DATA PATHS MAY HAVE ZERO TO N MACROS AFTER INPUT MACRO
CLOCK PATHS MAY HAVE ZERO TO N MACROS AFTER INPUT MACRO

FIGURE 4-1

Section 5:

Power/Packaging

INTRODUCTION

The **TOTAL** current (internal cells and I/O interface cells) is used to compute the worst-case power dissipated by the logic array. The worst-case power as it relates to junction temperature is used to examine the packaging and the heat-sink requirements of the final product.

The total current is a function of the interface macros used, the options selected for those macros, the overhead current, which is e function of the array chosen, the output terminations and the frequency of operation, which determines the AC current used by the internal macros. The total worst-case current for interface macros and overhead is found by using the correct worst-case current multiplier for the product grade (MILITARY or COMMERCIAL).

The total power dissipated by a device is a function of the total worst-case interface and overhead current, the worst-case power supply, the ECL terminations, and the power dissipated by the internal macros.

In addition to a straight-forward computation, the designer should review the following sections if applicable to the circuit under design:

- For some interface macros (es defined in Section 6, Macro Library documentation), tha current is state-dependent. See Compute State Dependent Current.

- For the Q14000B and Q6000B, overhead current is programmable. Refer to "Q14000B, Q6000B Typical Overhead Current" in this section.

PART 1: INTERFACE MACRO POWER DISSIPATION

MACRO OCCURRENCE TABLE - INTERFACE MACROS

A macro occurrence table can be constructed prior to design capture to assist in the computation of interface current and power dissipation. A macro occurrence table should provide the following data when complete:

TABLE 5-1
INTERFACE MACRO POWER COMPUTATION

- A list of the different interface macros used differentiated by option;
- The number of times (n) each macro appears on the schematics;
- The current (adjusted for state-dependence) I_{CC} and/or I_{EE} for one instance of the macro
- The total currant due to the n occurrences of each macro;
- The sums of the I_{CC} and I_{EE} currents;
- The overhead currents based on the I/O mode and the spacific array; (For Q14000B, Q6000B; sae Appendix 5-A); both I_{CC} and I_{EE} components
- The sum of the macro and overhead currents into total I_{CC} and total I_{EE};
- The correct worst-case current multiplier for the product grada (military of commercial);
- The total worst-case I_{CC} and I_{EE} currents;
- The worst-case voltages, $V_{CC_{wc}}$ and $V_{EE_{wc}}$;
- The product of the worst-case current and the worst-case voltages for P_{CC} and P_{EE};
- The computation for any ECL outputs:

$$P_{EO} = 1.3 \cdot I_{termination} \cdot \begin{matrix}\text{number of macros} \\ \text{with the same drive}\end{matrix}$$

- The final sum of all three:

$$P_{DC} = P_{CC} + P_{EE} + P_{EO}$$

This table is provided for a captured circuit by the AMCC MacroMatrix Macro Occurrence ERC.

FIGURE 5-1

```
**********************************************************************
*          MACRO OCCURRENCE AND POWER DISSIPATION                    *
*          VERSION 3.00                                              *
**********************************************************************
```

Path Name /USER/CLASS/Q14QUICK
Product Name PRODUCTNAME
Circuit family Q14000
Circuit technology E
Date 14 DEC 1988
Time 12:48
Product Grade MIL

PARTIAL LIST

No errors found.

MACRO NAME	# USED	SPECS		TOTALS	
		ICC mA	IEE mA	ICC mA	IEE mA
IE23	1	0.00	1.58	0.00	1.58
IE23H	1	0.00	2.35	0.00	2.35
IE25	1	0.00	4.05	0.00	4.05
IE25H	1	0.00	4.85	0.00	4.85
IEVCC	1	0.00	0.00	0.00	0.00
IT12H	1	3.20	0.00	3.20	0.00
...	...	...	...	...	...
ITGND	1	0.00	0.00	0.00	0.00
ITPWR	1	0.00	0.00	0.00	0.00
OE10	1	0.00	5.45	0.00	5.45
...	...	...	...	...	...
OE70	1	0.00	5.30	0.00	5.30
OK70	1	0.00	5.30	0.00	5.30
OT21H	1	2.00	0.00	2.00	0.00
OT24	1	2.67	0.00	2.67	0.00
UE49	1	0.00	7.65	0.00	7.65
UE49H	1	0.00	8.20	0.00	8.20
UT27	1	7.30	0.00	7.30	0.00
UT27H	1	9.35	0.00	9.35	0.00

	ICC mA	IEE mA
TOTAL TYPICAL MACRO CURRENT mA	39.94	61.94
TOTAL TYPICAL POWERED DOWN CURRENT mA	0.00	0.00
TOTAL TYPICAL OVERHEAD CURRENT mA	0.00	121.00
TOTAL TYPICAL CURRENT mA	39.94	182.94
TOTAL MAX CURRENT mA (TYP CURRENT TIMES 1.54) =	61.51	281.73
WORST CASE POWER DISSIPATION VCC (5.5)V X (61.5076)mA/1000 VEE (4.8)V X (281.727)mA/1000 ECL OUTPUT POWER DISSIPATION (14.0)mA X 1.3V X (6)outputs/1000 TOTAL POWER DISSIPATION		0.34 WATTS 1.35 WATTS 0.11 WATTS 1.80 WATTS

COMPUTING THE MAXIMUM WORST CASE POWER - INTERFACE MACROS

To compute the worst-case power, perform the following steps.

- **SELECT THE MACRO OPTION - INTERFACE MACROS**

Meny of the interfece macros for the Q14000 Series come with options. The L-option macros are slower then the S-option macros. They heve a lower fan-out load capability, lower maximum frequency of operation end lower dissipated current. The H-option macros are faster than the S-option macros and heve higher dissipated current. S- end H-option mecros drive the same loads. See Section 6 index for a list of the interface macros and their options.

During design, H-option macros, high fan-out drivers and other high-current interface macros should be used judiciously to avoid unnecessary high current/power dissipation. The use of L-option macros when available can help balance the use of high- current macros providing speed/power programmability if and only if the minimum pulse widths are not violated.

To estimate power prior to schematic capture, create a macro occurrence table of all interface macros used differentiated by option and list the current dissipeted by each. Keep I_{CC} and I_{EE} currents separate.

- **COMPUTE THE STATE DEPENDENT CURRENT**

The I_{CC} and I_{EE} values for many of the interface macros are specified for HIGH and LOW input. Bidirectionals are specified for enabled and disabled states.

To compute actual power for any given state of the circuit, the state and operating duty cycle of each I/O would have to be known, requiring a detailed vector analysis.

Without specific and unique operating duty cycles, the following procedure is recommended:

- For 2-state outputs (HIGH, LOW), calculate I_{EE} and I_{CC} as the average of the two values (50% HIGH, 50% LOW).

- For 3-state outputs (HIGH, LOW, Z or INPUT) calculate as 50% disabled high impedance Z state or input mode, 25% enabled HIGH and 25% enabled LOW.

- **COMPUTE THE TOTAL TYPICAL INTERFACE MACRO CURRENT**

Compute the total current used by all occurrences of each macro and sum these totals to find:

SUM OF MACROS I_{CC} CURRENT
SUM OF MACROS I_{EE} CURRENT

Unless the circuit uses a single-power supply these two sums must be kept separate.

- **ADD THE TYPICAL OVERHEAD CURRENT - Q9100B, Q2100B**

The overhead current is the base array current dissipated by the internal regulators, reference generators, selected I/O mode (TTL, ECL, MIXED), and power supply configuration (+5V, -5.2V, dual supply or other). The overhead current for the array is specified in the Overhead Current table. (Refer to Table 5-2.) The table is accessed by array and I/O mode.

Add the overhead current to the appropriate macro current sum already computed:

$$\text{TOTAL } I_{CC} = \text{SUM OF MACROS } I_{CC} + I_{CC_{OVERHEAD}}$$
$$\text{TOTAL } I_{EE} = \text{SUM OF MACROS } I_{EE} + I_{EE_{OVERHEAD}}$$

TABLE 5-2
Q14000 SERIES TYPICAL OVERHEAD CURRENT (mA)

ARRAY ↓	TTL MODE I_{CC},mA	ECL MODE I_{EE},mA	MIXED MODE I_{EE}/I_{CC},mA	+5V REF ECL/TTL I_{CC},mA
Q14000B	12	133*	133*/12	145*
Q9100B	18	96	96/22	118
Q6000B	12	133*	133*/12	145*
Q2100B	16	70	70/20	92

* For the Q14000B and Q6000B, the ECL overhead current is programmable, i.e., will depend on the final placement. These numbers represent the worst-case, - the case where all VRB and VTA10K or all VRB and VTA100K generators are required.

- **ADD THE TYPICAL OVERHEAD CURRENT WITH WORST-CASE USAGE ASSUMED**
  - Q14000B, Q6000B

Table 5-2 provides overhead current for the Q14000B and Q6000B under the assumption that all threshold generators for that I/O mode are in use. Since there is programmable power-down of those generators that are not required, this is the highest overhead current possible. Actual power-down is not known until place and route are successfully completed.

To refine the estimate or to compute expected actuals based on preplacement, refer to Appendix 5-A.

- **MULTIPLY BY THE WORST-CASE CURRENT MULTIPLIER (WCCM) TO FIND THE WORST-CASE CURRENT**
  - INTERFACE MACROS

Multiply the results by the appropriate worst-case current multiplier to obtain the worst-case I_{CC} ($I_{CC_{wc}}$) and worst-case I_{EE} ($I_{EE_{wc}}$) current.

$$I_{CC_{wc}} = \text{TOTAL } I_{CC} \cdot \text{WCCM}$$
$$I_{EE_{wc}} = \text{TOTAL } I_{EE} \cdot \text{WCCM}$$

For the Q14000 Series, the worst-case current multiplier, WCCM, is **1.54** for MILITARY and **1.35** for COMMERCIAL grade circuits. The worst-case current multiplier is used to compute the worst-case values for all specified interface macro currents and overhead currents.

TABLE 5-3 WORST-CASE CURRENT MULTIPLIER		
	Q9100B Q2100B	Q14000B Q6000B
MILITARY	1.54	1.54
COMMERCIAL	1.35	1.35

- **MULTIPLY BY THE WORST-CASE VOLTAGE**

The worst-case voltage is dependent on whether the circuit is COMMERCIAL or MILITARY. The typical variation is shown in Table 5-3. For COMMERCIAL circuits, with a –5.2V or a +5V supply, the voltage variation is usually ±5%. For COMMERCIAL circuits using V_{EE} = –4.2V, the variation is ±7%.

For MILITARY circuits, the voltage variation is usually ±10%. Note the worst-case voltage for the –4.5V supply as listed in Table 5-4 and on the data sheet, where –4.5V supply varies ±7%. The worst-case voltage in this case is –4.8V for MILITARY or COMMERCIAL.

TABLE 5-4 WORST-CASE VOLTAGE		
NOMINAL	COMMERCIAL	MILITARY
+5.0V –5.2V –4.5V	+5.25V –5.46V –4.8V	+5.5V –5.72V –4.8V

Multiply the worst-case current by the appropriate worst-case voltage:

$$P_{EE} + I_{EE_{wc}} \cdot V_{EE_{wo}}$$
$$P_{CC} + I_{CC_{wc}} \cdot V_{CC_{wo}}$$

- **ECL STATIC POWER P_{EO}**

The equation used by the AMCC MacroMatrix ERC software to compute ECL static power dissipation for ECL outputs is:

$$P_{EO} = XXmA \cdot 1.3V \cdot NUMBER\_OF\_ECL\_OUTPUTS$$

where XX is the current based on the termination.

The 1.3V term represents the average between V_{OH} and V_{OL}. This is considered to be the statistical worst-case for this function.

If there is more than one termination, the power for each is computed and summed to find the total $P_{ECL_{outputs}}$.

- **ECL OUTPUT TERMINATION CURRENT**

Table 5-5 provides the ECL output termination currents used by the AMCC MacroMatrix ERC software. The currents shown are the average current (average of I_{OH} and I_{OL}) and represent 50% terminations active.

TABLE 5-5
ECL 10K/100K TERMINATION CURRENT

TERMINATION:	CURRENT:	STANDARD MACRO:	ADJUST POWER COMPUTATION:
25 ohm	28.0 mA	NO	YES
50 ohm	14.0 mA	YES	NO
100 ohm	7.0 mA	NO	YES
200 ohm	3.5 mA	NO	YES

* the average current (average of I_{OH} and I_{OL}) for termination to –2V

- **WHEN 50 OHM OR 25 OHM TERMINATIONS NOT USED**

If other ECL output load resistances are used, the actual current value must be computed for use in this equetion. For a -2V termination, to find the average current in mA use:

$$I_{In\ mA} = \frac{0.7}{R * (10^{-3})} \quad \text{for any R}$$

For the Q14000 Series arrays, the macro occurrence ERC uses either a 50 ohm or a 25 ohm to -2V termination, depending on the macro.

- **WHEN $V_T \neq -2V$**

For other termination voltages, an adjustment to the power dissipation computation must be made by the designer. For a termination voltage V_T, to find the average current in mA use:

$$I_{In\ mA} = \frac{(-1.3V - V_T)}{R * (10^{-3})} \quad \text{for any R}$$

- **SUM THE RESULT - Total DC power**

Sum the results of the macro computations with any ECL output macro static power dissipation to obtain the total worst-case power dissipation for the interface macros.

$$Pd_{Interface} = P_{CC} + P_{EE} + P_{EO}$$

The result is the total worst-case power dissipated by the interface macros for the circuit on the target array.

MACROMATRIX MACRO OCCURRENCE ERC - INTERFACE MACROS

Currently, MacroMatrix ERC power computations are done with the worst-state current value, assuming the worst "state" at all times for those macro specified with HIGH and LOW or ENABLED and DISABLED current. The power dissipation value computed will be conservative. A manual computation can be made to adjust the current used for these macros.

MacroMatrix ECL Static power is computed with the 50 or 25 ohm termination under the assumption of 50% terminations active. Different termination resistive loads will require manual computation. These loads should be identified via the AMCCANN user-interface and be listed on AMCCIO.LST.

MacroMatrix ERC overhead current for the Q14000B and Q6000B uses the all-available-generators-in-use approach and will be conservative. For circuits with less than 100% I/O utilization, a manual computation is required. Final overhead current values will not be available until place and route are complete and Back-Annotation is approved.

In all of these cases, a manual computation is required if a refinement of the worst-case DC power dissipation produced by the MacroMatrix Macro Occurrence ERC is required.

PART 2: INTERNAL MACRO POWER DISSIPATION

• MACRO OCCURRENCE TABLE - INTERNAL LOGIC

A macro occurrence table for internal logic macros can be constructed prior to design capture to assist in the computation of internal and total circuit current and power dissipation, as well as cell utilization. A macro occurrence table for the internal logic should provide:

- A list of the different macros differentiated by option;
- The number of times each macro appears on the schematics;
- The number of cells used by each macro
- The number of cells due to n occurrences of the macro

The MacroMatrix ERC produces a BiCMOS/Bipolar Power Computation Worksheet which lists macros and their occurrences and which can be used for AC power analysis as well as for cell utilization checking. (See Section 2.)

- **COMPUTING AN ESTIMATE OF INTERNAL CELL POWER DISSIPATION**

The equation used to compute internal cell power dissipation is:

$$P_{internal_{wc}} = F * 0.2 * G * 20 \text{ microwatt/gate–MHz}$$

where: F = the highest frequency in MHz
0.2 = 20% of the gates switching at the maximum frequency of operation
G (internal gate count) = 3 * internal cell count

The internal cell count is the number of Basic cells used by the design. The internal gate count is estimated by multiplying the Basic cell count by 3. The Basic cell count is provided by the MacroMatrix Population ERC report as "SUM_LOGIC". The equation is reduced to:

$$P_{internal_{wc}} = F * \text{Basic Cells} * 12 \text{ microwatt/gate–MHz}$$

This equation provides an estimate of the worst-case power dissipation for the internal macros.

Use the same equation for MILITARY and COMMERCIAL computations.

NOTE: The accuracy of the equation decreases if the macros are partitioned into different frequency groups.

COMPUTING "ACTUAL" INTERNAL CELL POWER DISSIPATION

To compute "actual" internal cell power dissipation, the print-on-change at-speed simulation would need to trece all internal nets, a prohibitively complex exercise. None of the EWS workstations support this computation at this time.

FINAL RESULT

The sum of the estimated total power dissipated by all internal macro frequency groups and the total worst-case power dissipated by the interface macros, including overhead current and all computed refinements, is the total worst-case power dissipated by the BiCMOS circuit.

THERMAL COEFFICIENTS - I/O AREA
Q9100B, Q2100B

The temperature coefficients for the interface (I/O macro) area of the Q9100B and O2100B arrays are shown in Table 5-6.

TABLE 5-6
TEMPERATURE CQEFFICIENTS
BiCMOS ARRAYS

MACRO TYPE:	TCmacro (°C)	
	INPUT	OUTPUT
ECL (ANY SYSTEM)	0.03	0.0
TTL (+5 SYSTEM)	-0.07	-0.3
TTLMIX (DUAL SUPPLY SYSTEM)	-0.10	-0.2

The overall temperature coefficient for the chip I/O area is a weighted average:

$$TC_{chip} = \sum_{\text{all types}} \frac{n * TC_{macro}}{\text{TOTAL NUMBER OF I/O MACROS}}$$

where n = the number of macros of a given type
TC_{macro} = the temperature coefficient for that type

The thermal coefficient is used to derate the I/O current when the temperature is higher or lower than specified. The worst-case current is computed at the maximum temperature for the operating range. Should the part be guaranteed to operate at a lower temperature, then the worst-case interface current may be derated using the temperature coefficient as computed.

PACKAGE SELECTION

Thermal and electrical considerations can affect the selection of the package end heatsink. Package and heatsink selection should always be a consideration from the beginning of the design process. It should be a factor in the initial selection of the array series and the array within the series.

Package selection requires that the designer heve two computations completed: 1) the total maximum worst-case power dissipation; and 2) the total number of I/O signel pads required.

Prior to design start, preliminary estimates should be calculated as part of the feasibility task. Final verification can be performed with reports generated by the AMCC MacroMatrix Design Kit software.

The I/O signal pad count required is provided by the AMCC MacroMatrix ERC software Population Check Report as "SUM_TOTAL_I/O" and is the sum of all signals, all added power and all added ground pads as indicated on the schematics.

From this total, subtract those added power and ground pads that have baen placed to allow connection to the package internal power or ground plane (i.e., those that do not require a pin). If it is possible, AMCC requires placement so that no added power or ground will require a package pin.

Using entries from the ERC Population report:

Signal Pins needed = SUM_TOTAL_IO − number of added power pads with no pins − number of added ground pads with no pins

The ERC checks the number of signals and added power and grounds against the array pad count limit and issues an error if the limits were exceeded.

TABLE 5-7
ARRAY PAD COUNT LIMIT

ARRAY NAME	REQUIRED POWER-GROUND PADS **	CIRCUIT I/O PAD LIMIT	TOTAL EXTERNAL PADS
Q14000B	56	226	282
Q9100B	56	160	216
Q6000B	50	132	182
Q2100B	28	80	108

* ARRAY PAD LIMIT
** FIXED POWER-GROUND PADS; ALL MUST BE USED

AMCC offers an assortment of packages for the Q14000 Series Logic Arrays as shown in Table 5-8. Using the required signal pins count and the array, the matrices below allow the correct package to be selected.

TABLE 5-8
AMCC Q14000 STANDARD PACKAGING MATRIX
SIGNAL/POWER-GROUND MAP

Leaded Chip Carriers	mil ctr	SIGNAL PINS	PWR/GND PINS	Q2100B	Q6000B	Q9100B	Q14000B
84 lead flpk	N/A			x			
100 LDCC	50	80	20	x			
132 LDCC	25	92	40			x	x
172 LDCC	25	TBD	TBD		TBD		
196 LDCC	25	156	40			x	x

Pin Grid Arrays	Cavity up/ down	SIGNAL PINS	PWR/GND PINS	Q2100B	Q6000B	Q9100B	Q14000B
68 PGA	CD	48	20	x			
84 PGA	CD	64	20	x			
100 PGA	CU;CD	TBD	TBD	x	TBD		
169 PGA	CD	132	36		x	x	x
225 PGA	CD	160	52			x	x
301 PGA	CD	226	74				x

If it is assumed that all added power end ground macros were placed to allow internal package plane connection, than tha number of signal pads is equal to the number of I/O signals and this is the number of signal pins required on any packaga being considered for the circuit.

If it is not possible to place all added power and grounds to allow internal package plane connection, then sum all signal pads and all added power and ground pads that must connect to an external package pin. Use this total as the number of signal pins that must be available on a the package for it to be considered as an option for the circuit. Consult with AMCC applications before making a final selection.

COMPUTING THE JUNCTION TEMPERATURE

To ensure that the package and heatsink combination will meet performence requirements, the designer should compute the expected junction temperature for the product grade (MILITARY or COMMERCIAL) based on the specified thermal environment so as not to exceed the maximum allowed junction temperature.

For COMMERCIAL devices, the maximum junction temperature is 130°C. For MILITARY devices, the maximum junction temperature is 150°C.

The thermal resistance between the die junction and the ambient environment depends on several factors: die size, thermal resistance of the package, thermal resistance of the heatsink, the shape of the heatsink, ambient temperature, air flow speed and the direction of the air flow with respect to the package or heatsink fins.

- **COMPUTING JUNCTION TEMPERATURE FOR COMMERCIAL GRADE DEVICES**

To compute the junction temperature for COMMERCIAL grade devices, the designer needs to determine the maximum power dissipation of the die (P_d), the thermal resistance between the die and the ambient environment (θ_{ja}), and the maximum ambient temperature (T_a). The maximum junction temperature is:

$$T_j = (P_d * \theta_{ja}) + T_a$$

With proper thermal management, an ambient temperature T_a = 70°C can be achieved for most applications.

While the computation of P_d hes already been presented in this chapter and T_a is known, the thermal resistance θ_{ja} needs to be determined from the sum of two other thermal resistance specifications: θ_{jc} and θ_{ca}.

θ_{jc} is the thermal resistence between the die junction and the case (package). It is a function of die size, packege construction and material thermal conductivity. Refer to Table 5-9 for θ_{jc} of various package and device combinations.

θ_{ca} is the tharmal resistance betwaen the case (package) end the embient environment. It is a function of the eir flow and the heatsink that are used. Refer to the following pages that describe the heatsink sizes and shapes and provide tables of θ_{ca} for the heatsinks for various air flow rates.

$$\theta_{ja} = \theta_{jc} + \theta_{ca}$$

TABLE 5-9
AMCC STANDARD PACKAGING MATRIX
θ_{jc}/θ_{ja} in°C/W

Leaded Chip Carriers	Q2100B	Q6000B	Q9100B	Q14000B
84 lead flatpack	7/TBS			
100 LDCC 50 mil center	6/TBS			
132 LDCC 25 mil center			4/21	4/21
172 LDCC 25 mil center		TBS/TBS		
196 LDCC 25 mil center			4/21	4/21

100 LDCC does not use internal planes

Pin Grid Arrays**		Q2100B	Q6000B	Q9100B	Q14000B
68 PGA	CD	7/TBS			
84 PGA	CD	6.5/TBS			
100 PGA	CU or CD	6/30	TBS/TBS		
169 PGA	CD		4.5/21	3.5/17	3.5/17
225 PGA	CD			3/17	3/17
301 PGA	CD				3/15

** Size of PGA includes 1 orientation pin
68, 84 and 100 PGA does not use internal planes
θ_{ja} values are specified for a still air environment.
TBS means data not yet available

Compute the correct θ_{ja} to be used in the computation of the junction temperature.

This process can be performed in reverse, solving the first equation for the required θ_{ja} and then solving for the required heatsink(s) and air flow rate that are required.

• COMPUTING JUNCTION TEMPERATURE FOR • MILITARY GRADE DEVICES

To compute the junction temperature for MILITARY devices, the designer needs to determine the maximum power dissipation of the die (P_d), the thermal resistance between tha die and the case (package) (θ_{jc}), and the maximum case temperature (T_c). The maximum junction temperature is:

$$T_j = (P_d * \theta_{jc}) + T_c$$

The maximum ambient temperature T_c is teken as 125°C for most MILITARY applications.

θ_{jc} is supplied in Table 5-9.

If the maximum junction temperature does not exceed 150°C, the designer hes remained within the maximum die temperature specification of AMCC MILITARY arrays.

PLACEMENT

Placement restrictions for dual-cell I/Os, added power and ground disbursement, bidirectional macros, etc. are detailed in the AMCC placement document and in Appendix 5-A following this section. If a preplacement file is being prepared for submission to AMCC, consult AMCC first for the required worksheets (array floorplan), restrictions and file formats.

Note that the Q14000 Series MSI macros are hard macros, i.e., there is only one orientation (along a single row) that is allowed for each.

STANDARD PACKAGES

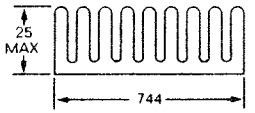
While AMCC prefers that only AMCC-standard packages be used for the Q14000 Series, custom packages can be considered as an individual program basis. Consult your local sales representative or regional sales manager for additional details.

Heatsinks

Table VI
AMCC Standard Heatsinks

DW0045-01
(AAVID PART #61995)

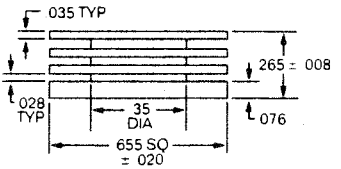
- 1 INCH LONG
- BLACK ANODIZED



θ_{CA} (°C/W)*	AIRFLOW (LFPM)*
10 5	100
7 5	200
5.5	300
4 5	400
3	600
2 5	800
2	900
2	1000

DW0045-02
(THERMALLOY PART #2281C)

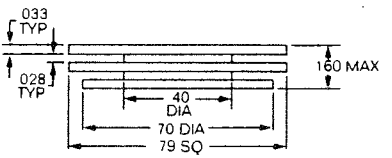
- GOLD CHROMATE FINISH



θ_{CA} (°C/W)*	AIRFLOW (LFPM)*
13 5	100
10	200
8	300
6	400
4	600
4	800
2 5	900
2 5	1000

DW0045-03
(THERMALLOY PART #2286C)

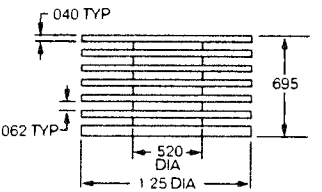
- GOLD CHROMATE FINISH



θ_{CA} (°C/W)*	AIRFLOW (LFPM)*
14	100
10	200
8	300
5 5	400
5	600
4	800
3 5	900
3	1000

DW0045-05
(THERMALLOY PART #2296C)

- GOLD CHROMATE FINISH



θ_{CA} (°C/W)*	AIRFLOW (LFPM)*
7 5	100
4	200
2 5	300
2	400
1	600
1	800
1	900
1	1000

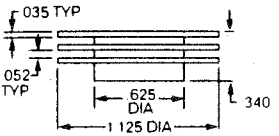
*θ_CA figures are estimates interpolated from Thermalloy heatsink information (tolerances XXX = ± 010 and XX = ± 02) All dimensions in inches For the most current thermal data please consult the factory

AMCC reserves the right to change specifications in any manner without notice

Table VI (cont'd.)

DW0045-06

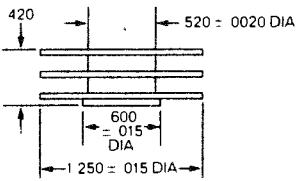
(THERMALLOY PART #16033-1) • GOLD CHROMATE FINISH



θ_{CA} (°C/W)*	AIRFLOW (LFPM)*
10 5	100
6 5	200
4 5	300
4	400
2 5	600
2	800
1 5	900
1 5	1000

DW0045-10

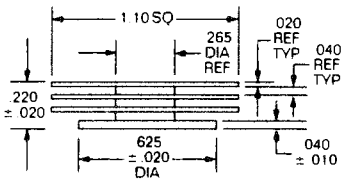
(THERMALLOY PART #2293B) • BLACK ANODIZED



θ_{CA} (°C/W)*	AIRFLOW (LFPM)*
7	100
4 5	200
3 5	300
3	400
2	600
1 5	800
1	900
1	1000

DW0045-12

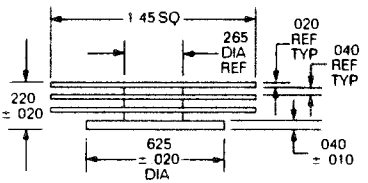
(THERMALLOY PART #17881) • BLACK ANODIZED



θ_{CA} (°C/W)*	AIRFLOW (LFPM)*
12.5	100
9	200
6 5	300
5 5	400
3 5	600
3	800
2 5	900
2 5	1000

DW0045-13

(THERMALLOY PART #17878) • BLACK ANODIZED



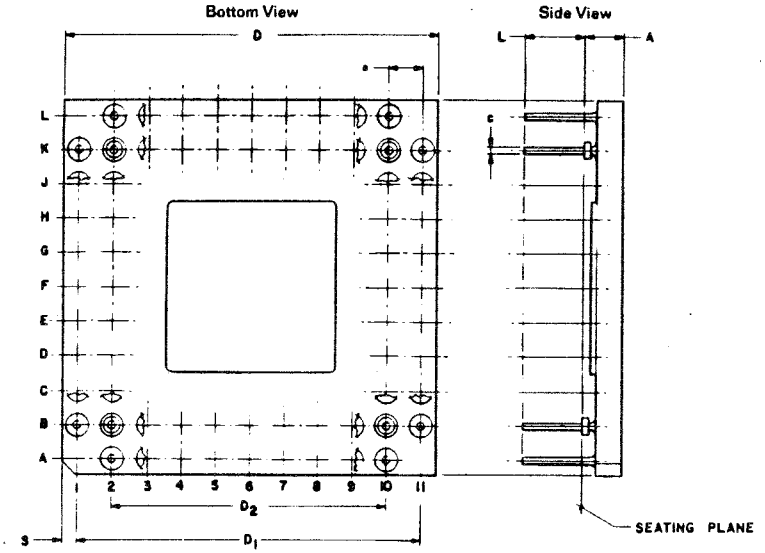
θ_{CA} (°C/W)*	AIRFLOW (LFPM)*
10	100
7 5	200
5	300
4	400
2 5	600
2	800
2	900
1 5	1000

*θ_{CA} figures are estimates interpolated from Thermalloy heatsink information (tolerances XXX = ± 010 and XX = ± 02) All dimensions in inches For the most current thermal data please consult the factory

Leaded Chip Carriers

▪ 68 Pin Grid Array Hermetic Ceramic Package (Cavity Down)

Q5000 Series
Q14000 Series



Sym.	Inches (mm) Max.	Min.
A	150 (3 81)	100 (2 54)
c	020 (0 51)	016 (0 41)
D	1 [illegible] 28 22 [illegible] sq	1 089 (27 66) sq
D_1	1 010 (25 65) sq	990 (25 15) sq
D_2	810 (20 57) sq	790 (20 07) sq
D_3	-	-
e	105 (2 67)	095 (2 41)
L	125 (3 07)	095 (2 41)
S	121 (3 07) sq	079 (2 01) sq

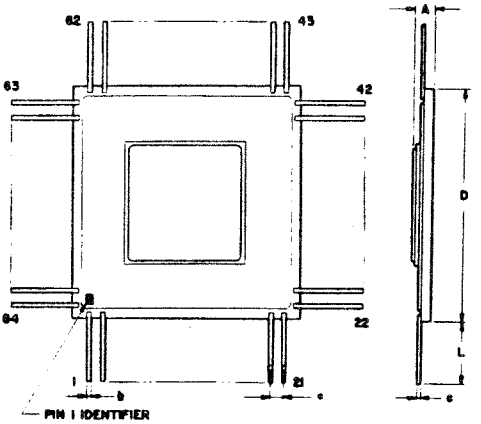
PIN MATRIX

LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES
1	B1	18	L2	35	K11	52	A10
2	B2	19	K2	36	K10	53	B10
3	C1	20	L3	37	J11	54	A9
4	C2	21	K3	38	J10	55	B9
5	D1	22	L4	39	H11	56	A8
6	D2	23	K4	40	H10	57	B8
7	E1	24	L5	41	G11	58	A7
8	E2	25	K5	42	G10	59	B7
9	F1	26	L6	43	F11	60	A6
10	F2	27	K6	44	F10	61	B6
11	G1	28	L7	45	E11	62	A5
12	G2	29	K7	46	E10	63	B5
13	H1	30	L8	47	D11	64	A4
14	H2	31	K8	48	D10	65	B4
15	J1	32	L9	49	C11	66	A3
16	J2	33	K9	50	C10	67	B3
17	K1	34	L10	51	B11	68	A2

0166

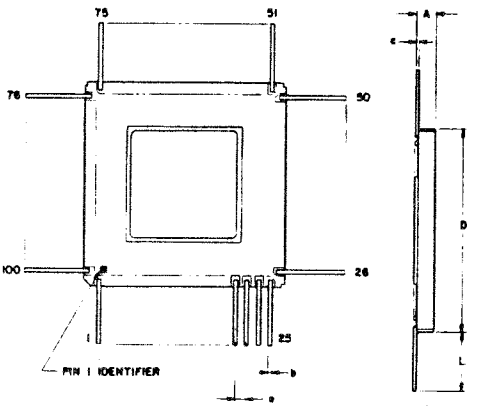
Q5000 Series
Q14000 Series

▪ 84 Lead Hermetic Ceramic Flatpack



Sym.	Inches (mm) Max.	Min.
A	120(3.05)	083(2.11)
b	020(0.51)	016(0.41)
b_1		
c	012(0.30)	009(0.23)
D	1.173(18.16) sq	1.149(29.18) sq
E		
E_1		
e	055(1.40)	045(1.14)
L	300(7.62)	275(6.99)
Q		
S		

▪ 100 Lead Hermetic Ceramic Leaded Chip Carrier (50 Mil Spacing)

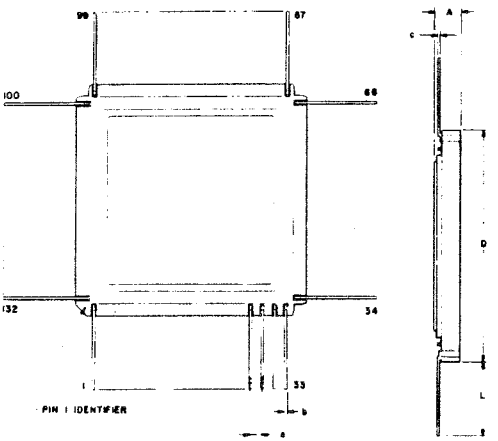


Sym.	Inches (mm) Max.	Min.
A	119(3.02)	079(2.01)
b	020(0.51)	016(0.41)
b_1		
c	013(0.33)	007(0.18)
D	1.465(37.21) sq	1.435(36.45) sq
E		
E_1		
e	055(1.40)	045(1.14)
L	400(10.16	200(5.08)
Q		
S		

0986

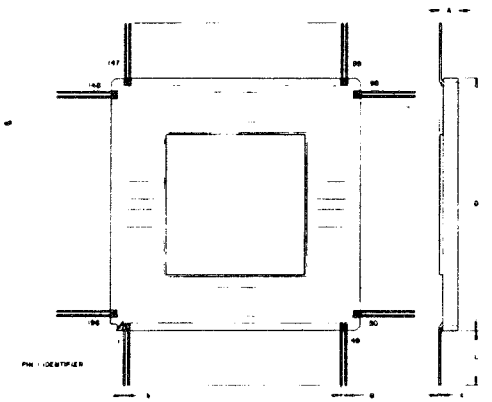
▪ 132 Lead Hermetic Ceramic Leaded Chip Carrier

Q5000 Series
Q14000 Series



Sym.	Inches (mm) Max.	Min.
A	126(3 20)	097(2 46)
b	013(0 33)	009(0 23)
b, c	– 010(0 25)	– 006(0 15)
D	960(24 38) sq	945(24 00) sq
E	–	–
E,	–	–
e	030(0 76)	020(0 51)
L	–	275(6 99)
Q	–	–
S	–	–

▪ 196 Lead Hermetic Ceramic Leaded Chip Carrier



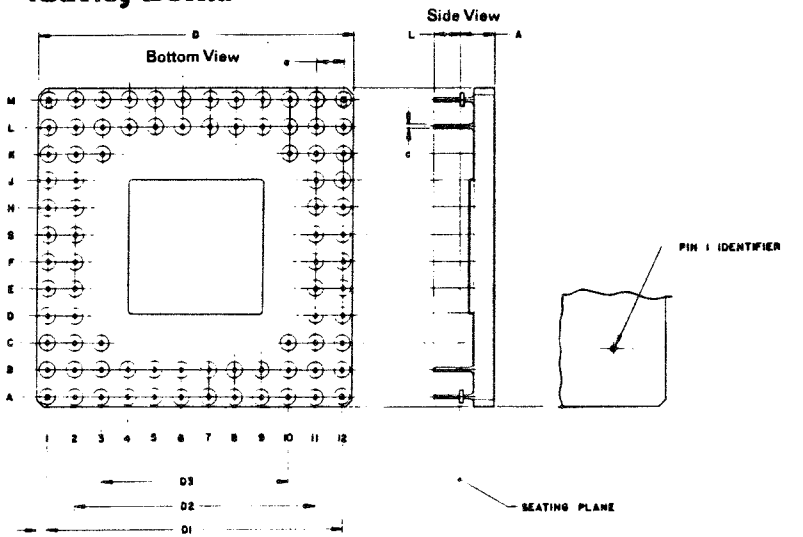
Sym.	Inches (mm) Max.	Min.
A	175 (4 44)*	155 (3 94)
b	010(0 25)	006(0 15)
b, c	– 008(0 20)	– 004(0 10)
D	1 360(34 54) sq	1 340(34 04) sq
E	–	–
E,	–	–
e	027(0 69)	023(0 58)
L	305(7 75)	285(7 24)
Q	–	–
S	–	–

*Includes .065T chip capacitors (not shown)

Pin Grid Arrays

▪ 84 Pin Hermetic Ceramic Pin Grid Array (Cavity Down)

Q5000 Series
Q14000 Series
Q20000 Series



Sym.	Inches (mm) Max.	Min.
A	154 (3 91)	107 (2 72)
c	020 (0 51)	016 (0 41)
D	1 215 (30 86) sq	1 190 (27 81) sq
D_1	1 105 (28 07) sq	1 095 (27 81) sq
D_2	905 (22 99) sq	895 (22 73) sq
D_3	705 (17 91) sq	695 (17 65) sq
e	105 (2 67)	095 (2 41)
L	130 (3 30)	090 (2 29)
S	055 (1 40) sq	045 (1 14) sq

PIN MATRIX

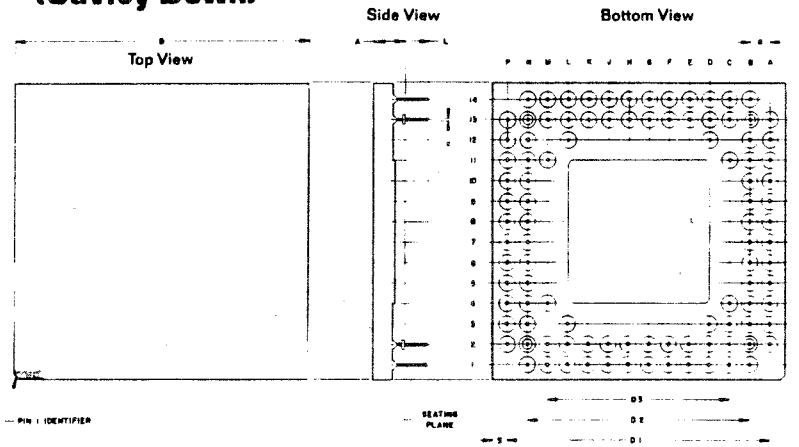
LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES
1	A1	22	M1	43	M12	64	A12
2	C2	23	L3	44	K11	65	B11
3	B1	24	M2	45	L12	66	A11
4	C1	25	M3	46	K12	67	A10
5	D2	26	L4	47	J11	68	B9
6	D1	27	M4	48	J10	69	A9
7	E2	28	L5	49	H11	70	B8
8	E1	29	M5	50	H12	71	A8
9	F1	30	L6	51	G12	72	B7
10	F2	31	M6	52	G11	73	A7
11	G1	32	L7	53	F12	74	B6
12	G2	33	M7	54	F11	75	A6
13	H1	34	M8	55	E12	76	A5
14	H2	35	L8	56	E11	77	B5
15	J1	36	M9	57	D12	78	A4
16	J2	37	L9	58	D11	79	B4
17	K1	38	M10	59	C12	80	A3
18	L1	39	M11	60	B12	81	A2
19	K2	40	L10	61	C11	82	B3
20	L2	41	L11	62	B11	83	B2
21	K3	42	K10	63	C10	84	C3

STANDOFF COORDINATES A1 A13 N1 N13

0988

▪ 100 Pin Hermetic Ceramic Pin Grid Array (Cavity Down)

Q5000 Series
Q14000 Series



Sym.	Inches (mm) Max.	Min.
A	160(4 06)	122(3 10)
c	020(0 51)	016(0 41)
D	1 465(37 21)sq	1 435(36 45)sq
D_1	1 305(33 15)sq	1 295(32 89)sq
D_2	1 105(28 07)sq	1 095(27 81)sq
D_3	905(22 99)sq	895(22 73)sq
e	105(2 67)	095(2 41)
L	140(3 56)	110(2 79)
S	090(2 29)sq	060(1 52)sq

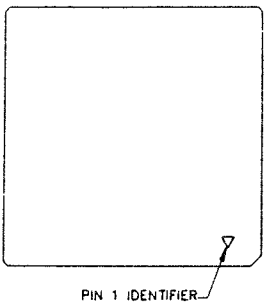
PIN MATRIX

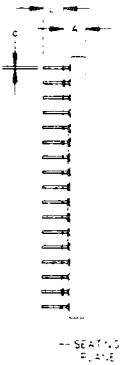
LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES
1	D3	26	N6	51	L12	76	B9
2	E2	27	N7	52	K13	77	B8
3	D2	28	N2	53	L13	78	B13
4	B1	29	N3	54	N14	79	B12
5	C1	30	N4	55	M14	80	B11
6	D1	31	P2	56	L14	81	A13
7	F2	32	P3	57	J13	82	A12
8	G2	33	P4	58	H13	83	A11
9	E1	34	P5	59	K14	84	A10
10	F1	35	P6	60	J14	85	A9
11	G1	36	P7	61	H14	86	A8
12	H2	37	N8	62	G13	87	B7
13	J2	38	N9	63	F13	88	B6
14	H1	39	P8	64	G14	89	A7
15	J1	40	P9	65	F14	90	A6
16	K1	41	P10	66	E14	91	A5
17	L1	42	P11	67	D14	92	A4
18	K2	43	P12	68	E13	93	A3
19	L3	44	P13	69	D12	94	A2
20	L2	45	N11	70	D13	95	B4
21	M1	46	N12	71	C14	96	B3
22	M2	47	N13	72	C13	97	B2
23	N1	48	M13	73	B14	98	C2
24	M4	49	N10	74	C11	99	B5
25	N5	50	M11	75	B10	100	C4

▪ 169 Pin Hermetic Ceramic Pin Grid Array (Cavity Down)

Q14000 Series

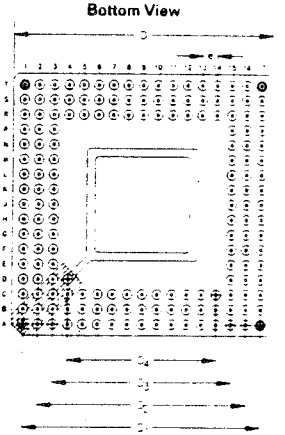
Top View





Side View

Bottom View



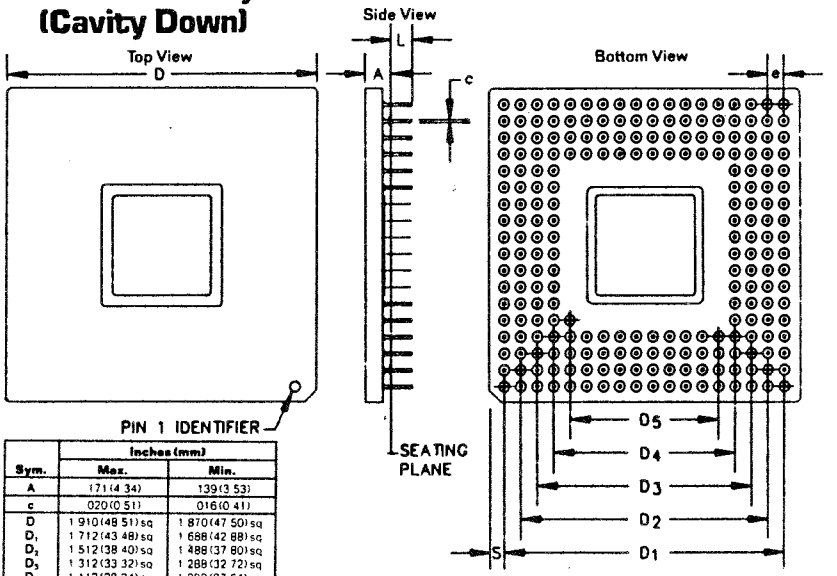
Sym.	Inches (mm)	
	Max.	Min.
A	.165(4.19)	.135(3.43)
c	.020(0.51)	.016(0.41)
D	1.768(44.91)sq.	1.732(43.99)sq.
D_1	1.605(40.77)sq.	1.595(40.51)sq.
D_2	1.405(35.69)sq.	1.395(35.43)sq.
D_3	1.205(30.61)sq.	1.195(30.35)sq.
D_4	1.005(25.53)sq.	.995(25.27)sq.
e	.105(2.67)	.095(2.41)
L	.145(3.68)	.115(2.92)
S	.088(2.224)sq.	.062(1.58)sq.

PIN MATRIX

LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES
1	B2	35	T2	69	P15	103	B15		E3		H3
2	B1	36	R4	70	R16	104	A15		G3		K3
3	D3	37	S3	71	R17	105	B14		L3		R8
4	C2	38	T3	72	P16	106	A14		N3	VSS	R10
5	C1	39	S4	73	P17	107	B13		R5		K15
6	D2	40	T4	74	N16	108	A13		R7		H15
7	D1	41	S5	75	N17	109	B12		R11		C8
8	E2	42	T5	76	M16	110	A12	VCC	R13		C10
9	E1	43	S6	77	M17	111	B11		N15		
10	F2	44	T6	78	L16	112	A11		L15		
11	F1	45	S7	79	L17	113	B10		G15		
12	G2	46	T7	80	K16	114	A10		E15		
13	G1	47	S8	81	K17	115	B9		C13		
14	H2	48	T8	82	J16	116	A9		C11		
15	H1	49	S9	83	J17	117	B8		C7		
16	J2	50	T9	84	H16	118	A8		C5		
17	J1	51	S10	85	H17	119	A7				
18	K2	52	T10	86	G17	120	B7				
19	K1	53	T11	87	G16	121	B6		F3		
20	L1	54	S11	88	F16	122	A6		J3		
21	L2	55	S12	89	F17	123	A5		M3		
22	M2	56	T12	90	E17	124	B5		R6		
23	M1	57	T13	91	E16	125	A4		R9		
24	N1	58	S13	92	D17	126	B4	VDD	R12		
25	N2	59	T14	93	D16	127	A3		M15		
26	P1	60	S14	94	C17	128	C4		J15		
27	P2	61	T15	95	C16	129	B3		F15		
28	R1	62	R14	96	D15	130	A2		C12		
29	R2	63	S15	97	B17	131	C3		C9		
30	P3	64	T16	98	B16	132	A1		C6		
31	S1	65	T17	99	C15						
32	S2	66	R15	100	A17						
33	R3	67	S16	101	A16						
34	T1	68	S17	102	C14						

▪ 225 Pin Hermetic Ceramic Pin Grid Array (Cavity Down)

Q14000 Series



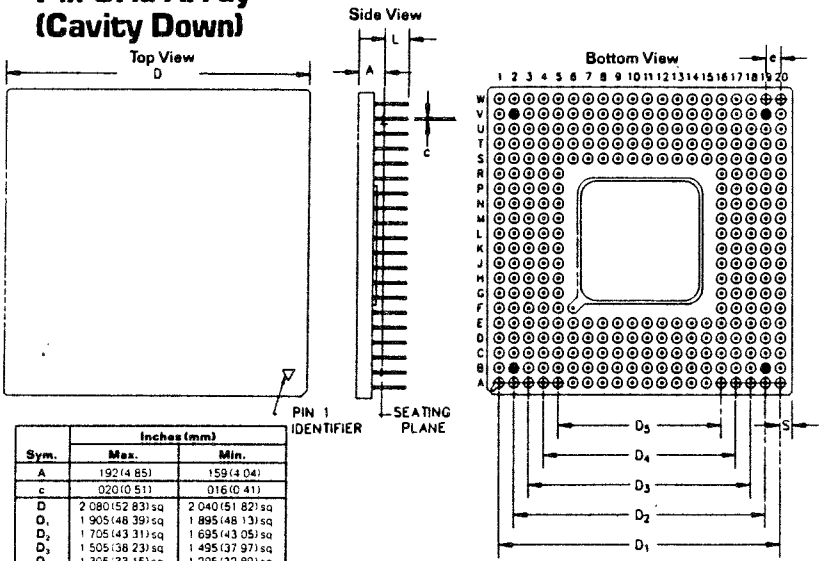
Sym.	Inches (mm) Max.	Min.
A	171 (4 34)	139 (3 53)
c	020 (0 51)	016 (0 41)
D	1 910 (48 51) sq	1 870 (47 50) sq
D_1	1 712 (43 48) sq	1 688 (42 88) sq
D_2	1 512 (38 40) sq	1 488 (37 80) sq
D_3	1 312 (33 32) sq	1 288 (32 72) sq
D_4	1 112 (28 24) sq	1 088 (27 64) sq
D_5	912 (23 16) sq	888 (22 56) sq
e	105 (2 67)	095 (2 41)
L	145 (3 68)	115 (2 92)
S	111 (2 82) sq	079 (2 01) sq

PIN MATRIX

LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES
1	B1	26	L3	51	S7	76	S14	101	J18	126	B15	151	A5		C9		D6		D4
2	D3	27	M2	52	T6	77	U16	102	J17	127	A15	152	B5		C10		D7		D5
3	C2	28	N1	53	U6	78	T16	103	H18	128	C13	153	C6		D9		D8		D14
4	C1	29	N2	54	T7	79	S15	104	H17	129	B14	154	A4		D10		D11		D15
5	E3	30	M3	55	S8	80	U17	105	G18	130	A14	155	B4		J3		D12		E4
6	D2	31	P1	56	U7	81	T18	106	H16	131	C12	156	C5		J4		D13	V_{cc}	E15
7	D1	32	P2	57	T8	82	R16	107	G17	132	B13	157	A3		J15		F4		P4
8	F3	33	N3	58	U8	83	S17	108	F18	133	A13	158	B3		J16		F15		P15
9	E2	34	R1	59	T9	84	S18	109	F17	134	B12	159	C4		K3		G4		R4
10	E1	35	R2	60	U9	85	P16	110	G16	135	C11	160	A2		K4		G15		R5
11	G3	36	P3	61	U10	86	R17	111	E18	136	A12				K15		H4		R14
12	F2	37	S1	62	T10	87	R18	112	E17	137	B11				K16	V_{DD}	H15		R15
13	F1	38	S2	63	U11	88	N16	113	F16	138	A11				R9		L4		A1
14	G2	39	R3	64	T11	89	P17	114	D18	139	B10				R10		L15		A18
15	H3	40	T1	65	U12	90	P18	115	D17	140	A10				S9		M4		B2
16	G1	41	U2	66	S11	91	M16	116	E16	141	A9				S10		M15		B17
17	H2	42	S4	67	T12	92	N17	117	C18	142	B9						N4		C3
18	H1	43	T3	68	U13	93	N18	118	C17	143	A8						N15		C16
19	J2	44	U3	69	T13	94	M17	119	D16	144	B8						R6		E5
20	J1	45	S5	70	S12	95	L16	120	B18	145	A7						R7	NONE	S3
21	K1	46	T4	71	U14	96	M18	121	A17	146	C8						R8		S16
22	K2	47	U4	72	T14	97	L17	122	C15	147	B7						R11		T2
23	L1	48	S6	73	S13	98	L18	123	B16	148	A6						R12		T17
24	L2	49	T5	74	U15	99	K17	124	A16	149	B6						R13		U1
25	M1	50	U5	75	T15	100	K18	125	C14	150	C7								U18

• 301 Pin Hermetic Ceramic Pin Grid Array (Cavity Down)

Q14000 Series



Sym.	Inches (mm) Max.	Min.
A	192 (4 85)	159 (4 04)
c	020 (0 51)	016 (0 41)
D	2 080 (52 83) sq	2 040 (51 82) sq
D_1	1 905 (48 39) sq	1 895 (48 13) sq
D_2	1 705 (43 31) sq	1 695 (43 05) sq
D_3	1 505 (38 23) sq	1 495 (37 97) sq
D_4	1 305 (33 15) sq	1 295 (32 89) sq
D_5	1 105 (28 07) sq	1 095 (27 81) sq
e	105 (2 67)	095 (2 41)
L	170 (4 32)	140 (3 56)
S	096 (2 44) sq	064 (1 63) sq

PIN MATRIX

LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES	LEAD No	PIN DES
	A1		U18		M5	1	B1	27	V1	53	V18	79	C20	105	B4	131	P3	157	U12	183	K18	209	B11
	A7	V_{CC}	W1		M16	2	C2	28	V2	54	V19	80	C19	106	A3	132	P4	158	T12	184	K17	210	C11
	A14		W7		P5	3	C1	29	V3	55	V20	81	B20	107	B3	133	R3	159	U13	185	J19	211	D11
	A20		W14		P16	4	D2	30	W3	56	U19	82	B19	108	B2	134	R4	160	T13	186	J18	212	B10
	C3		W20		R1	5	D1	31	V4	57	U20	83	B18	109	D4	135	S3	161	U14	187	J17	213	C10
	C18		A2		R20	6	E2	32	W4	58	T19	84	A18	110	D3	136	S4	162	T14	188	H18	214	D10
	E6		A8		S5	7	E1	33	V5	59	T20	85	B17	111	E4	137	T3	163	U15	189	H17	215	B9
	E8		A13	V_{SS}	S7	8	F2	34	W5	60	S19	86	A17	112	E3	138	T4	164	T15	190	G18	216	C9
	E13		A19		S9	9	G2	35	V6	61	S20	87	B16	113	F4	139	U4	165	U16	191	G17	217	D9
	E15		E5		S12	10	H2	36	W6	62	R19	88	A16	114	F3	140	T5	166	T16	192	F18	218	C8
	G1		E7		S14	11	H1	37	V7	63	P19	89	B15	115	G4	141	U5	167	U17	193	F17	219	D8
	G5		E9		S16	12	J1	38	V8	64	N19	90	A15	116	G3	142	T6	168	T17	194	E18	220	C7
V_{CC}	G16		E12		W2	13	K1	39	V9	65	N20	91	B14	117	H4	143	U6	169	T18	195	E17	221	D7
	G20	V_{CC}	E14		W8	14	L1	40	W9	66	M20	92	B13	118	H3	144	T7	170	S17	196	D18	222	C6
	J5		E16		W13	15	L2	41	W10	67	L19	93	B12	119	J4	145	U7	171	S18	197	D17	223	D6
	J16		F1		W19	16	M1	42	W11	68	L20	94	A12	120	J3	146	U8	172	R17	198	C18	224	C5
	K2		F20		E10	17	N1	43	W12	69	K20	95	A11	121	J2	147	T8	173	R18	199	C16	225	D5
	K19		H5		E11	18	N2	44	V13	70	J20	96	A10	122	K4	148	U9	174	P17	200	C16	226	C4
	N5		H16		F5	19	P2	45	V14	71	H20	97	A9	123	K3	149	T9	175	P18	201	D15		
	N16		K5		F16	20	R2	46	W15	72	H19	98	B8	124	L3	150	U10	176	N17	202	C15		
	P1		K16	V_{CC}	L5	21	S1	47	V15	73	G19	99	B7	125	L4	151	U10	177	N18	203	D14		
	P20				L16	22	S2	48	W16	74	F19	100	A6	126	M2	152	T10	178	M17	204	C14		
	S6				R5	23	T1	49	V16	75	E20	101	B6	127	M3	153	V11	179	M18	205	C13		
	S8				R16	24	T2	50	W17	76	E19	102	A5	128	M4	154	U11	180	M19	206	D13		
	S13				S10	25	U1	51	V17	77	D20	103	B5	129	N3	155	T11	181	L17	207	C12		
	S15				S11	26	U2	52	W18	78	D19	104	A4	130	N4	156	V12	182	L18	208	D12		
	U3																						

I/O PLACEMENT

DUAL-CELL I/O MACROS
- all arrays

Dual-cell I/O macros are restricted in the cells on which they may be placed. They may NOT be placed in any cell pair that is separated by a power or ground, they may not be placed to straddle a corner or other non-cell circuitry. If dual-cell I/O macros are to be placed, refer to the specific placement restriction for the array. Dual-cell I/Os placed on Q9100B or Q21000B bidirectional cells use a different layout than those placed on the other I/O cells for these arrays.

The OE10 and IE25 dual cell macros, end any others that are issued in the future, must be placed so that the two cells ere adjacent. The starting cell is restricted on the arrays as follows:

TABLE 5-A-1
PADS (CELLS) THAT CANNOT BE USED FOR
DUAL CELL I/O MACROS

Q14000B	Q9100B	Q6000B	Q2100B
8	5	4	5
26	11	8	10
32	24	19	19
47	36	27	24
59	46	35	32
68	51	39	37
79	59	48	46
87	65	54	51
103	78	65	55
118	90	73	60
130	100	82	69
138	105	88	74
149	113	95	86
157	119	99	91
173	132	110	100
188	144	118	105
200	154	126	
219	159	130	
220	167	139	
228	173	145	
244	186	156	
259	198	164	
271	208	173	
279	213	179	

SINGLE-CELL BIDIRECTIONAL MACROS
- Q9100B, Q2100B

Single-cell bidirectional macros are restricted to the following pads:

TABLE 5-A-2
SINGLE-CELL BIDI PLACEMENT

Q2100B	82-91, 96-105	
Q9100B	163-173, 190-198,	178-186, 203-213

ADDED POWER AND GROUNDS
- all arrays

Placement of added power and ground macros should be such that they can be bonded to an internal package power or ground plane if it is physically possible to do so.

The power and grounds added to handle simultaneously switching outputs also must be interspersed with those outputs.

Grounds added for high-speed path isolation need to be placed next to their designated signals.

Grounds added for TTL output - ECL input separation need to be placed between these signals.

FIXED POWER AND GROUND PAD PLACEMENT

Once the MacroMetrix ERCs and AMCCANN have been executed, the file AMCCPKG.LST will contain information on the fixed power and ground pins, showing the fixed pad assignment for each. The graphics on the chip macros are commentary information only, although it should match the file. In cases of discrepancy, defer to the AMCCPKG.LST information.

TESTER LIMIT
- Q14000B

The Trillium tester limit for signals is currently 224. The Q14000B I/O pads 67 and 147 cannot be used for I/O signals but may be used by added power and grounds. The Trillium tester capability will be expanded by 4Q89.

PROGRAMMABLE I/O OVERHEAD CURRENT - Q14000B, Q6000B

For the Q14000B and the Q6000B, the I_{EE}/I_{CC} overhead current specified in Table 5-2 corresponds to all VRB-VTA10K or all VRB-VTA100K generators being in use. The actual overhead for the circuit corresponds to the actual number of these generators required for the number of I/O cells used and their final placement. This is the programmable I/O - reference generator power-down feature.

Note: I/O placement can affect performance.

Programmable I/O overhead is the conditional placement of reference generators based on the placement of certain classes of I/O macros within certain groups of I/O cells. If none of these I/O macros exist within a group of cells, then the generator assigned to that group is not used.

TABLE 5-A-3
I/O PLACEMENT

IF ECL INPUT; OUTPUT PLACED ON CELL(PAD):		USE GENERATOR VRB; VTA; VTK
Q14000B	Q6000B	I
1-16	1-8	1
21-47	13-27	2
52-68	32-39	3
72-87	43-54	4
92-118	59-73	5
123-138	78-88	6
142-157	92-99	7
162-188	104-118	8
193-209	123-130	9
213-228	134-145	10
233-259	150-164	11
264-279	169-179	12

Example: If for an Q14000B ECL10K circuit, ECL outputs are on cells (pads) labeled 1,5,10,15,25,30; then the number of VRB generators required is 2: VRB1 and VRB2.

If the ECL inputs are on cells (pads) 2-4, 72-87, 92-118, 162-188, 233-259 and 266-272; the number of VTA10K generators required is 6: VTA1, VTA4, VTA5, VTA8, VTA11 and VTA12.

There is a maximum of 12 VRB generators, VRB1-VRB12, 12 VTA10K generators, VTA1-VTA12, and 12 VTA100K generators, VTK1-VTK12.

The incremental current (contributed to the overhead current) per generator is:

TABLE 5-A-4
CURRENT DISSIPATION BY GENERATOR

GENERATOR TYPE	CURRENT mA	
VRBi	6.0	ECL outputs (ECL 100K inputs)
VTAi	0.8	ECL 10K inputs
VTKi	0.8	ECL 100K inputs

i = 1, 2, 3, ..., 12

There is a fixed (base) component to the I_{EE} overhead current that is always present. This is listed along with the I_{CC} overhead current in Table 5-A-4.

TABLE 5-A-5
FIXED COMPONENT OF THE
TYPICAL OVERHEAD CURRENT (mA)

ARRAY ↓	TTL MODE I_{CC},mA	ECL MODE I_{EE},mA	MIXED MODE I_{EE}/I_{CC},mA	+5V REF ECL/TTL I_{CC},mA
Q14000B	12	51	51/12	63
Q6000B	12	51	51/12	63

For an ECL 10K or ECL10K/TTL circuit, both the VRB generator current and VTA10K generator currents must be computed and added to the value from Table 5-A-5.

For an ECL 100K or ECL100K/TTL circuit, both the VRB generator and VTA100K generator currents must be computed and added to the value from Table 5-A-5.

FOR ECL 10K, MIXED ECL 10K/TTL AND +5V REF ECL 10K/TTL CIRCUITS

VRB GENERATOR COMPONENT OF OVERHEAD CURRENT

For circuits using the chip macros:

QxxxxBECL10K
QxxxxBMIX10K
QxxxxBTTL10K

VRB generators are a function of the number of ECL outputs (all).

To compute an estimate with no knowledge of placement, sum the number of ECL 10K outputs and ECL 100K outputs. The number of VRB groupings on a Q14000B or Q6000B array is 12. By dividing the sum of the outputs by 12 (and rounding), the minimum number of VRB generators required can be estimated. Note that this assumes an optimum placement.

$$A = \frac{\#\ \text{ECL outputs}}{12} \quad \text{rounded}$$

Each VRB generator uses 6.0mA current.

- The minimum current due to VRB generators on a specific Q14000B array is:

  A * 6.0mA.

- The maximum current due to VRB generators that could be on any Q14000B array:

  12 * 6.0mA = 72mA.

- The actual current for a specific design is computed as the number of VRB generators actually used times 6.0mA. The actual overhead current due to VRB generators cannot be computed until placement and routing are complete and Back-Annotation has been approved.

VTA10K GENERATOR COMPONENT OF OVERHEAD CURRENT

For circuits using the chip macros:

QxxxxBECL10K
QxxxxBMIX10K
QxxxxBTTL10K

VTA10K generators are a function of the numbar of ECL inputs.

To compute an estimate with no knowledge of placement, count the number of ECL inputs. Note that with these chip macros, all ECL inputs are taken as ECL 10K inputs. The number of VTA10K (VTAi) groupings on a Q14000B or Q6000B array is 12. By dividing the number of inputs by 12 (and rounding), the minimum number of VTAi generators required can be estimated. Note that this assumes an optimum placement.

$$B = \frac{\text{\# of ECL inputs}}{12} \quad \text{rounded}$$

- The minimum current due to VTA10K generators on a Q14000B array is:

  B * 0.8mA.

- The maximum current due to VTA10K generators that could be on a Q14000B array is:

  12 * 0.8mA = 9.6mA.

- The actual current for a specific design is computed as the number of VTA10K generators actually used times 0.8mA. The actual overhead current due to VTA10K generators cannot be computed until placement and routing are complete and Back-Annotation is approved.

FOR ECL 100K, MIXED ECL 100K/TTL AND +5V REF ECL 100K/TTL CIRCUITS

VRB GENERATOR COMPONENT OF OVERHEAD CURRENT

For circuits using the chip macros:

QxxxxBECL100K
QxxxxBMIX100K
QxxxxBTTL100K

VRB generators are a function of the number of ECL outputs (all) and ECL 100K inputs.

To compute an estimata with no knowledge of placement, sum the number of ECL 10K outputs and ECL 100K outputs with the number of ECL 100K inputs. Note that with these chip macros, all ECL inputs are taken as ECL 100K inputs. The number of VRB groupings on a Q14000B or Q6000B array is 12. By dividing the sum of the outputs and the inputs by 12 (and rounding), the minimum number of VRB generators required can be estimated. Note that this assumes an optimum placement.

$$A = \frac{\#\text{ ECL outputs} + \#\text{ ECL inputs}}{12} \quad \text{rounded}$$

Each VRB generator uses 6.0mA current.

- The minimum current due to VRB generators on a specific Q14000B or Q6000B array is:

  A * 6.0mA.

- The maximum current due to VRB generators that could be on any Q14000B or Q6000B array is:

  12 * 6.0mA = 72mA.

- The actual current for a specific design is computed as the number of VRB generators actually used * 6.0mA. The actual overhead current due to VRB generators cannot be computed until placement and routing are complete and Back-Annotation has been approved.

VTA100K GENERATOR COMPONENT OF OVERHEAD CURRENT

For circuits using the chip macros:

QxxxxBECL100K
QxxxxBMIX100K
QxxxxBTTL100K

VTA100K generators are a function of the number of ECL inputs.

To compute an estimate with no knowledge of placement, count the number of ECL inputs. Note that with these chip macros, all ECL inputs are taken as ECL 100K inputs. The number of VTA100K (VTKi) groupings on a Q14000B or Q6000B array is 12. By dividing the number of inputs by 12 (and rounding), the minimum number of VTKi generators required can be estimated. Note that this assumes an optimum placement.

$$C = \frac{\text{\# of ECL inputs}}{12} \quad \text{rounded}$$

- The minimum current due to VTA100K generators on a Q14000B array is:

  C * 0.8mA.

- The maximum current due to VTA100K generators that could be on a Q14000B array is:

  12 * 0.8mA = 9.6mA.

- The actual current for a specific design is computed as the number of VTA100K generators actually used times 0.8mA. The actual overhead current due to VTA100K generators cannot be computed until placement and routing are complete and Back-Annotation is approved.

TABLE 5-A-6 EXPANDED TYPICAL OVERHEAD CURRENT (mA)				
ARRAY ↓	TTL MODE I_{CC},mA	ECL MODE I_{EE},mA	MIXED MODE I_{EE}/I_{CC},mA	+5V REF ECL/TTL I_{CC},mA
FIXED COMPONENT				
Q14000B	12	51	51/12	63
Q6000B	12	51	51/12	63
VARIABLE COMPONENTS				
VBRI VTAI VTKI		6-72 0.8-9.6 0.8-9.6	6-72 0.8-9.6 0.8-9.6	6-72 0.8-9.6 0.8-9.6
where VTAI and VTKI cannot exist on the same array				
OVERHEAD CURRENT RANGE				
Q14000B	12	51.8-133	51.8-133/12	63.8-145.4
Q6000B	12	51.8-133	51.8-133/12	63.8-145.4

PRE-PLACEMENT MACRO OCCURRENCE ERC REPORT - Q14000B, Q6000B

Prior to place and route, The ERC Macro-Occurrence report will show the overhaad current computed with the assumption of worst-case placement, i.e., the maximum number of threshold generators in use for the given I/O mode. This will be a higher power result than may be seen in the actual circuit, depending on the actual placement and ECL I/O usage.

The final power dissipation is a function of the final I/O placement, available after routing and Back-Annotation approval.

POST-PLACEMENT MACRO OCCURRENCE ERC REPORT - Q14000B, Q6000B

After place and route, the ERC Macro Occurrence report will show the ACTUAL overhaad current and the ACTUAL power dissipation based on tha overhead current value computed and passad down to tha EWS in tha CIRCUIT.PKG file. The lina entry in the CIRCUIT.PKG file would be at the top of the file and be in the following form:

OVERHEADCURRENT 123

CIRCUIT.PKG is created after the place and route has been completed. It is available with the Back-Annotation CORxxx.ews files. AMCCERC will check to see if CIRCUIT.PKG exists before performing the Macro Occurrence computations.

Section 6:

Macro Library

6-1-1 Q14000 TTL MACROS

- For any TTL input/output in a single +5V power supply circuit

Q9100B, Q2100B					
Page	Macro Name	Option	Type	Size	Description
6-1-3	IT01	S	IO	1	UNBUFFERED TTL
6-1-4	TI01	S	B	1	SINGLE TTL LEVEL TRANS.
6-1-5	TI03	S	B	2	TRIPLE TTL LEVEL TRANS.
6-1-6	IT12	S, H	IO	1, 1	BUFFERED TTL INPUT
6-1-7	OT21	S, H	IO	1, 1	TTL OUTPUT WITH NOR
6-1-8	OT24	S	IO	1	TTL 3-STATE INV. OUTPUT
6-1-9	UT27	S, H	IO	1, 1	TTL BIDIRECTIONAL I/O
6-1-10	Example hook-up of UT27				

6-2-1 Q14000 TTLMIX MACROS

- For TTL input/output in ECL/TTL mixed circuit with two power supplies (–5.2V and +5V for ECL 10K input, any ECL output or –4.5V and +5V for ECL 100K input, any ECL output).

Q9100B, Q2100B					
Page	Macro Name	Option	Type	Size	Description
6-2-3	IT52	L, H	IO	1, 1	TTLMIX BUFFERED INPUT
6-2-4	OT61	S, H	IO	1, 1	TTLMIX OUTPUT WITH OR
6-2-5	OT64	S, H	IO	1, 1	TTLMIX 3-STATE OUTPUT
6-2-6	OT65	S	IO	1	TTLMIX 8mA 3-STATE OUTPUT
6-2-7	UT67	S	IO	1	TTLMIX BIDIRECTIONAL I/O
6-2-8	Example hook-up of UT67				

Q14000B, Q6000B					
Page	Macro Name	Option	Type	Size	Description
6-2-10	IT62	S	IO	1	TTLMIX BUFFERED INPUT
6-2-11	OT71	S, L	IO	1, 1	TTLMIX OUTPUT
6-2-12	OT74	S, L	IO	1, 1	TTLMIX 3-STATE OUTPUT

6-3-1 Q14000 ECL MACROS

- For ECL input/output in any circuit, +5V ECL, standard ECL, and ECL/TTL mix circuits

OEnn is used for ECL 10K
OKnn is used for ECL 100K
UEnn is used for bidirectional ECL 10K
UKnn is used for bidirectional ECL 100K

Q9100B, Q2100B

Q14000B, Q6000B

6-4-1 Q14000 INTERNAL LOGIC MACROS

- S-OPTION ONLY - No other options available = (812) change

EXOR/EXNOR GATES

Page	Macro Name	Type	Size	Description
6-4-3	EX06	BASIC	1	EXCLUSIVE OR
6-4-4	EX08	BASIC	1	2-INPUT XNOR

FLIP FLOPS

Page	Macro Name	Type	Size	Description
6-4-5	FF04A	BASIC	3	D F/F, Q, QN, ASN, ARN
6-4-6	FF05	BASIC	2	D F/F, Q, QN
6-4-7	FF06	BASIC	2	D F/F, Q, QN, ASN
6-4-8	FF07	BASIC	2	D F/F, Q, QN, ARN
6-4-9	FF09	BASIC	2	D F/F, QN, ASN, ARN
6-4-10	FF10	BASIC	2	D F/F, Q, ASN, ARN
6-4-11	FF11	BASIC	3	D F/F W/2:1 MUX
6-4-12	FF12	BASIC	3	D F/F W/2:1 MUX; ARN
6-4-14	FF13	BASIC	3	D F/F W/2:1 MUX; ASN
6-4-16	FF14A	BASIC	3	D F/F W/2:1 MUX; ASN; ARN
6-4-18	FF23A	BASIC	4	J-K F/F, ARN
6-4-19	FF24A	BASIC	4	J-K F/F, ASN; ARN
6-4-21	FF70	BASIC	2	Metastable D F/F, Q

Q14000 INTERNAL LOGIC MACROS

GATES

Page	Macro Name	Type	Size	Description
6-4-22	GT05	BASIC	1	3-INPUT OR
6-4-23	GT06	BASIC	2	6-INPUT OR
6-4-24	GT07	BASIC	3	8-INPUT OR
6-4-25	GT13	BASIC	1	3-INPUT NOR
6-4-26	GT14	BASIC	2	4-INPUT NOR
6-4-27	GT15	BASIC	1	DUAL 2-INPUT NOR
6-4-28	GT21	BASIC	1	DOUBLED UP INVERTER
6-4-29	GT22	BASIC	1	BUFFER W/DOUBLED-UP OUTPUT
6-4-30	GT23	BASIC	1	DUAL INVERTER
6-4-31	GT34A	BASIC	2	5-INPUT AND
6-4-33	GT35	BASIC	1	4-INPUT NAND
6-4-35	GT38A	BASIC	2	8-INPUT AND
6-4-37	GT40	BASIC	1	DUAL 2-INPUT NAND
6-4-38	GT41A	BASIC	1	2 1-2 INPUT AND-OR INVERT
6-4-39	GT42A	BASIC	1	2 2-2 INPUT AND-OR INVERT
6-4-40	GT43A	BASIC	2	2 3-3 INPUT AND-OR INVERT
6-4-41	GT45A	BASIC	1	2 2-1 INPUT OR-AND INVERT
6-4-42	GT46A	BASIC	1	2 2-2 INPUT OR-AND INVERT
6-4-43	GT48A	BASIC	2	4 2-2-2-2 INPUT OR-AND INVERT
6-4-44	GT49	BASIC	1	3-INPUT NAND
6-4-45	GT50	BASIC	2	4 2-2-2-2 INPUT AND-OR INVERT
6-4-46	GT51	BASIC	2	2 3-3 INPUT OR-AND INVERT
6-4-47	GT52	BASIC	1	3-INPUT AND

LATCHES

Page	Macro Name	Type	Size	Description
6-4-48	LA03	BASIC	1	D LATCH; AS
6-4-49	LA04	BASIC	1	D LATCH
6-4-50	LA05	BASIC	2	D LATCH; AR

6-5-1 Q14000 MSI MACROS

- S-OPTION ONLY - No other options available

ADDERS

Page	Macro Name	Type	Size	Description
6-5-3	ADD283A	BASIC	15	4 BIT CARRY-LOOK-AHEAD ADDER

COMPARATOR

Page	Macro Name	Type	Size	Description
6-5-6	CMP688	BASIC	6	8 BIT MAGNITUDE COMPARATOR

COUNTER

Page	Macro Name	Type	Size	Description
6-5-8	CTR161A	BASIC	18	4 BIT UP CNTR W/AR, LOAD, EN
6-5-10	CTR163B	BASIC	16	4 BIT COUNTER W/SR, LOAD, EN

DECODER

Page	Macro Name	Type	Size	Description
6-5-13	DEC138A	BASIC	7	3-8 DECODER W/ENABLE

MULTIPLEXERS

Page	Macro Name	Type	Size	Description
6-5-15	MUX153A	BASIC	2	4:1 MUX W/LO ENABLE
6-5-18	MUX157A	BASIC	5	QUAD 2:1 MUX W/ENABLE LOW

REGISTERS

Page	Macro Name	Type	Size	Description
6-5-20	REG06	BASIC	6	6 BIT LATCH
6-5-22	REG164A	BASIC	16	8 BIT S/P SHIFT REG; AR
6-5-24	REG175A	BASIC	10	4 BIT REGISTER; AR
6-5-26	REG373A	BASIC	8	8 BIT LATCH; AR

6-6-1 SPECIAL MACROS

Page	Macro Name	Cell	Size	Description
6-6-3	ITPWR	I/O	1	ADDED VCC PIN FOR TTL
6-6-4	ITGND	I/O	1	ADDED GROUND PIN FOR TTL
6-6-5	IEVCC	I/O	1	ADDED ECL VCC SUPPLY

CHIP MACROS

CHIP MACROS - Use no cells; Must use 1 per circuit
- Update schmatics to show (812) on Chip macros -

Page	Macro Name	Description
6-6-8	Q9100BTTL	FOR 100% TTL; Q9100B ARRAY
6-6-8	Q9100BECL10K	FOR 100% ECL10K; Q9100B ARRAY
6-6-8	Q9100BECL100K	FOR 100% ECL100K; Q9100B ARRAY
6-6-9	Q9100BMIX10K	DUAL SUPPLY ECL10K/TTL; Q9100B ARRAY
6-6-9	Q9100BMIX100K	DUAL SUPPLY ECL100K/TTL; Q9100B ARRAY
6-6-10	Q9100BTTL10K	FOR +5V ECL10K/TTL; Q9100B ARRAY
6-6-10	Q9100BTTL100K	FOR +5V ECL100K/TTL; Q9100B ARRAY
6-6-8	Q2100BTTL	FOR 100% TTL; Q2100B ARRAY
6-6-8	Q2100BECL10K	FOR 100% ECL10K; Q2100B ARRAY
6-6-8	Q2100BECL100K	FOR 100% ECL100K; Q2100B ARRAY
6-6-9	Q2100BMIX10K	DUAL SUPPLY ECL10K/TTL; Q2100B ARRAY
6-6-9	Q2100BMIX100K	DUAL SUPPLY ECL100K/TTL; Q2100B ARRAY
6-6-10	Q2100BTTL10K	FOR +5V ECL10K/TTL; Q2100B ARRAY
6-6-10	Q2100BTTL100K	FOR +5V ECL100K/TTL; Q2100B ARRAY
TBS	Q14000B	
TBS	Q6000B	

MACRO NAMING CONVENTION - Q14000

THE EXPANSION OF A MACRO NAME IS GIVEN BELOW:

```
aa{a}nnb
  :  : :
  :  : :
  :  : :..... POWER/FAN-OUT      S - STANDARD     (30 LOADS)
  :  :                              High-fan-out  (50 LOADS)
  :  :                           H - SPEED        (30 LOADS)
  :  :                           (3-STATE DRIVERS - 8 LOADS)
  :  :
  :  :.....CELL # (00-119)
  :
  :.....CELL TYPE: TWO - THREE LETTERS
                   (THREE LETTERS FOR MSI MACROS)
```

KEY

AD -	ADDER
ADD -	MSI ADDER
BB -	MSI BUILDING BLOCK - AMCC USE ONLY
BI -	ECL INPUT BUFFERED LOGIC
CPG -	MSI CARRY LOOK-AHEAD GENERATOR
CMP -	MSI COMPARATOR
CTR -	MSI COUNTER
DE -	DECODER
DEC -	MSI DECODER
EX -	EXOR
FF -	FLIP FLOP, F/F
FFF -	MSI F/F
GT -	GENERAL GATES
LA -	LATCH
MX -	MULTIPLEXOR, MUX
REG -	MSI REGISTER
IE -	ECL input
OE -	ECL 10K output
UE -	ECL 10K bidirectional
OK -	ECL 100K output
IT -	TTL input
OT -	TTL output
UT -	TTL bidirectional

FOR TTL I/O MACROS:

00-39 = 100 % TTL; OR MIX IN A +5V ONLY CIRCUIT
40-79 = MIX IN A DUAL POWER SUPPLY CIRCUIT

FOR ECL I/O MACROS:

LETTER DESIGNATION FOR ECL 10K AND ECL 100K
ECL MACROS DO NOT VARY WITH I/O MODE

CHIP MACRO NAMING CONVENTION:

Qaaaaabcccdddd

Where:

aaaaa	3-5 characters that identify the array be name: 9100 2100
b	Character that designates the family B
ccc	3 characters that identify the I/O mode TTL ECL MIX for two-power supplies
dddd	3-4 characters to identify the ECL input type ØØØ for none 10K 100K

Section 6-1:

TTL Interface

FOR 100% TTL OR ECL/TTL MIXED MODE CIRCUITS;
SINGLE +5V POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

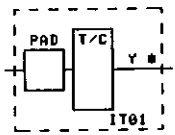
IT01 1 I/O cell PAD & WIRE W/ESD PROTECTION

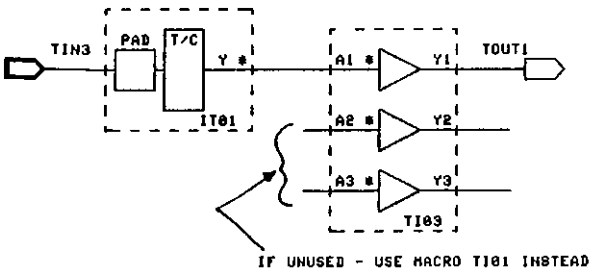
		S	H	
Tpd PAD->Y	++	0.00	0.00	ns
	--	0.00	0.00	ns
ICC		0.00	0.00	mA
FAN-OUT LOAD LIMIT:		10	10	loads
k-FACTOR	RISING	0.005	0.005	ns/LU
	FALLING	0.005	0.005	ns/LU

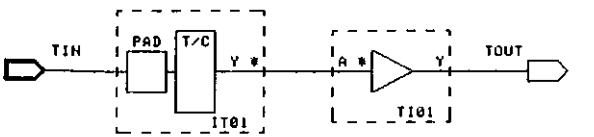
---

* Y PIN CONNECTS TO TI01 OR TI03

Y = PAD







ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

TI01 1 B cell SINGLE TTL LEVEL TRANSLATOR

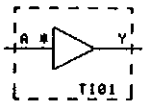
		S	
Tpd A->Y	++	2.00	ns
	--	2.10	ns
ICC: INPUT LOW		0.00	mA
INPUT HIGH		0.40	mA
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR RISING		0.025	ns/LU
FALLING		0.025	ns/LU

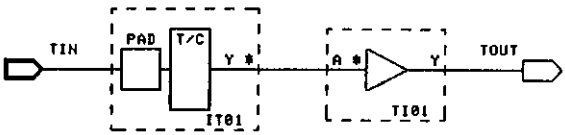
---

* A MUST BE DRIVEN BY IT01 MACRO

A = Y

A	Y
0	0
1	1





ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

TI03 2 B cell TRIPLE TTL LEVEL TRANSLATOR

		S	
Tpd Ai->Yi	++	2.00	ns
	--	2.10	ns
i = 1,2,3			
ICC: INPUT LOW		0.00	mA
INPUT HIGH		0.40	mA
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR RISING		0.025	ns/LU
FALLING		0.025	ns/LU

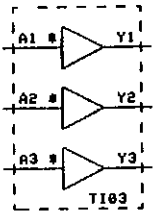
---

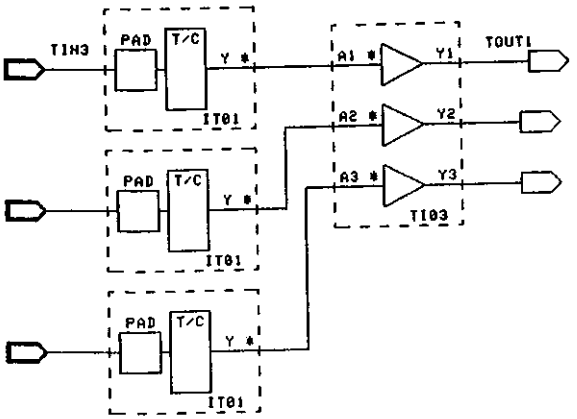
* A1, A2, A3 MUST BE DRIVEN BY IT01 MACRO

A1 = Y1

A2 = Y2

A3 = Y3



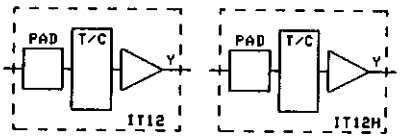


FOR 100% TTL OR ECL/TTL MIXED MODE CIRCUITS;
SINGLE +5V POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

IT12 1 I/O cell BUFFERED TTL INPUT

		S	H	
Tpd PAD->Y	++	2.97	2.60	ns
	--	3.90	3.71	ns
ICC: INPUT LOW		2.80	3.20	mA I/O
INPUT HIGH		2.70	3.10	mA I/O
FAN-OUT LOAD LIMIT:		50	50	loads
k-FACTOR RISING		0.025	0.025	ns/LU
FALLING		0.030	0.030	ns/LU

Y = PAD



FOR 100% TTL OR ECL/TTL MIXED MODE CIRCUITS;
SINGLE +5V POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

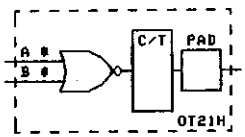
OT21 1 I/O cell TTL BUFFERED OUTPUT WITH NOR

		H	
(1 INPUT CHANGING)			
Tpd A,B->PAD	+-	2.35	ns
	-+	2.44	ns
(BOTH INPUTS CHANGING)			
A,B->PAD	+-	2.31	ns
	-+	2.35	ns
ICC: INPUTS LOW		0.00	mA I/O
INPUT(S) HIGH		2.00	mA I/O
k-FACTOR RISING		0.055	ns/pF
FALLING		0.055	ns/pF

---

* A, B COUNT AS 3 LOADS EACH
EITHER A OR B MUST BE DRIVEN BY A MACRO
IF ONE INPUT IS UNUSED, TIE TO GLOBAL GROUND

$PAD = \overline{A + B}$



FOR 100% TTL OR ECL/TTL MIXED MODE CIRCUITS;
SINGLE +5V POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

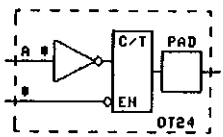
OT24 1 I/O cell TTL 3-STATE INVERTING OUTPUT

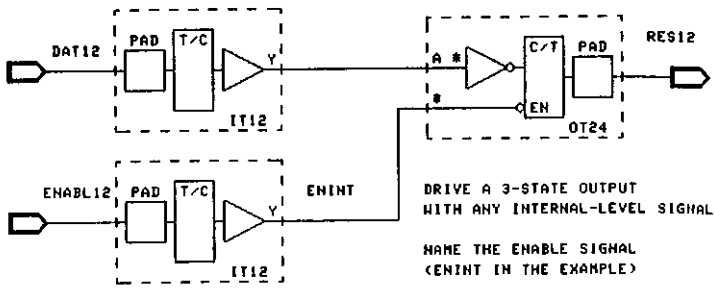
		S	
Tpd A->PAD	+-	2.32	ns
	-+	2.39	ns
EN->PAD	LZ	4.07	ns
	HZ	1.32	ns
	ZL	4.87	ns
	ZH	2.51	ns
ENABLED:			
ICC: INPUT LOW		0.00	mA I/O
INPUT HIGH		1.97	mA I/O
DISABLED:			
ICC		2.67	mA I/O
k-FACTOR	RISING PAD	0.055	ns/pF
	FALLING	0.055	ns/pF

---

* A, EN COUNT AS 3 LOADS EACH
A, EN - EACH MUST BE DRIVEN BY A MACRO

EN	A	PAD
0	0	1
0	1	0
1	0	3-STATE
1	1	3-STATE





FOR 100% TTL OR ECL/TTL MIXED MODE CIRCUITS;
SINGLE +5V POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

UT27 1 I/O cell TTL BIDIRECTIONAL

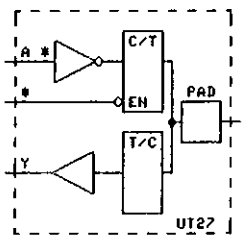
			S	H	
Tpd	PAD->Y	++	3.12	2.71	ns
		--	3.84	3.55	ns
	A->PAD	+-	3.21	2.75	ns
		-+	5.17	3.83	ns
	EN->PAD	HZ	2.45	2.45	ns
		ZH	5.25	5.25	ns
		LZ	2.45	2.35	ns
		ZL	4.25	4.25	ns
ENABLED:					
ICC:	INPUT LOW		3.05	3.40	mA I/O
	INPUT HIGH		5.15	6.80	mA I/O
DISABLED:					
ICC:	INPUT LOW		5.85	6.75	mA I/O
	INPUT HIGH		7.30	9.35	mA I/O
FAN-OUT LOAD LIMIT:		Y	50	50	loads
k-FACTOR	RISING	Y	0.025	0.025	ns/LU
	FALLING		0.030	0.030	ns/LU
k-FACTOR	RISING	PAD	0.055	0.055	ns/pF
	FALLING		0.055	0.055	ns/pF

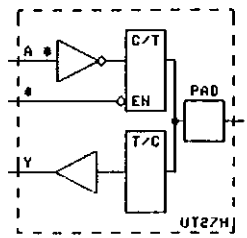
---

* A, EN COUNT AS 3 LOADS EACH
A, EN - EACH MUST BE DRIVEN BY A MACRO

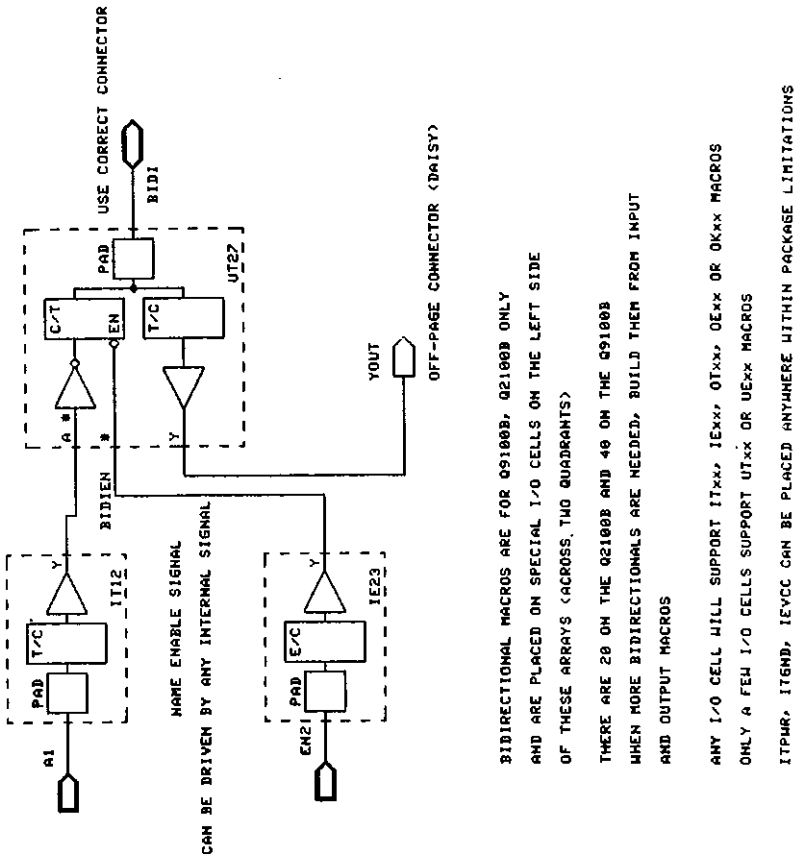
EN = 0: PAD = $\bar{A}$ Y = $\bar{A}$

EN = 1: Y = PAD





FOR 100% TTL OR ECL/TTL MIXED MODE CIRCUITS;
SINGLE +5V POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY



Bidirectional macros for Q9100B, Q2100B only

Section 6-2:

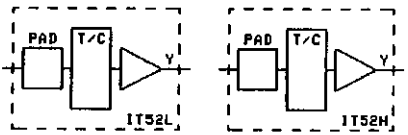
TTL Mix Interface

FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

IT52 1 I/O cell TTLMIX BUFFERED INPUT

		S	L	H	
Tpd PAD->Y	++		2.79	1.30	ns
	--		4.11	1.30	ns
ICC			0.16	0.43	mA I/O
IEE			0.94	2.30	mA I/O
FAN-OUT LOAD LIMIT:			50	50	loads
k-FACTOR	RISING		0.020	0.025	ns/LU
	FALLING		0.047	0.030	ns/LU

Y = PAD



FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

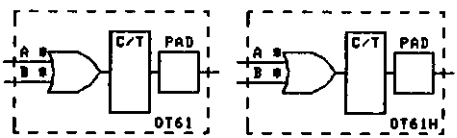
OT61 1 I/O cell TTLMIX OUTPUT WITH OR

		S	H	
(1 INPUT CHANGING)				
Tpd A,B->PAD	++	3.07	3.01	ns
	--	4.64	3.04	ns
(BOTH INPUTS CHANGING)				
A,B->PAD	++	4.55	3.52	ns
	--	4.86	3.37	ns
ICC: INPUTS LOW		1.25	1.52	mA I/O
INPUT(S)HIGH		0.85	1.40	mA I/O
IEE		1.07	1.64	mA I/O
k-FACTOR RISING	PAD	0.055	0.055	ns/pF
FALLING		0.055	0.055	ns/pF

---

* A, B COUNT AS 8 LOADS EACH
EITHER A OR B MUST BE DRIVEN BY A MACRO

PAD = A + B



FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

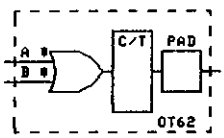
OT62 1 I/O cell 8mA TTL OUTPUT

		S	
(1 INPUT CHANGING))			
Tpd A,B->PAD	++	5.41	ns
	--	7.85	ns
(BOTH INPUTS CHANGING)			
A,B->PAD	++	7.99	ns
	--	8.18	ns
ICC: INPUTS LOW		0.59	mA I/O
INPUT(S)HIGH		0.28	mA I/O
IEE		0.48	mA I/O
k-FACTOR RISING	PAD	0.055	ns/pF
FALLING		0.055	ns/pF

---

* A, B COUNT AS 8 LOADS EACH

PAD = A + B



FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

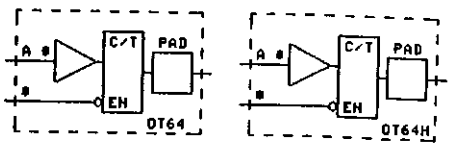
OT64 1 I/O cell TTLMIX 3-STATE OUTPUT

		S	H	
Tpd A->PAD	++	3.62	3.46	ns
	--	4.52	2.94	ns
(EN->PAD)	LZ	2.78	2.64	ns
	HZ	3.37	3.42	ns
	ZL	5.80	4.81	ns
	ZH	3.39	3.40	ns
ENABLED:				
ICC:	INPUT LOW	1.31	1.52	mA I/O
	INPUT HIGH	0.89	1.83	mA I/O
IEE		2.50	3.45	mA I/O
DISABLED:				
ICC		1.25	3.18	mA I/O
IEE		2.50	3.45	mA I/O
k-FACTOR	RISING PAD	0.055	0.055	ns/pF
	FALLING	0.055	0.055	ns/pF

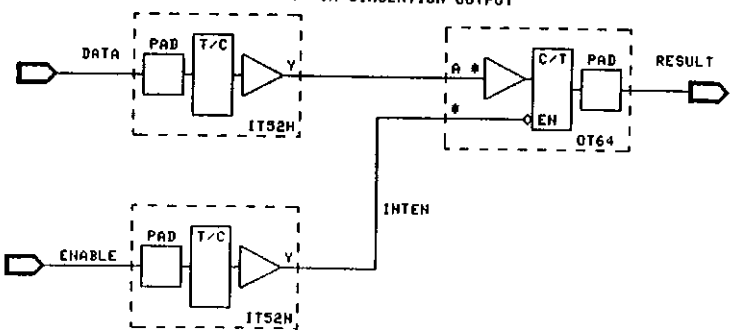
---

* A COUNTS AS 8 LOADS
* EN COUNTS AS 16 LOADS
A, EN - EACH MUST BE DRIVEN BY A MACRO

IF EN = 0, PAD = A
IF EN = 1, PAD = HIGH-Z



DRIVE A 3-STATE OUTPUT WITH ANY INTERNAL SIGNAL
NAME THE ENABLE SIGNAL - LIST IN SIMULATION OUTPUT



FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

OT65 1 I/O cell MIXED TTL OUTPUT W/TRISTATE, 8mA

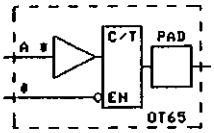
			S	
Tpd	A->PAD	++	7.08	ns
		--	7.64	ns
	(EN->PAD)	LZ	3.16	ns
		HZ	3.88	ns
		ZL	12.12	ns
		ZH	7.79	ns
ENABLED:				
ICC:	INPUT LOW		0.59	mA I/O
	INPUT HIGH		0.28	mA I/O
IEE			1.11	mA I/O
DISABLED:				
ICC			0.90	mA I/O
IEE			1.11	mA I/O
k-FACTOR	RISING	PAD	0.055	ns/pF
	FALLING		0.055	ns/pF

---

* A COUNT AS 8 LOAD
* EN COUNT AS 16 LOADS

IF EN = 0, PAD = A

IF EN = 1, PAD = HIGH Z



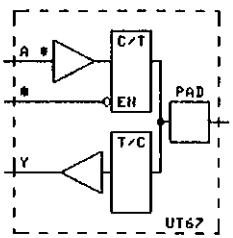
FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

UT67 1 I/O cell TTLMIX BIDIRECTIONAL

			S	
Tpd	A->PAD	++	3.76	ns
		--	5.01	ns
	EN->PAD	HZ	4.49	ns
		ZH	3.50	ns
		LZ	3.29	ns
		ZL	5.52	ns
	PAD->Y	++	5.67	ns
		--	3.41	ns
ENABLED:				
ICC:	INPUT LOW		2.96	mA I/O
	INPUT HIGH		2.51	mA I/O
IEE:	INPUT LOW		5.55	mA I/O
	INPUT HIGH		5.75	mA I/O
DISABLED:				
ICC:	INPUT LOW		3.78	mA I/O
	INPUT HIGH		3.42	mA I/O
IEE:	INPUT LOW		5.96	mA I/O
	INPUT HIGH		5.57	mA I/O
FAN-OUT LOAD LIMIT:		Y	50	loads
k-FACTOR	RISING	Y	0.025	ns/LU
	FALLING		0.030	ns/LU
k-FACTOR	RISING	PAD	0.055	ns/pF
	FALLING		0.055	ns/pF

---

* A COUNTS AS 8 LOADS
* EN COUNTS AS 16 LOADS
A, EN EACH MUST BE DRIVEN BY A MACRO

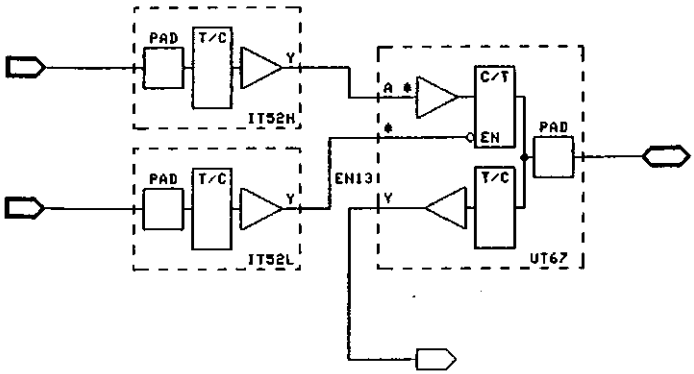


FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

UT67 1 I/O cell TTLMIX BIDIRECTIONAL

EN = 0: PAD = A Y = A

EN = 1: Y = PAD



BIDIRECTIONAL - NAME THE SIGNAL DRIVING THE ENABLE PIN
LIST THE SIGNAL IN THE SIMULATION OUTPUT FILE
THE ENABLE CAN BE DRIVEN BY ANY INTERNAL-LEVEL SIGNAL

BIDIRECTIONAL MACROS ARE FOR Q9100B, Q2100B ONLY
AND ARE PLACED ON SPECIAL I/O CELLS ON THE LEFT SIDE
OF THESE ARRAYS (ACROSS TWO QUADRANTS)

THERE ARE 20 ON THE Q2100B AND 40 ON THE Q9100B
WHEN MORE BIDIRECTIONALS ARE NEEDED, BUILD THEM FROM INPUT
AND OUTPUT MACROS

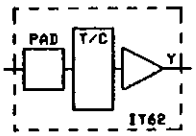
ANY I/O CELL WILL SUPPORT ITxx, IExx, OTxx, OExx OR OKxx MACROS
ONLY A FEW I/O CELLS SUPPORT UTxx OR UExx MACROS

ITPWR, ITGND, IEVCC CAN BE PLACED ANYWHERE WITHIN PACKAGE LIMITATIONS

FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q14000B/Q6000B ONLY

IT62 1 I/O cell		TTL INPUT BUFFER	
		S	
Tpd			
PAD->Y	++	1.85	ns
	--	1.85	ns
ICC		1.50	mA I/O
FAN-OUT LOAD LIMIT:		50	loads
k-FACTOR	RISING	0.030	ns/LU
	FALLING	0.034	ns/LU

Y = PAD

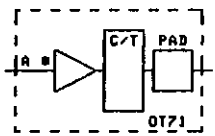


FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q14000B/Q6000B ONLY

CT71 1 I/O cell		TTL OUTPUT		
		S	L	
Tpd				
A->PAD	++	1.90	2.90	ns
	--	3.75	3.75	ns
ICC		1.50	1.00	mA I/O
IEE		0.50	0.50	mA I/O
k-FACTOR	RISING	0.055	0.055	ns/pF
	FALLING	0.055	0.055	ns/pF

* A COUNTS AS 3 LOADS

PAD = A



AMCC Q14000 MACRO SUMMARY - TTLMIX (903)

FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q14000B/Q6000B ONLY

OT74 1 I/O cell TTL 3-STATE OUTPUT

			S	L	
Tpd					
	A->PAD	++	2.05	3.05	ns
		--	3.85	3.85	ns
	EN->PAD	tpZL	9.00	9.00	ns
		tpZH	9.00	9.00	ns
		tpLZ	9.00	9.00	ns
		tpHZ	9.00	9.00	ns
ICC			1.85	1.20	mA I/O
IEE			1.85	1.20	mA I/O
k-FACTOR	RISING		0.055	0.55	ns/LU
	FALLING		0.055	0.55	ns/LU

---

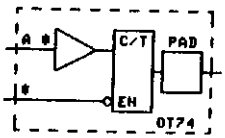
* A COUNTS AS 4 LOADS
* EN COUNTS AS 3 LOADS

```
IF EN = 0:

  PAD = A

IF EN = 1:

  PAD = H . Z
```



Section 6-3:

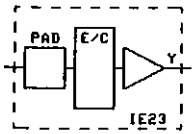
ECL Interface

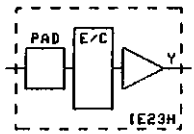
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

IE23 1 I/O cell ECL INPUT BUFFER

		S	H	
Tpd PAD->Y	++	1.23	1.20	ns
	--	0.97	1.10	ns
IEE		1.58	2.35	mA I/O
FAN-OUT LOAD LIMIT:		50	50	loads
k-FACTOR	RISING	0.025	0.025	ns/LU
	FALLING	0.030	0.030	ns/LU

Y = PAD



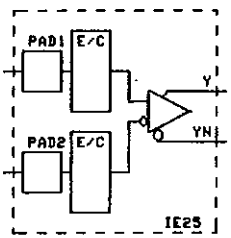


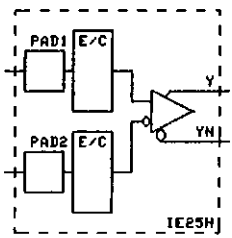
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

IE25 2 I/O cell DIFFERENTIAL ECL INPUT BUFFER

			S	H	
Tpd PAD->Y	-+	++	3.16	2.15	ns
	+-	--	2.72	1.76	ns
PAD->YN	--	+-	2.72	1.76	ns
	++	-+	3.16	2.15	ns
IEE: A HIGH, AN LOW			3.60	3.95	mA I/O
A LOW, AN HIGH			4.05	4.85	mA I/O
FAN-OUT LOAD LIMIT:			50	50	loads
			50	50	loads
k-FACTOR RISING			0.025	0.025	ns/LU
FALLING			0.030	0.030	ns/LU

PAD 1	PAD 2	Y	YN
0	0	UNKNOWN	UNKNOWN
0	1	0	1
1	0	1	0
1	1	UNKNOWN	UNKNOWN





FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

OE10 2 I/O cell ECL DIFFERENTIAL OUTPUT

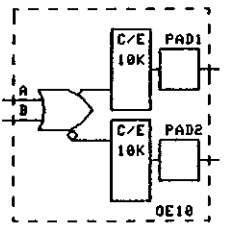
		S	
(1 INPUT CHANGING)			
Tpd A,B->PAD1	++	0.37	ns
	--	0.64	ns
A,B->PAD2	+-	0.55	ns
	-+	0.31	ns
(ALL INPUTS CHANGING)			
A,B->PAD1	++	0.37	ns
	--	0.56	ns
A,B->PAD2	+-	0.55	ns
	-+	0.25	ns
IEE: INPUT LOW		4.40	mA I/O
INPUT HIGH		5.45	mA I/O
k-FACTOR RISING		0.045	ns/pF
FALLING		0.045	ns/pF

A, B - AT LEAST ONE MUST BE DRIVEN BY A MACRO

PAD1 = A + B

PAD2 = $\overline{\overline{A} + \overline{B}}$

OE10: ECL 10K



ECL 10K

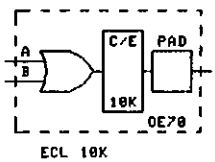
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

Ox70 1 I/O cell	ECL OUTPUT WITH OR		
	OE70 S	OK70 S	
Tpd A,B->PAD ++	0.42	0.44	ns
--	0.79	0.81	ns
IEE: INPUTS LOW	4.40	4.40	mA I/O
INPUT(S)HIGH	5.30	5.30	mA I/O
k-FACTOR RISING	0.045	0.045	ns/pF
	0.045	0.045	ns/pF

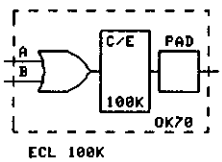
* A, B COUNT AS 3 LOADS EACH
EITHER A OR B MUST BE DRIVEN BY A MACRO

PAD = A + B

OE70: ECL 10K
OK70: ECL 100K



ECL 10K



ECL 100K

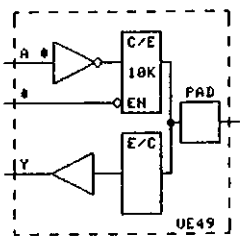
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

UE49 1 I/O cell ECL BIDIRECTIONAL

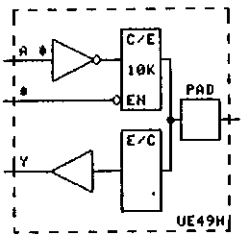
			S	H	
Tpd A,EN->PAD		+-	0.53	0.53	ns
		-+	0.38	0.38	ns
PAD->Y		++	3.45	2.55	ns
		--	2.65	2.02	ns
ENABLED:					
IEE: INPUT LOW			6.65	7.20	mA I/O
INPUT HIGH			7.65	8.20	mA I/O
DISABLED:					
IEE: INPUT LOW			7.65	8.20	mA I/O
INPUT HIGH			7.65	8.20	mA I/O
FAN-OUT LOAD LIMIT:		Y	50	50	loads
k-FACTOR	RISING	Y	0.025	0.025	ns/LU
	FALLING		0.030	0.030	ns/LU
k-FACTOR	RISING	PAD	0.045	0.045	ns/pF
	FALLING		0.045	0.045	ns/pF

---

* A, EN COUNT AS 3 LOADS EACH
A, EN, Y EACH MUST BE DRIVEN BY A MACRO



ECL 10K



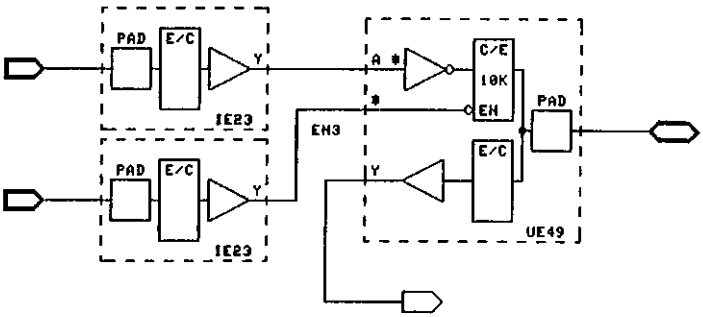
ECL 10K

FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q9100B/Q2100B ONLY

EN = 0: PAD = $\bar{A}$ Y = $\bar{A}$

EN = 1: Y = PAD

UE49: ECL 10K



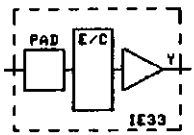
DRIVE THE ENABLE PIN BY ANY INTERNAL-LEVEL SIGNAL

NAME THE ENABLE SIGNAL
LIST IT IN THE SIMULATION OUTPUT FILE

FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q14000B/Q6000B ONLY

IE33 1 I/O cell ECL INPUT BUFFER		
	S	
Tpd		
PAD->Y ++	2.65	ns
--	2.65	ns
IEE	1.30	mA I/O
FAN-OUT LOAD LIMIT:	50	loads
k-FACTOR RISING	0.030	ns/LU
FALLING	0.034	ns/LU

Y = PAD



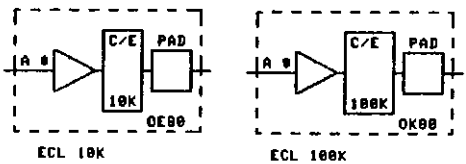
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC Q14000B/Q6000B ONLY

0x80 1 I/O cell	ECL OUTPUT	
	OE70;OK70	
Tpd		
A->PAD ++	0.70	ns
--	1.00	ns
IEE	4.60	mA I/O
FAN-OUT LOAD LIMIT:	1	loads
k-FACTOR RISING	0.045	ns/pF
FALLING	0.045	ns/pF

* A COUNTS AS 3 LOADS

PAD = A

OE80: 10K ECL
OK80: 100K ECL



Section 6-4:

Basic Logic Macros

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

EX06 1 B cell EXCLUSIVE OR

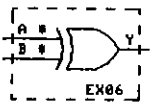
		S	
Tpd A->Y(B=0)	++	1.36	ns
	--	1.97	ns
B->Y(A=0)	++	1.20	ns
	--	1.36	ns
A->Y(B=1)	+-	0.60	ns
	-+	0.90	ns
B->Y(A=1)	+-	1.20	ns
	-+	1.54	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* A COUNTS AS 3 LOADS
* B COUNTS AS 2 LOADS

A ⊕ B = Y

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

EX08 1 B cell EXCLUSIVE NOR

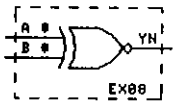
		S	
Tpd A->YN(B=0)	+-	0.61	ns
	-+	0.88	ns
B->YN(A=0)	+-	1.25	ns
	-+	1.71	ns
A->YN(B=1)	++	1.37	ns
	--	1.95	ns
B->YN(A=1)	++	0.99	ns
	--	1.44	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR RISING		0.025	ns/LU
FALLING		0.025	ns/LU

---

* A COUNTS AS 3 LOADS
* B COUNTS AS 2 LOADS

$$YN = \overline{A \oplus B}$$

A	B	YN
0	0	1
0	1	0
1	0	0
1	1	1



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

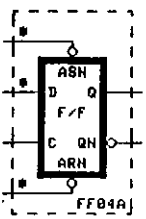
FF04A 3 B cells D-FLIP-FLOP, ASN, ARN, Q, QN

			S	
Tpd	C->Q	++	1.91	ns
		+-	1.67	ns
	C->QN	++	2.68	ns
		+-	2.66	ns
	ASN->Q	-+	3.29	ns
	ASN->QN	--	1.34	ns
	ARN->Q	--	2.13	ns
	ARN->QN	-+	3.13	ns
Tsu	(D)		1.00	ns
Th	(D)		0.50	ns
Trec	(ARN)		1.00	ns
Trec	(ASN)		0.50	ns
PW	(C)		1.85	ns
PW	(ASN,ARN)		1.95	ns
FAN-OUT LOAD LIMIT:Q,QN			30	loads
k-FACTOR	RISING Q,QN		0.025	ns/LU
	FALLING		0.025	ns/LU

---

* ASN, ARN, D COUNT AS 2 LOADS EACH

C	D	ASN	ARN	Qn+1	QNn+1
R	0	1	1	0	1
R	1	1	1	1	0
F	X	1	1	Qn	QNn
X	X	0	1	1	0
X	X	1	0	0	1
X	X	0	0	X	X



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

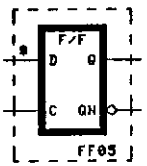
FF05 2 B cells D-FLIP-FLOP, Q, QN

		S	
Tpd C->Q	++	1.96	ns
	+-	1.83	ns
C->QN	++	2.55	ns
	+-	2.65	ns
Tsu (D)		0.70	ns
Th (D)		0.80	ns
PW (C)		1.55	ns
FAN-OUT LOAD LIMIT:Q,QN		30	loads
k-FACTOR RISING	Q,QN	0.025	ns/LU
FALLING		0.025	ns/LU

---

* D COUNTS AS 2 LOADS

C	D	Qn+1	QNn+1
R	0	0	1
R	1	1	0
F	X	Qn	QNn
0	X	Qn	QNn
1	X	Qn	QNn



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

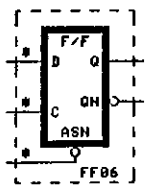
FF06 2 B cells D-FLIP-FLOP, Q, QN, ASN

		S	
Tpd C->Q	++	1.22	ns
	+-	1.69	ns
C->QN	++	2.26	ns
	+-	1.54	ns
ASN->Q	-+	0.70	ns
ASN->QN	--	1.00	ns
Tsu (D)		1.35	ns
Th (D)		0.15	ns
Trec(ASN)		0.50	ns
PW (C)		1.70	ns
PW (ASN)		1.95	ns
FAN-OUT LOAD LIMIT:Q,QN		30	loads
k-FACTOR	RISING Q,QN	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* D COUNTS AS 2 LOADS
* C, ASN COUNTS AS 3 LOADS

C	D	ASN	Qn+1	QNn+1
R	0	1	0	1
R	1	1	1	0
F	X	1	Qn	QNn
X	X	0	1	0



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

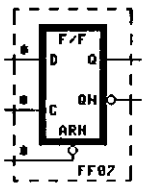
FF07 2 B cells D-FLIP-FLOP, Q, QN, ARN

		S	
Tpd C->Q	++	1.47	ns
	+-	1.43	ns
C->QN	++	2.45	ns
	+-	2.02	ns
ARN->Q	--	2.20	ns
ARN->QN	-+	3.42	ns
Tsu (D)		1.70	ns
Th (D)		0.00	ns
Trec(ARN)		1.30	ns
PW (C)		1.70	ns
PW (ARN)		1.95	ns
FAN-OUT LOAD LIMIT: Q,QN		30	loads
k-FACTOR	RISING Q,QN	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ARN, D COUNT AS 2 LOADS EACH
* C COUNTS AS 3 LOADS

C	D	ARN	Qn+1	QNn+1
R	0	1	0	1
R	1	1	1	0
F	X	1	Qn	QNn
X	X	0	0	1



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

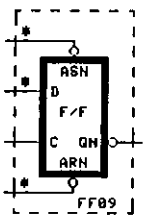
FF09 2 B cells D FLIP-FLOP, QN, ASN, ARN

		S	
Tpd C->QN	++	2.25	ns
	+-	2.31	ns
ARN->QN	-+	0.54	ns
ASN->QN	--	1.98	ns
Tsu (D)		1.00	ns
Th (D)		0.50	ns
Trec(ARN)		1.00	ns
Trec(ASN)		0.50	ns
PW (C)		1.85	ns
PW (ARN,ASN)		1.95	ns
FAN-OUT LOAD LIMIT :		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* D, ARN, ASN COUNT AS 2 LOADS EACH

C	D	ASN	ARN	QNn+1
R	0	1	1	1
R	1	1	1	0
F	X	1	1	QNn
X	X	0	1	0
X	X	1	0	1
X	X	0	0	X



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

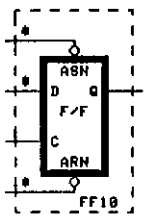
FF10 2 B cells D FLIP-FLOP, Q, ASN, ARN

		S	
Tpd C->Q	++	1.74	ns
	+-	1.72	ns
ARN->Q	--	2.20	ns
ASN->Q	-+	0.52	ns
Tsu (D)		1.00	ns
Th (D)		0.50	ns
Trec(ARN)		1.00	ns
Trec(ASN)		0.50	ns
PW (C)		1.85	ns
PW (ARN,ASN)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* D, ARN, ASN COUNT AS 2 LOADS EACH

C	D	ASN	ARN	QNn+1
R	0	1	1	0
R	1	1	1	1
F	X	1	1	Qn
X	X	0	1	1
X	X	1	0	0
X	X	0	0	X



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

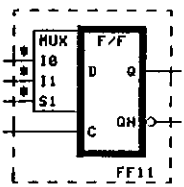
FF11 3 B cells D-FLIP-FLOP WITH 2:1 MUX

		S	
Tpd C->Q	++	2.56	ns
	+-	2.70	ns
C->QN	++	1.97	ns
	+-	1.85	ns
Tsu (I0,I1)		1.50	ns
Tsu (S1)		1.90	ns
Th (I0,I1)		0.00	ns
Th (S1)		0.00	ns
PW (C)		1.55	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR RISING		0.025	ns/LU
FALLING		0.025	ns/LU

---

* I0, I1, S1 COUNT AS 2 LOADS EACH

S1	I0	I1	C	Qn+1	QNn+1
X	X	X	0	Qn	QNn
X	X	X	1	Qn	QNn
0	0	X	R	0	1
0	1	X	R	1	0
1	X	0	R	0	1
1	X	1	R	1	0
X	0	0	R	0	1
X	0	1	R	UNKNOWN	
X	1	0	R	UNKNOWN	
X	1	1	R	1	0
X	X	X	F	Qn	QNn



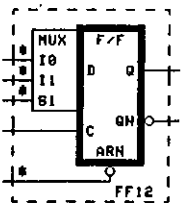
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

FF12 3 B cells D-FLIP-FLOP WITH 2:1 MUX, ARN

		S	
Tpd C->Q	++	3.06	ns
	+-	2.79	ns
C->QN	++	1.97	ns
	+-	1.84	ns
ARN->Q	--	1.63	ns
ARN->QN	-+	2.85	ns
Tsu (I0,I1)		1.50	ns
Tsu (S1)		2.70	ns
Th (I0,I1)		0.00	ns
Th (S1)		0.00	ns
Trec(ARN)		0.50	ns
PW (C)		1.70	ns
PW (ARN)		1.95	ns
FAN-OUT LOAD LIMIT:Q,QN		30	loads
k-FACTOR	RISING Q,QN	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ARN, I0, I1, S1 COUNT AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

FF12 3 B cells D-FLIP-FLOP WITH 2:1 MUX, ARN

ARN	S1	I0	I1	C	Qn+1	QNn+1
1	X	X	X	0	Qn	QNn
1	X	X	X	1	Qn	QNn
1	0	0	X	R	0	1
1	0	1	X	R	1	0
1	1	X	0	R	0	1
1	1	X	1	R	1	0
1	X	0	0	R	0	1
1	X	0	1	R	UNKNOWN	
1	X	1	0	R	UNKNOWN	
1	X	1	1	R	1	0
0	X	X	X	X	0	1
1	X	X	X	F	Qn	QNn

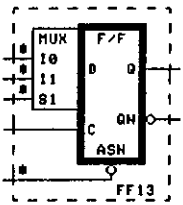
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

FF13 3 B cells D-FLIP-FLOP WITH 2:1 MUX, ASN

		S	
Tpd C->Q	++	2.54	ns
	+-	2.95	ns
C->QN	++	2.12	ns
	+-	1.84	ns
ASN->Q	-+	3.05	ns
ASN->QN	--	2.36	ns
Tsu (I0,I1)		1.80	ns
Tsu (S1)		3.00	ns
Th (I0,I1)		0.00	ns
Th (S1)		0.00	ns
Trec(ASN)		1.00	ns
PW (C)		1.70	ns
PW (ASN)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ASN, I0, I1, S1 COUNT AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

FF13 3 B cells D-FLIP-FLOP WITH 2:1 MUX, ASN

ASN	Sl	I0	Il	C	Qn+1	QNn+1
1	X	X	X	0	Qn	QNn
1	X	X	X	1	Qn	QNn
1	0	0	X	R	0	1
1	0	1	X	R	1	0
1	1	X	0	R	0	1
1	1	X	1	R	1	0
1	X	0	0	R	0	1
1	X	0	1	R	UNKNOWN	
1	X	1	0	R	UNKNOWN	
1	X	1	1	R	1	0
0	X	X	X	X	1	0
1	X	X	X	F	Qn	QNn

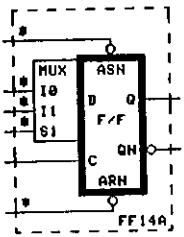
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

FF14A 3 B cells D-FLIP-FLOP WITH 2:1 MUX, ASN, ARN

		S	
Tpd C->Q	++	2.68	ns
	+-	2.92	ns
C->QN	++	1.98	ns
	+-	1.76	ns
ARN->Q	--	1.07	ns
ARN->QN	-+	2.62	ns
ASN->Q	-+	2.79	ns
ASN->QN	--	1.94	ns
Tsu (I0,I1)		1.70	ns
Th (I0,I1)		0.00	ns
Tsu (S1)		2.60	ns
Th (S1)		0.00	ns
Trec(ARN)		0.50	ns
Trec(ASN)		1.00	ns
PW (C)		1.85	ns
PW (ASN,ARN)		1.95	ns
FAN-OUT LOAD LIMIT:Q,QN		30	loads
k-FACTOR RISING	Q,QN	0.025	ns/LU
FALLING		0.025	ns/LU

---

* ASN, ARN, I0, I1, S1 COUNTS AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

FF14A 3 B cells D-FLIP-FLOP WITH 2:1 MUX, ASN, ARN

When ARN and ASN go inactive within lns of each other, the outputs of the EWS model for FF14A will go into the "UNKNOWN" state. Some Tpd delays for recovering from the UNKNOWN may vary from those of the normal operation defined above.

C	D	ASN	ARN	Qn+1	QNn+1
R	0	1	1	0	1
R	1	1	1	1	0
X	X	0	1	1	0
X	X	1	0	0	1
X	X	0	0	0	1

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

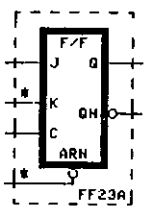
FF23A 4 B cells J-K FLIP-FLOP, ARN

			S	
Tpd	C->Q	++	2.02	ns
		+-	1.80	ns
	C->QN	++	2.59	ns
		+-	2.93	ns
	ARN->Q	--	1.96	ns
	ARN->QN	-+	2.74	ns
Tsu(J,K)			4.20	ns
Th (J,K)			0.00	ns
Trec(ARN)			1.00	ns
PW(C)			1.70	ns
PW(ARN)			1.95	ns
FAN-OUT LOAD LIMIT:			30	loads
k-FACTOR	RISING		0.025	ns/LU
	FALLING		0.025	ns/LU

---

* ARN COUNTS AS 3 LOADS, K COUNTS AS 2 LOADS

C	J	K	ARN	Qn+1	QNn+1
R	0	0	1	Qn	QNn
R	0	1	1	0	1
R	1	0	1	1	0
R	1	1	1	QNn	Qn
F	X	X	1	Qn	QNn
X	X	X	0	0	1



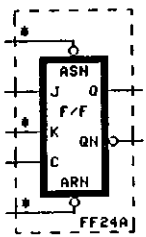
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

FF24A 4 B cells J-K FLIP-FLOP, ASN, ARN

		S	
Tpd C->Q	++	1.78	ns
	+-	1.75	ns
C->QN	++	2.60	ns
	+-	2.86	ns
ARN->Q	--	2.22	ns
ARN->QN	-+	2.52	ns
ASN->Q	-+	2.85	ns
ASN->QN	--	1.23	ns
Tsu (J,K)		3.60	ns
Th (J,K)		0.00	ns
Trec(ARN)		1.00	ns
Trec(ASN)		0.50	ns
PW (C)		1.85	ns
PW (ARN,ASN)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ARN, ASN, K COUNT AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

FF24A 4 B cells J-K FLIP-FLOP, ASN, ARN

C	J	K	ASN	ARN	Qn+1	QNn+1
R	0	0	1	1	Qn	QNn
R	0	1	1	1	0	1
R	1	0	1	1	1	0
R	1	1	1	1	QNn	Qn
F	X	X	1	1	Qn	QNn
X	X	X	0	1	1	0
X	X	X	1	0	0	1
X	X	X	0	0	0	0

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

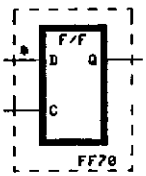
FF70 2 B cells METASTABLE HARDENED D-FLIP-FLOP, Q

		S	
Tpd C->Q	++	2.11	ns
	+-	1.65	ns
Tsu (D)		0.75	ns
Th (D)		0.75	ns
PW		1.55	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* D COUNTS AS 2 LOADS

C	D	Qn+1
R	0	0
R	1	1
F	X	Qn
0	x	Qn
1	x	Qn



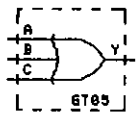
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT05 1 B cell 3-INPUT OR

		S	
Tpd A->Y	++	1.02	ns
	--	1.47	ns
B->Y	++	0.94	ns
	--	1.46	ns
C->Y	++	1.11	ns
	--	1.01	ns
(2 INPUTS CHANGING)			
A,B->Y	++	0.75	ns
	--	1.67	ns
B,C->Y	++	0.73	ns
	--	1.47	ns
A,C->Y	++	0.77	ns
	--	1.49	ns
(ALL INPUTS CHANGING)			
A,B,C->Y	++	0.61	ns
	--	1.69	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

Y= A + B + C

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

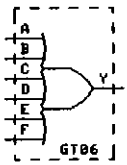


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT06 2 B cell 6-INPUT OR

		S	
Tpd A->Y	++	1.31	ns
	--	1.51	ns
B->Y	++	1.23	ns
	--	1.52	ns
C->Y	++	1.40	ns
	--	1.61	ns
D->Y	++	1.33	ns
	--	1.60	ns
E->Y	++	1.63	ns
	--	1.62	ns
F->Y	++	1.54	ns
	--	1.61	ns
(ALL INPUTS CHANGING) A,B,C, D,E,F->Y	++	0.57	ns
	--	2.05	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

Y = A + B + C + D + E + F

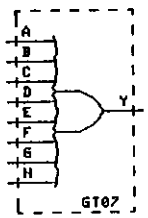


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT07 3 B cell 8-INPUT OR

		S	
Tpd A->Y	++	2.12	ns
	--	2.17	ns
B->Y	++	2.05	ns
	--	2.16	ns
C->Y	++	2.46	ns
	--	2.21	ns
D->Y	++	2.38	ns
	--	2.20	ns
E->Y	++	2.33	ns
	--	2.31	ns
F->Y	++	2.53	ns
	--	2.29	ns
G->Y	++	2.29	ns
	--	2.28	ns
H->Y	++	2.23	ns
	--	2.26	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

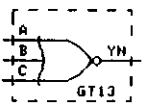
Y = A + B + C + D + E + F + G + H



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT13	1 B Cell	3-INPUT NOR	
		S	
(1 INPUT CHANGING)			
Tpd A->YN	+-	1.20	ns
	-+	1.96	ns
B->YN	+-	1.13	ns
	-+	1.92	ns
C->YN	+-	1.25	ns
	-+	1.52	ns
(2 INPUTS CHANGING)			
A,B->YN	+-	0.97	ns
	-+	2.12	ns
A,C->YN	+-	0.91	ns
	-+	2.00	ns
B,C->YN	+-	0.87	ns
	-+	1.97	ns
(ALL INPUTS CHANGING)			
A,B,C->YN	+-	0.76	ns
	-+	2.16	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

$YN = \overline{A + B + C}$

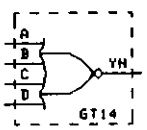


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT14 2 B cell 4-INPUT NOR

		S	
(1 INPUT CHANGING)			
Tpd A->YN	+-	1.64	ns
	-+	1.79	ns
B->YN	+-	1.36	ns
	-+	1.75	ns
C->YN	+-	1.65	ns
	-+	1.67	ns
D->YN	+-	1.36	ns
	-+	1.64	ns
(2 INPUTS CHANGING)			
A,B->YN	+-	1.05	ns
	-+	1.85	ns
A,C->YN	+-	1.50	ns
	-+	1.78	ns
A,D->YN	+-	1.33	ns
	-+	1.75	ns
B,C->YN	+-	1.34	ns
	-+	1.76	ns
C,D->YN	+-	1.05	ns
	-+	1.75	ns
B,D->YN	+-	1.25	ns
	-+	1.74	ns
(ANY 3 INPUTS CHANGING)			
	+-	1.05	ns
	-+	1.83	ns
(ALL INPUTS CHANGING)			
	+-	0.96	ns
	-+	1.84	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR RISING		0.030	ns/LU
FALLING		0.025	ns/LU

$YN = \overline{A + B + C + D}$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT15 1 B cell DUAL 2-INPUT NOR

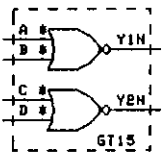
		S	
(1 INPUT CHANGING)			
Tpd A->Y1N	+-	0.36	ns
	-+	1.15	ns
D->Y2N	+-	0.36	ns
	-+	1.15	ns
B->Y1N	+-	0.36	ns
	-+	1.26	ns
C->Y2N	+-	0.36	ns
	-+	1.26	ns
(2 INPUTS CHANGING)			
A,B->Y1N	+-	0.13	ns
	-+	1.30	ns
C,D->Y2N	+-	0.13	ns
	-+	1.30	ns
FAN-OUT LOAD LIMIT:		Y1N, Y2N 30	loads
k-FACTOR	RISING	Y1N, Y2N 0.030	ns/LU
	FALLING	0.025	ns/LU

---

* A, B, C, D COUNT AS 2 LOADS EACH

$Y1N = \overline{A + B}$

$Y2N = \overline{C + D}$

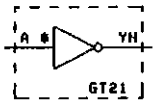


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT21 1 B cell HIGH-FAN-OUT INVERTING DRIVER

		S	
Tpd A->YN	+-	0.40	ns
	-+	0.66	ns
FAN-OUT LOAD LIMIT:		50	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

$YN = \overline{A}$

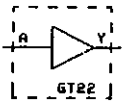


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT22 1 B cell HIGH-FAN-OUT DRIVER, NON-INVERTING

		S	
Tpd A->Y	++	0.86	ns
	--	1.16	ns
FAN-OUT LOAD LIMIT:		50	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

Y = A



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT23 1 B cell DUAL INVERTER

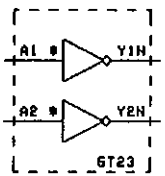
			S	
Tpd	A1->Y1N	+-	0.33	ns
		-+	0.59	ns
	A2->Y2N	+-	0.33	ns
		-+	0.59	ns
FAN-OUT LOAD LIMIT:			Y1N, Y2N 30	loads
k-FACTOR	RISING		Y1N, Y2N 0.025	ns/LU
	FALLING		0.025	ns/LU

---

* A1, A2 COUNT AS 2 LOADS EACH

$Y1N = \overline{\overline{A1}}$

$Y2N = \overline{\overline{A2}}$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT34A 2 B cell 5-INPUT AND

			S	
(1 INPUT CHANGING)				
Tpd	A->Y	++	1.08	ns
		--	0.93	ns
	B->Y	++	1.06	ns
		--	1.09	ns
	C->Y	++	1.22	ns
		--	0.94	ns
	D->Y	++	1.28	ns
		--	1.11	ns
	E->Y	++	1.41	ns
		--	1.31	ns
(2 INPUTS CHANGING)				
	A,B->Y	++	1.23	ns
		--	0.64	ns
	A,C->Y	++	1.26	ns
		--	0.82	ns
	A,D->Y	++	1.34	ns
		--	0.88	ns
	A,E->Y	++	1.45	ns
		--	0.91	ns
	B,C->Y	++	1.28	ns
		--	0.88	ns
	B,D->Y	++	1.36	ns
		--	0.97	ns
	B,E->Y	++	1.48	ns
		--	1.04	ns
	C,D->Y	++	1.43	ns
		--	0.64	ns
	C,E->Y	++	1.39	ns
		--	0.64	ns
	D,E->Y	++	1.46	ns
		--	0.72	ns
(ALL INPUTS CHANGING)				
A,B,C,D,E->Y		++	1.58	ns
		--	0.49	ns

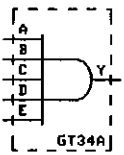
con't

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT34A 2 B cell 5-INPUT AND

		S	
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.030	ns/LU
	FALLING	0.025	ns/LU

Y = A.B.C.D.E



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT35 1 B cell 4-INPUT NAND

			S	
(1 INPUT CHANGING)				
Tpd	A->YN	-+	0.70	ns
		+-	0.47	ns
	B->YN	-+	0.79	ns
		+-	0.61	ns
	C->YN	-+	0.89	ns
		+-	0.79	ns
	D->YN	-+	0.95	ns
		+-	0.87	ns
(2 INPUTS CHANGING)				
	A,B->YN	-+	0.46	ns
		+-	0.68	ns
	A,C->YN	-+	0.43	ns
		+-	0.73	ns
	A,D->YN	-+	0.41	ns
		+-	0.75	ns
	B,C->YN	-+	0.48	ns
		+-	0.78	ns
	B,D->YN	-+	0.45	ns
		+-	0.80	ns
	C,D->YN	-+	0.50	ns
		+-	0.96	ns
(ANY 3 INPUTS CHANGING)				
		+-	0.91	ns
		-+	0.37	ns
(ALL INPUTS CHANGING)				
		+-	0.99	ns
		-+	0.28	ns

con't

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

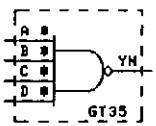
GT35 1 B cell 4-INPUT NAND

		S	
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.030	ns/LU

---

* A, B, C, D COUNT AS 2 LOADS EACH

$YN = \overline{A.B.C.D}$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT38A 2 B cells 8-INPUT AND GATE

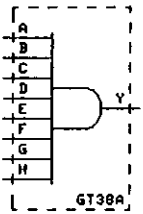
			S	
(1 INPUT CHANGING)				
Tpd	A->Y	++	2.19	ns
		--	1.41	ns
	B->Y	++	2.08	ns
		--	1.33	ns
	C->Y	++	1.93	ns
		--	1.19	ns
	D->Y	++	1.82	ns
		--	1.03	ns
	E->Y	++	2.19	ns
		--	1.41	ns
	F->Y	++	2.08	ns
		--	1.33	ns
	G->Y	++	1.93	ns
		--	1.19	ns
	H->Y	++	1.82	ns
		--	1.03	ns
(2 INPUTS CHANGING)				
	A,E->Y	++	2.47	ns
		--	1.20	ns
	B,F->Y	++	2.39	ns
		--	1.11	ns
	C,G->Y	++	2.15	ns
		--	1.00	ns
	D,H->Y	++	1.93	ns
		--	0.86	ns
(ALL INPUTS CHANGING)				
		++	2.41	ns
		--	0.40	ns
			con't	

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT38A 2 B cells 8-INPUT AND GATE

		S	
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.030	ns/LU
	FALLING	0.025	ns/LU

Y = A.B.C.D.E.F.G.H



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT40 1 B cells DUAL 2-INPUT NAND

			S	
(1 INPUT CHANGING)				
Tpd	A->Y1N	+-	0.40	ns
		-+	0.63	ns
	C->Y2N	+-	0.40	ns
		-+	0.63	ns
	B->Y1N	+-	0.45	ns
		-+	0.72	ns
	D->Y2N	+-	0.45	ns
		-+	0.72	ns
(2 INPUTS CHANGING)				
	A,B->Y1N	+-	0.55	ns
		-+	0.39	ns
	C,D->Y2N	+-	0.55	ns
		-+	0.39	ns

FAN-OUT LOAD LIMIT: Y1N, Y2N 30 loads

k-FACTOR RISING Y1N, Y2N 0.025 ns/LU

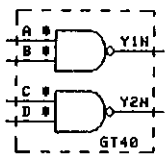
FALLING 0.025 ns/LU

---

* A, B, C, D COUNT AS 2 LOADS EACH

$Y1N = \overline{A\,B}$

$Y2N = \overline{C\,D}$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

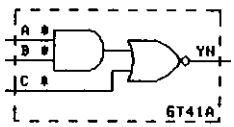
GT41A 1 B cell 2-WIDE 1-2 INPUT AND-OR INVERT

			S	
Tpd	A->YN	+-	0.82	ns
		-+	0.90	ns
	B->YN	+-	0.96	ns
		-+	0.93	ns
	C->YN	+-	1.01	ns
		-+	1.05	ns
FAN-OUT LOAD LIMIT:			30	loads
k-FACTOR	RISING		0.030	ns/LU
	FALLING		0.025	ns/LU

---

* A, B, C COUNT AS 2 LOADS EACH

$YN = \overline{(\overline{A.B}) + C}$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

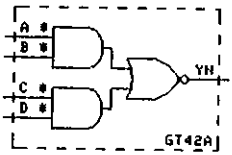
GT42A 1 B cell 2-WIDE 2-2 INPUT AND-OR INVERT

			S	
Tpd	A->YN	+-	0.68	ns
		-+	1.09	ns
	B->YN	+-	0.67	ns
		-+	1.37	ns
	C->YN	+-	0.84	ns
		-+	1.43	ns
	D->YN	+-	0.81	ns
		-+	1.71	ns
FAN-OUT LOAD LIMIT:			30	loads
k-FACTOR	RISING		0.030	ns/LU
	FALLING		0.030	ns/LU

* A, B, C, D COUNT AS 2 LOADS EACH

$YN = \overline{A.B + C.D}$

A	B	C	D	YN
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

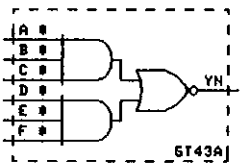
GT43A 2 B cell 2-WIDE 3-3 INPUT AND-OR INVERT

			S	
Tpd	A->YN	+-	0.81	ns
		-+	1.41	ns
	B->YN	+-	0.84	ns
		-+	1.71	ns
	C->YN	+-	0.87	ns
		-+	1.84	ns
	D->YN	+-	1.25	ns
		-+	1.71	ns
	E->YN	+-	1.29	ns
		-+	1.99	ns
	F->YN	+-	1.38	ns
		-+	2.12	ns
FAN-OUT LOAD LIMIT:			30	loads
k-FACTOR	RISING		0.035	ns/LU
	FALLING		0.040	ns/LU

---

* A,B,C,D,E,F COUNTS AS 2 LOADS EACH

$$YN = (\overline{A.B.C}) + (\overline{D.E.F})$$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

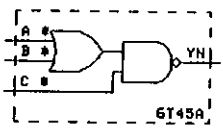
GT45A 1 B cell 2-WIDE 1-2 INPUT OR-AND INVERT

			S	
Tpd	A->YN	+-	0.67	ns
		-+	1.10	ns
	B->YN	+-	0.82	ns
		-+	1.21	ns
	C->YN	+-	0.72	ns
		-+	0.59	ns
FAN-OUT LOAD LIMIT:			30	loads
k-FACTOR	RISING		0.030	ns/LU
	FALLING		0.030	ns/LU

---

* A, B, C COUNT AS 2 LOADS EACH

$YN = \overline{(A+B).C}$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT46A 1 B cell 2-WIDE 2-2 INPUT OR-AND INVERT

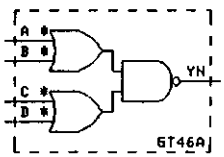
			S	
Tpd	A->YN	+-	0.86	ns
		-+	1.13	ns
	B->YN	+-	0.92	ns
		-+	1.22	ns
	C->YN	+-	0.71	ns
		-+	1.19	ns
	D->YN	+-	0.77	ns
		-+	1.27	ns
FAN-OUT LOAD LIMIT:			30	loads
k-FACTOR	RISING		0.030	ns/LU
	FALLING		0.030	ns/LU

---

* A, B, C, D COUNT AS 2 LOADS EACH

$YN = \overline{(\overline{A+B}).(\overline{C+D})}$

A	B	C	D	YN
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

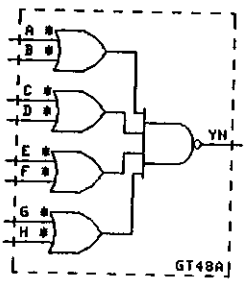
GT48A 2 B cells 4-WIDE 2-2-2-2 INPUT OR-AND INVERT

			S	
Tpd	A->YN	+-	0.98	ns
		-+	1.07	ns
	B->YN	+-	1.06	ns
		-+	1.16	ns
	C->YN	+-	1.26	ns
		-+	1.72	ns
	D->YN	+-	1.37	ns
		-+	1.79	ns
	E->YN	+-	1.78	ns
		-+	2.31	ns
	F->YN	+-	1.95	ns
		-+	2.38	ns
	G->YN	+-	2.01	ns
		-+	2.08	ns
	H->YN	+-	2.02	ns
		-+	2.75	ns
FAN-OUT LOAD LIMIT:			30	loads
k-FACTOR	RISING		0.035	ns/LU
	FALLING		0.040	ns/LU

---

*A, B, C, D, E, F, G, H COUNT AS 2 LOADS EACH

$$YN = \overline{(A+B).(C+D).(E+F).(G+H)}$$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

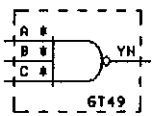
GT49 1 B cells 3-INPUT NAND

			S	
(1 INPUT CHANGING)				
Tpd	A->YN	+-	0.67	ns
		-+	0.86	ns
	B->YN	+-	0.71	ns
		-+	1.05	ns
	C->YN	+-	0.48	ns
		-+	0.77	ns
(2 INPUTS CHANGING)				
	A,B->YN	+-	0.77	ns
		-+	0.51	ns
	A,C->YN	+-	0.73	ns
		-+	0.45	ns
	B,C->YN	+-	0.65	ns
		-+	0.48	ns
(ALL INPUTS CHANGING)				
	A,B,C-YN	+-	0.83	ns
		-+	0.36	ns
FAN-OUT LOAD LIMIT:			30	loads
k-FACTOR		RISING	0.025	ns/LU
		FALLING	0.025	ns/LU

---

* A, B, C COUNT AS 2 LOADS EACH

$YN = \overline{A.B.C}$

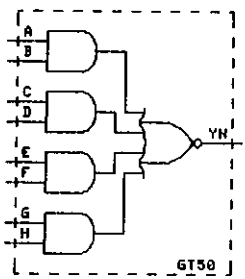


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT50 2 B cell 4 WIDE 2-2-2-2 INPUT AND - OR INVERT

			S	
Tpd	A->YN	+-	1.77	ns
		-+	2.15	ns
	B->YN	+-	1.88	ns
		-+	2.70	ns
	C->YN	+-	1.98	ns
		-+	2.22	ns
	D->YN	+-	2.06	ns
		-+	2.73	ns
	E->YN	+-	2.04	ns
		-+	2.14	ns
	F->YN	+-	2.16	ns
		-+	2.67	ns
	G->YN	+-	2.26	ns
		-+	2.22	ns
	H->YN	+-	2.36	ns
		-+	2.71	ns
FAN-OUT LOAD LIMIT:			30	loads
k-FACTOR	RISING		0.025	ns/LU
	FALLING		0.025	ns/LU

$YN = \overline{A.B + C.D + E.F + G.H}$

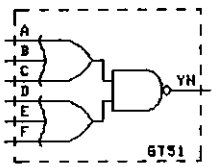


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT51 2 B cell 2-WIDE 3-3 INPUT OR - AND INVERT

			S	
Tpd	A->YN	+-	1.15	ns
		-+	1.99	ns
	B->YN	+-	1.29	ns
		-+	2.06	ns
	C->YN	+-	1.47	ns
		-+	2.16	ns
	D->YN	+-	1.19	ns
		-+	2.16	ns
	E->YN	+-	1.33	ns
		-+	2.23	ns
	F->YN	+-	1.51	ns
		-+	2.33	ns
FAN-OUT LOAD LIMIT:			30	loads
k-FACTOR	RISING		0.030	ns/LU
	FALLING		0.025	ns/LU

$YN = \overline{(A+B+C)(D+E+F)}$



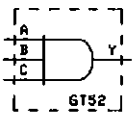
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

GT52 1 B cell 3-INPUT AND

			S	
(1 INPUT CHANGING)				
Tpd	A->Y	++	1.19	ns
		--	1.04	ns
	B->Y	++	1.41	ns
		--	1.42	ns
	C->Y	++	1.47	ns
		--	1.59	ns
(2 INPUTS CHANGING)				
	A,B->Y	++	1.37	ns
		--	0.70	ns
	A,C->Y	++	1.32	ns
		--	0.69	ns
	B,C->Y	++	1.57	ns
		--	0.88	ns
(ALL INPUTS CHANGING)				
	A,B,C->Y	++	1.49	ns
		--	0.56	ns
FAN-OUT LOAD LIMIT:			30	loads
k-FACTOR		RISING	0.025	ns/LU
		FALLING	0.025	ns/LU

Y = A.B.C

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

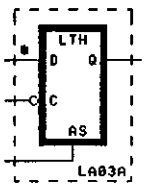


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

LA03A 1 B cell		LATCH WITH ASYNC. SET	
		S	
Tpd C->Q	-+	1.55	ns
	--	2.36	ns
D->Q	++	1.00	ns
	--	1.63	ns
AS->Q	++	0.85	ns
	--	1.49	ns
Tsu (D)		1.20	ns
Th (D)		0.30	ns
Trec(AS)		1.60	ns
PW (C)		1.70	ns
PW (AS)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

* D,C COUNTS AS 2 LOADS EACH

C	D	AS	Qn+1
0	0	0	0
0	1	0	1
1	X	0	Qn
X	X	1	1

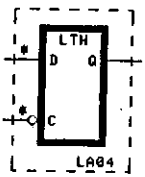


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

LA04 1 B cell		LATCH TRANSPARENT LOW	
		S	
Tpd C->Q	-+	2.79	ns
	--	3.13	ns
D->Q	++	1.55	ns
	--	2.05	ns
Tsu (D)		1.00	ns
Th (D)		0.50	ns
PW (C)		2.10	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

* C COUNTS AS 2 LOADS
* D COUNTS AS 2 LOADS

C	D	Qn+1
0	0	0
0	1	1
1	X	Qn



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

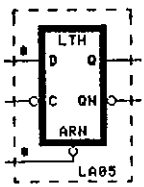
LA05 2 B cell LATCH WITH ACTIVE LOW RESET

		S	
Tpd C->Q	-+	2.81	ns
	--	2.78	ns
C->QN	-+	2.31	ns
	--	2.21	ns
D->Q	++	1.51	ns
	--	1.58	ns
D->QN	+-	0.91	ns
	-+	1.11	ns
ARN->Q	--	1.24	ns
ARN->QN	-+	0.73	ns
Tsu (D)		1.00	ns
Th (D)		0.50	ns
Trec(ARN)		0.00	ns
PW (ARN)		2.10	ns
PW (C)		2.30	ns
FAN-OUT LOAD LIMIT:	Q, QN	30	loads
k-FACTOR	RISING Q,QN	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* D,ARN COUNTS AS 2 LOADS

C	D	ARN	Qn+1	QNn+1
0	0	1	0	1
0	1	1	1	0
1	X	1	Qn	QNn
X	X	0	0	1



Section 6-5:

MSI Macros

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

ADD283A 15 B cells 4-BIT CARRY LOOK-AHEAD ADDER; CO

			S	
Tpd	Ai,Bi->Si	++	5.80	ns
		--	5.40	ns
		+-	5.80	ns
		-+	5.30	ns
	Ai,Bi->CO	++	4.80	ns
		--	4.80	ns
	CI->CO	++	2.40	ns
		--	2.70	ns
	CI->Si	++	4.60	ns
		--	4.90	ns
		+-	4.50	ns
		-+	4.70	ns

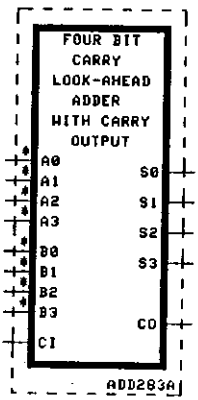
i = 0,1,2,3

FAN-OUT LOAD LIMIT: Si, CO 30 loads

k-FACTOR RISING Si,CO 0.025 ns/LU
FALLING 0.025 ns/LU

---

* Ai,Bi COUNTS AS 2 LOADS EACH
i = 0,1,2,3



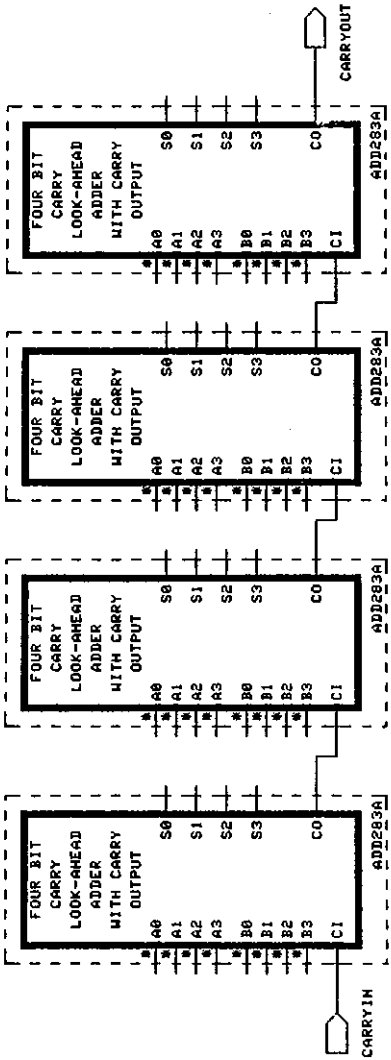
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

ADD283A 16 B cells 4-BIT CARRY LOOK-AHEAD ADDER; CO

ADD283A is a fast 4-bit binary full adder with carry look-ahead. ADD283A adds two 4-bit binary words (A3-A0, B3-B0) plus the incoming carry (CI) and generates the binary sum bits (S3-S0) and the carry-out (CO). ADD283 operates with either active-high or active-low operands (positive or negative logic).

```
                    CI
     A3   A2   A1   A0
+    B3   B2   B1   B0
-------------------------
CO   S3   S2   S1   S0
```

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

CMP688 6 B cells 8-BIT MAGNITUDE COMPARATOR

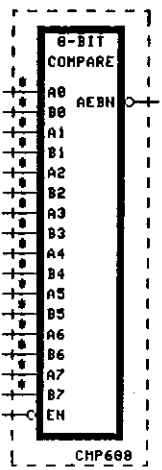
		S	
Tpd Ai->AEBN	++	2.55	ns
	-+	2.19	ns
	+-	4.17	ns
	--	4.97	ns
Bi->AEBN	++	2.58	ns
	-+	2.56	ns
	+-	4.60	ns
	--	4.62	ns
EN->AEBN	++	0.86	ns
	--	2.29	ns

i = 0,1,2,3,4,5,6,7

FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ALL Ai, Bi INPUTS COUNT AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

CMP688 6 B cells 8-BIT MAGNITUDE COMPARATOR

CMP688 compares A7-A0 and B7-B0, the magnitudes of two 8-bit binary words. The output (AEBN) is LOW if the magnitudes of the input words are equal. For all other conditions, the output is HIGH. When the enable input (EN) is HIGH, it overrides the result of the comparison and forces the output HIGH. Note that the Ai, Bi inputs are interleaved for this macro.

FUNCTION TABLE

INPUTS DATA Ai;Bi	ENABLE EN	OUTPUT AEBN	where A and B are binary words
A=B	0	0	if all Ai bits equal all Bi bits
A>B	0	1	if the sum of the Ai bits is Greater than the sum of the Bi bits
A<B	0	1	if the sum of the Ai bits is Less than the sum of the Bi bits
X	1	1	if CMP688 is disabled

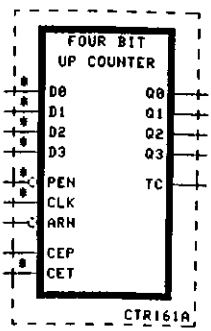
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

CTR161A 18 B cells 4-BIT UP COUNTER W/ASYNC. RESET

		S	
Tpd CLK->Qi	++	1.87	ns
	+-	1.84	ns
CLK->TC	++	3.20	ns
	+-	2.80	ns
ARN->Qi	--	3.00	ns
ARN->TC	--	3.96	ns
CET->TC	++	1.32	ns
	--	1.55	ns
i = 0,1,2,3			
Tsu (Di)		1.75	ns
Th (Di)		0.00	ns
i=0,1,2,3			
Tsu (PEN)		2.20	ns
Th (PEN)		0.00	ns
Tsu (CEP)		5.00	ns
Th (CEP)		0.00	ns
Trec(ARN)		1.45	ns
PW (ARN)		2.46	ns
PW (CLK)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING Qi	0.025	ns/LU
	FALLING	0.025	ns/LU
	RISING TC	0.025	ns/LU
	FALLING	0.025	ns/LU
MAXIMUM FREQUNCY		85	MHz COM5
OF OPERATION		75	MHz COM4
(fMAX)		70	MHz MIL

---

* Di,PEN,CLK,CET COUNT AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

CTR161A 18 B cells 4-BIT UP COUNTER W/ASYNC. RESET

CTR161A is synchronously presettable for applications such as programmable dividers. The LOW-active preset enable input (PEN) allows parallel loading of this counter with the contents of the data inputs (D3-D0) on the next rising edge of the clock input (CLK). This macro provides two types of count enable inputs (CEP, CET), and generates the teral count indicator (TC) to allow versatility in multi-stage synchronous counting. TC signals the following stage to advance on the next clock. Either CEP or CET will stop the counter from counting when disabled. CET will also force TC to zero. CTR161 has an asynchronous master reset (ARN) that overrides all other inputs and forces the outputs (Q3-Q0, TC) LOW.

FUNCTION TABLE

INPUTS						OUTPUTS
RESET ARN	LOAD PEN	ENABLE CEP	ENABLE CET	CLOCK CLK	Qi	TC
0	X	X	X	X	RESET Qi	0
1	0	X	1	R	LOAD	If sum Qi=15, TC=1 else TC=0
1	0	X	0	R	LOAD	0
1	1	0	1	X	STOP	If sum Qi=15, TC=1 else TC=0
1	1	X	0	X	STOP	0
1	1	1	1	R	COUNT UP	If sum Qi=15, TC=1 else TC=0
1	1	1	1	F	NO CHANGE	If sum Qi=15, TC=1 else TC=0

TC = Q3.Q2.Q1.Q0.CET . = AND
X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE

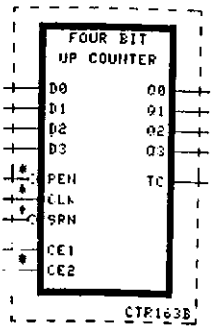
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

CTR163B 16 B cells 4-BIT UP COUNTER W/SYNC. RESET

		S	
Tpd CLK->Qi	++	1.90	ns
	+-	2.10	ns
CLK->TC	++	3.22	ns
	+-	3.35	ns
CE2->TC	++	1.32	ns
	--	1.21	ns
i = 0,1,2,3			
Tsu (SRN)		5.00	ns
Th (SRN)		0.00	ns
Tsu (PEN)		4.50	ns
Th (PEN)		0.00	ns
Tsu (CE1)		5.80	ns
Th (CE1)		0.00	ns
Tsu (CE2)		5.80	ns
Th (CE2)		0.00	ns
Tsu (Di)		5.00	ns
Th (Di)		0.00	ns
i=0,1,2,3			
PW (CLK)		2.22	ns
PW (SRN)		2.46	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING Qi	0.025	ns/LU
	FALLING	0.025	ns/LU
	RISING TC	0.025	ns/LU
	FALLING	0.025	ns/LU
MAXIMUM FREQUNCY		85	MHz COM5
OF OPERATION		75	MHz COM4
(fMAX)		70	MHz MIL

---

* PEN, CLK, CE2 COUNT AS 2 LOADS EACH
* SRN COUNTS AS 6 LOADS



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

CTR163B 16 B cells 4-BIT UP COUNTER W/SYNC. RESET

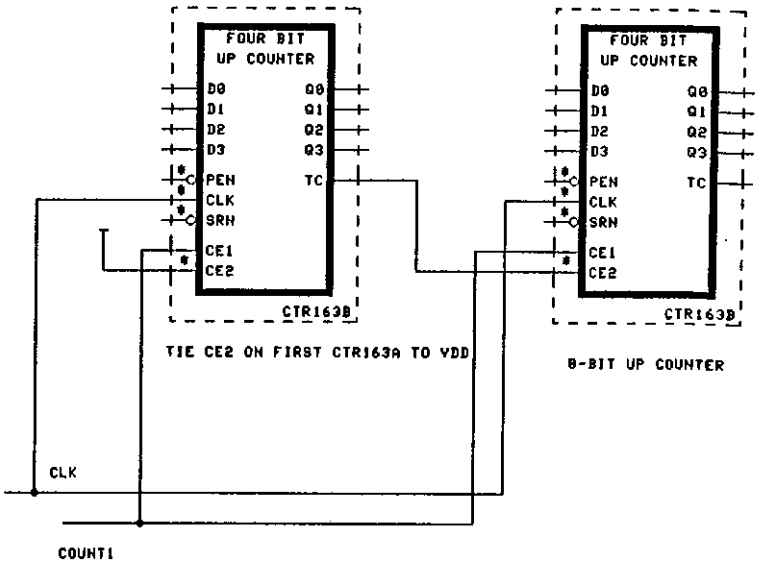
CTR163B is synchronously presettable for applications such as programmable dividers. The LOW-active preset enable input (PEN) allows presettable parallel loading of this counter with the contents of the data inputs (D0-D3) on the next rising edge of the clock (CLK). This macro provides two types of count enable inputs (CE1, CE2), and generates the teral count indicator (TC) to allow versatility in multi-stage synchronous counting. TC signals the following stage to advance on the next clock. Either CE1 or CE2 will stop the counter from counting when disabled. CE2 will also force TC to zero. CTR163B has a synchronous reset input (SRN) that overrides counting and parallel loading and allows the outputs (Q0-Q3, TC) to be simultaneously reset on the rising edge of the next clock input.

FUNCTION TABLE

INPUTS						OUTPUTS
RESET SRN	LOAD PEN	ENABLE CE1	ENABLE CE2	CLOCK CLK	Qi	TC
0	X	X	X	R	RESET Qi	0
1	0	X	1	R	LOAD	If sum Qi=15, TC=1 else TC=0
1	0	X	0	R	LOAD	0
1	1	0	1	X	STOP	If sum Qi=15, TC=1 else TC=0
1	1	X	0	X	STOP	0
1	1	1	1	R	COUNT UP	If sum Qi=15, TC=1 else TC=0
1	1	1	1	F	NO CHANGE	If sum Qi=15, TC=1 else TC=0

TC = Q3.Q2.Q1.Q0.CE2 . = AND
X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

DEC138A 7 B cells 3:8 DECODER WITH HIGH ENABLE

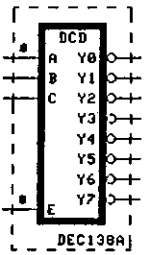
		S	
Tpd A->Yi	++	1.74	ns
	--	1.83	ns
	+-	1.44	ns
	-+	1.60	ns
B->Yi	++	1.83	ns
	--	2.87	ns
	+-	2.26	ns
	-+	1.68	ns
C->Yi	++	2.01	ns
	--	3.08	ns
	+-	2.37	ns
	-+	1.81	ns
E->Yi	+-	1.41	ns
	-+	1.76	ns

i = 0,1,2,3,4,5,6,7

FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* A, E COUNT AS 2 LOADS EACH
EACH OUTPUT HAS A FAN-OUT LIMIT OF 30



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

DEC138A 7 B cells 3:8 DECODER WITH HIGH ENABLE

DEC138A has three select inputs (A, B, C), and provides eight mutually exclusive, active LOW outputs (Y0-Y7). The enable input (E) can be used to select input when expanding to a 4:16 line decoder.

E	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0

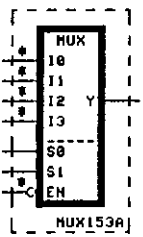
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

MUX153A 2 B cells 4:1 NON-INVRTNG. MUX W/ LO ENABLE

			S	
Tpd	EN->Y	+-	0.38	ns
		-+	0.86	ns
	Ii->Y	++	1.85	ns
		--	2.25	ns
	S0->Y	++	2.93	ns
		+-	3.25	ns
		-+	3.36	ns
		--	3.45	ns
	S1->Y	++	1.92	ns
		+-	1.63	ns
		-+	2.13	ns
		--	2.05	ns
i = 0,1,2,3				
FAN-OUT LOAD LIMIT:			30	loads
k-FACTOR	RISING		0.030	ns/LU
	FALLING		0.025	ns/LU

---

* EN COUNTS AS 2 LOADS
* Ii INPUTS COUNT AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

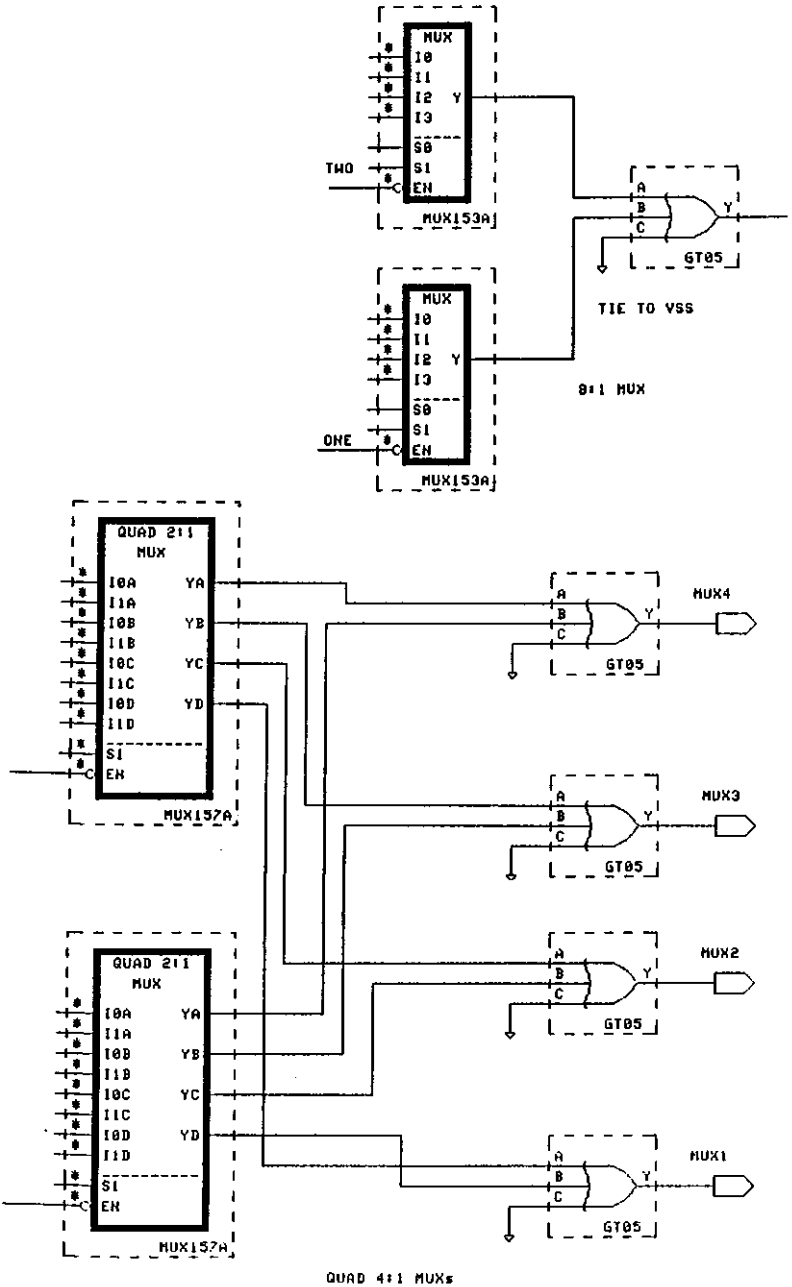
MUX153A 2 B cells 4:1 NON-INVRTNG. MUX W/ LO ENABLE

MUX153A selects one data input from four sources (I0-I3). Output (Y) presents the selected data in its true form. MUX153 can also be used to generate 2-stage AND-OR functions of three variables. The active-low enable input (EN) can be used as a select input when expanding to a larger multiplexor (8:1, 16:1, ... 64:1). The outputs of two or more MUX153s are ORed together for a large multiplexor.

$$Y = \overline{I0}.\overline{S0}.\overline{S1}.EN + I1.\overline{S0}.\overline{S1}.EN + \overline{I2}.S0.\overline{S1}.EN + I3.S0.\overline{S1}.EN$$

EN	S0	S1	I0	I1	I2	I3	Y
1	X	X	X	X	X	X	0
0	0	0	0	X	X	X	0
0	0	0	1	X	X	X	1
0	1	0	X	0	X	X	0
0	1	0	X	1	X	X	1
0	0	1	X	X	0	X	0
0	0	1	X	X	1	X	1
0	1	1	X	X	X	0	0
0	1	1	X	X	X	1	1
0	X	X	0	0	0	0	0
0	X	X	1	1	1	1	1
X	X	X	0	0	0	0	0
0	X	0	0	0	X	X	0
0	X	0	1	1	X	X	1
0	X	1	X	X	0	0	0
0	X	1	X	X	1	1	1
0	0	X	0	X	0	X	0
0	0	X	1	X	1	X	1
0	1	X	X	0	X	0	0
0	1	X	X	1	X	1	1

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC



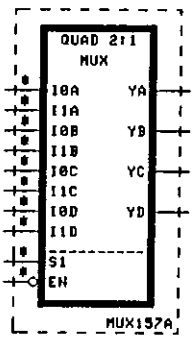
QUAD 4:1 MUXs

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

MUX157A 5 B cells QUAD 2:1 MUX WITH ENABLE LOW

		S	
Tpd I0i->Yi	++	1.34	ns
	--	1.61	ns
I1i->Yi	++	1.32	ns
	--	1.62	ns
S1->Yi	++	2.52	ns
	+-	2.69	ns
	-+	2.71	ns
	--	2.54	ns
EN->Yi	+-	1.49	ns
	-+	1.77	ns
i = A,B,C,D			
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

* EN, I0i, I1i, S1 COUNT AS 2 LOADS (i = A,B,C,D)



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

MUX157A 5 B cells QUAD 2:1 MUX WITH ENABLE LOW

The MUX157A is composed of 4 2:1 MUXs, each of which selects one data input from two sources (I0i,Ili). The select input (SI) and the enable input (EN) are common to all the multiplexors. The outputs (Yi) present the selected data in true form. MUX157 can also generate 2-stage AND-OR functions of two variables. The active LOW enable can be used as a select input when expanding to a quad of larger multiplexors (four 4:1, four 8:1, etc.). The corresponding outputs of two or more MUX153s are ORed together for a large multiplexor.

i = A, B, C, D

EN	Sl	I0i	Ili	Yi
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1
0	X	1	1	1
0	X	0	0	0

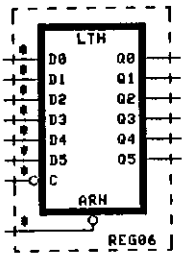
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

REG06 6 B cells HEX (6 bit) D-LATCH WITH ASYNC. RESET

		S	
Tpd C->Qi	-+	2.15	ns
	--	2.00	ns
D->Qi	++	1.25	ns
	--	1.22	ns
ARN->Qi	--	1.14	ns
	++	1.03	ns
	i= 0,1,2,3,4,5		
Tsu (D)		0.50	ns
Thd (D)		1.00	ns
Trec(ARN)		1.30	ns
PW (C)		1.95	ns
PW (ARN)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU
MAXIMUM FREQUENCY		165	MHz CON5
OF OPERATION		146	MHz CON4
(fMAX)		130	MHz MIL

---

* ARN COUNTS AS 6 LOADS
* Di, C COUNTS AS 2 LOADS EACH
See also REG373, an 8-bit latch w/o reset



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

REG06 6 B cells HEX (6 bit) D-LATCH WITH ASYNC. RESET

REG06 consists of six D-type latches with a common clock. When the clock input (C) is HIGH, the latches are all transparent to the data inputs (Di). When the clock is LOW, the data inputs that meet the set-up time requirement are latched. The output (Qi) is available in true form only.

i = 0,1,2,3,4,5

ARN	Di	C	Qin+1
0	X	X	0
1	1	0	1
1	0	0	0
1	X	1	Qin

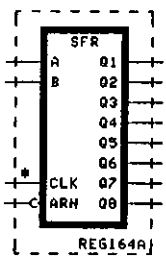
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

REG164A 16 B cells 8-BIT SR/PR SHFT RGSTR W/RESET

	S	
Tpd CLK->Qi ++	3.29	ns
+-	3.50	ns
ARN->Qi --	3.73	ns
i= 1,2,3,4,5,6,7,8		
Tsu (A,B)	1.50	ns
Thd (A,B)	0.00	ns
Trec(ARN)	1.20	ns
PW (ARN)	2.50	ns
PW (CLK)	2.50	ns
FAN-OUT LOAD LIMIT:	30	loads
k-FACTOR RISING	0.025	ns/LU
FALLING	0.025	ns/LU
MAXIMUM FREQUENCY	83	MHz COM5
OF OPERATION	73	MHz COM4
(fMAX)	66	MHz MIL

---

* CLK COUNTS AS 2 LOADS



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

REG164A 16 B cells 8-BIT SR/PR SHFT RGSTR W/RESET

REG164A is an 8-bit serial-in, parallel-out shift register. Serial data input (A,B) are synchronously entered through a 2-input AND gate on the rising edge of the clock input (CLK). The active-LOW reset input (ARN) clears this shift register asynchronously and sets all outputs (Q1-Q8) LOW independent of the clock.

ARN	CLK	A	B	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	
0	X	X	X	0	0	0	0	0	0	0	0	RESET
1	0	X	X	Q1n	Q2n	Q3n	Q4n	Q5n	Q6n	Q7n	Q8n	HOLD
1	R	1	1	1	Q1n	Q2n	Q3n	Q4n	Q5n	Q6n	Q7n	SHIFT IN1
1	R	X	0	0	Q1n	Q2n	Q3n	Q4n	Q5n	Q6n	Q7n	SHIFT IN0
1	R	0	X	0	Q1n	Q2n	Q3n	Q4n	Q5n	Q6n	Q7n	SHIFT IN0

Qin = last steady state value

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

REG175A 10 B cells 4-BIT REGISTER WITH ASYNC. RESET

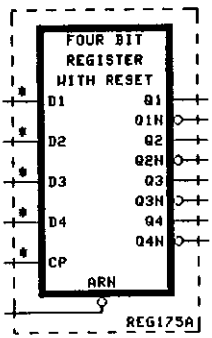
		S	
Tpd CP->Qi	++	2.80	ns
	+-	2.17	ns
CP->QiN	++	3.19	ns
	+-	3.67	ns
ARN->Qi	--	3.90	ns
ARN->QiN	-+	4.48	ns

i=1,2,3,4

Tsu (Di)	1.20	ns
Thd (Di)	0.30	ns
Trec (ARN)	0.50	ns
PW (ARN)	1.95	ns
PW (CP)	1.95	ns
FAN-OUT LOAD LIMIT:	30	loads
k-FACTOR RISING	0.025	ns/LU
FALLING	0.025	ns/LU
MAXIMUM FREQUENCY	165	MHz COM5
OF OPERATION	146	MHz COM4
(fMAX)	130	MHz MIL

---

* CP, D1, D2, D3, D4 COUNT AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

REG175A 10 B cells 4-BIT REGISTER WITH ASYNC. RESET

REG175A contains four flip/flops with a single data input each (Di). The clock input (CP) and reset input (ARN) are shared by all four flip/flops on the REG175A. Both true and complemented outputs are provided for each flip/flop (Qi, QiN).

CP	Di	ARN	Qin+1	QiNn+1
X	X	0	0	1
R	0	1	0	1
R	1	1	1	0
0	X	1	Qin	QiNn

i = 1,2,3,4

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

REG373A 8 B cells OCTAL D-LATCH TRANSPARENT HIGH

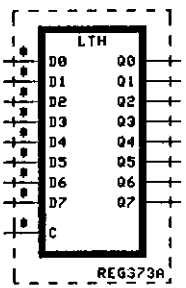
		S	
Tpd Di->Qi	++	0.86	ns
	--	1.14	ns
C->Qi	++	1.84	ns
	+-	2.37	ns
Tsu (Di)		0.70	ns
Th (Di)		0.80	ns
PW (C)		1.95	ns

i=0,1,2,3,4,5,6,7

FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING Q0->Q7	0.025	ns/LU
	FALLING	0.025	ns/LU
MAXIMUM FREQUENCY		165	MHz COM5
OF OPERATION		146	MHz COM4
(fMAX)		130	MHz MIL

---

* C COUNTS AS 2 LOADS
* Di COUNTS AS 2 LOADS (i = 0...7)



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

REG373A 8 B cells OCTAL D-LATCH TRANSPARENT HIGH

REG373A consists of eight D-type latches with a common clock. When the clock input (C) is HIGH, the latches are all transparent to the data inputs (Di). When the clock is LOW, the data inputs that meet the set-up time requirement are latched. The output (Qi) is available in true form only.

C	Qi
0	LATCHED
1	TRANSPARENT (Di)

i = 0,1,2,3,4,5,6,7

Section 6-6:

Special

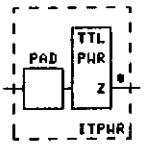
ADDED POWER AND GROUNDS

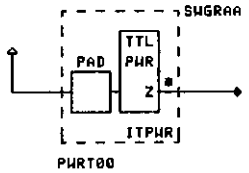
ITPWR I/O CELL ADDED V_{CC} (+5V) PAD

REQUIRED WHEN AN ADDED TTL POWER PAD IS NEEDED.
USES THE PAD PORTION OF THE I/O CELL.
USED TO OBTAIN A CORRECT POPULATION REPORT AND EXTERNAL PIN (PAD) COUNT BY THE AMCC MACROMATRIX ERC SOFTWARE.

- GROUND THE INPUT PIN WITH THE WIRE POINTING UP
- TERMINATE THE OUTPUT

NOTE: When placing an ITPWR macro, the macro must be interspersed with the simultaneously switching outputs it supports. On the Q14000B array and any other array with packages that contain internal power-ground planes, an ITPWR must be placed on a PAD that will allow it to be connected to the internal plane if it is at all possible. Placing it on a pad that must connect to a package pin requires a custom DUT board for test.





NAME USING THE CONVENTIONS,
IDENTIFY SWGROUP WITH THE SWGROUP
PARAMETER OR PROPERTY
AS REQUIRED

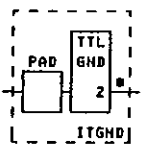
ADDED POWER AND GROUNDS

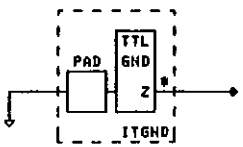
ITGND I/O CELL ADDED TTL GND PAD

REQUIRED WHEN AN ADDED TTL GROUND PAD IS NEEDED.
USES THE PAD PORTION OF THE I/O CELL.
USED TO OBTAIN A CORRECT POPULATION REPORT AND EXTERNAL PIN (PAD) COUNT BY THE AMCC MACROMATRIX ERC SOFTWARE.

- GROUND THE INPUT PIN WITH THE WIRE POINTING DOWN
- TERMINATE THE OUTPUT

NOTE: When placing an ITGND macro, the macro must be interspersed with the simultaneously switching outputs it supports. On the Q14000B array and any other array with packages that contain internal power-ground planes, an ITGND must be placed on a PAD that will allow it to be connected to the internal plane if it is at all possible. Placing it on a pad that must connect to a package pin requires a custom DUT board for test.





GNDT00

NAME USING THE CONVENTIONS,
IDENTIFY SWGROUP WITH THE SWGROUP
PARAMETER OR PROPERTY
AS REQUIRED

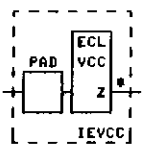
ADDED POWER AND GROUNDS

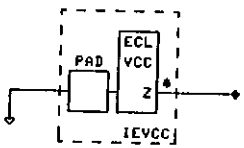
IEVCC I/O CELL ADDED ECL VCC PAD

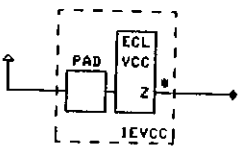
REQUIRED WHEN AN ADDED ECL VCC PAD IS NEEDED.
USES THE PAD PORTION OF THE I/O CELL.
USED TO OBTAIN A CORRECT POPULATION REPORT AND EXTERNAL PIN (PAD) COUNT BY THE AMCC MACROMATRIX ERC SOFTWARE.

- GROUND THE INPUT PIN WITH THE WIRE POINTING DOWN FOR STANDARD-REFERENCE ECL; POINTING UP FOR +5V REF ECL.
- TERMINATE THE OUTPUT
- IEVCC is a GROUND pad in a STD-REF ECL circuit.
- IEVCC is a POWER pad in a +5V REF ECL circuit.

NOTE: When placing an IEVCC macro, the macro must be interspersed with the simultaneously switching outputs it supports. On the Q14000B array and any other array with packages that contain internal power-ground planes, an IEVCC must be placed on a PAD that will allow it to be connected to the internal plane if it is at all possible. Placing it on a pad that must connect to a package pin requires a custom DUT board for test.







NAME USING THE CONVENTIONS,
IDENTIFY SWGROUP WITH THE SWGROUP
PARAMETER OR PROPERTY
AS REQUIRED

CHIP MACROS

CHIP MACROS:

The chip macro documents the number of fixed power and ground pins that a particular array has for a given I/O mode. It also documents the internal pin count limit, the number of each type of cell available on a given array, the allowed cell utilization, the default power supply or supplies, the worst-case current multiplier for MIL and for COM product grades and other data as required by the AMCC MacroMatrix software. Note that the POWER_SUPPLY and PRODUCT_GRADE parameters control the multipliers used in the Front-Annotation FNTCOM.ews file.

- MUST BE USED - THE MACROMATRIX ERC SOFTWARE REQUIRES THAT A CHIP MACRO BE USED ON THE SCHEMATICS

- Follow directions in the MACROMATRIX USER'S GUIDE (Volume II, Section 8) and MACROMATRIX INSTALLATION MANUAL (Volume II, Section 7) to attach parameters or values to the chip macros as required - the procedure is EWS-specific.

- Ground and terminate inputs and outputs as shown in the examples. The inputs to a chip macro are always tied to global_ground regardless of the individual chip technology (BiCMOS, Bipolar).

- Chip macros are named (CHIP00) but are not listed in the placement file, use no cells and draw no current. They are informational units only.

- Page 1 of the schematics should contain the chip macros and the added power and ground macros.

CHIP MACROS

Chip Macro Parameters that are legal for the Q14000 Series:

		TTL	100% ECL	MIX	+5MIX
PRODUCT_NAME	AMCC ASSIGNED NAME	X	X	X	X
DEVICE_NUMBER	AMCC ASSIGNED NUMBER	X	X	X	X
PRODUCT_GRADE	MIL OR COM	X	X	X	X
POWER_SUPPLY	FOR OTHER THAN DEFAULT	-	X	X	-

The first three parameters are REQUIRED for design submission - the ERCs will use default values and continue but the resulting report (AMCCERC.LST) cannot be submitted.

Allowed POWER_SUPPLY parameter values for the Q14000 Series:

default	What appears on the chip macro graphic
STD4	-4.5V ECL VEE SUPPLY; ECL VCC = 0V
STD5	-5.2V ECL VEE SUPPLY; ECL VCC = 0V
5VREF	+5V ECL VCC SUPPLY; ECL VEE = 0V

Note: The Q14000B and Q6000B arrays are not part of the (812) macro release. Information on these arrays is PRELIMINARY.

CHIP MACROS

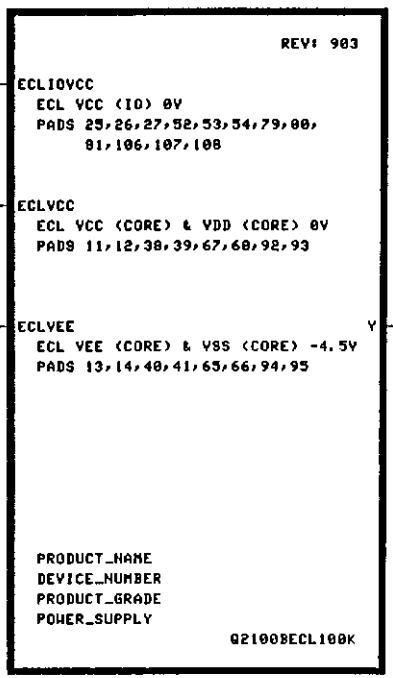
FOR SINGLE POWER SUPPLY +5V CIRCUITS; 100% TTL:

Q14000BTTL	FOR 100% TTL CIRCUIT ON A Q14000B
Q9100BTTL	FOR 100% TTL CIRCUIT ON A Q9100B
Q6000BTTL	FOR 100% TTL CIRCUIT ON A Q6000B
Q2100BTTL	FOR 100% TTL CIRCUIT ON A Q2100B

FOR SINGLE POWER SUPPLY CIRCUITS; 100% ECL:

Q14000BECL10K	FOR 100% ECL 10K CIRCUIT ON A Q14000B
Q9100BECL10K	FOR 100% ECL 10K CIRCUIT ON A Q9100B
Q6000BECL10K	FOR 100% ECL 10K CIRCUIT ON A Q6000B
Q2100BECL10K	FOR 100% ECL 10K CIRCUIT ON A Q2100B
Q14000BECL100K	FOR 100% ECL 100K CIRCUIT ON A Q14000B
Q9100BECL100K	FOR 100% ECL 100K CIRCUIT ON A Q9100B
Q6000BECL100K	FOR 100% ECL 100K CIRCUIT ON A Q6000B
Q2100BECL100K	FOR 100% ECL 100K CIRCUIT ON A Q2100B

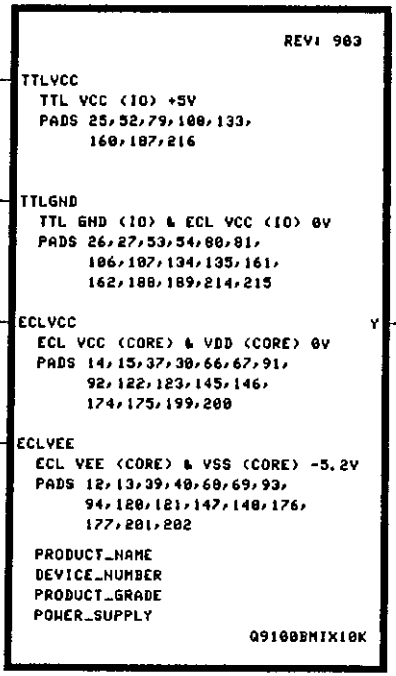
SUPPLY = -5.2V, -4.5V, or +5V



CHIP MACROS

FOR DUAL POWER SUPPLY CIRCUITS; ECL/TTL MIX:

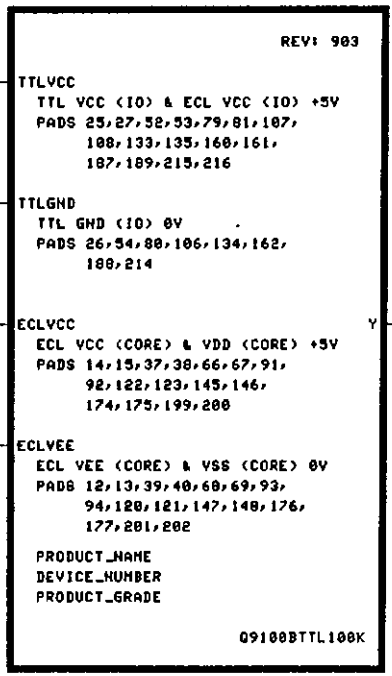
Q14000BMIX10K	FOR ECL 10K/TTL CIRCUIT ON A Q14000B
Q9100BMIX10K	FOR ECL 10K/TTL CIRCUIT ON A Q9100B
Q6000BMIX10K	FOR ECL 10K/TTL CIRCUIT ON A Q6000B
Q2100BMIX10K	FOR ECL 10K/TTL CIRCUIT ON A Q2100B
Q14000BMIX100K	FOR ECL 100K/TTL CIRCUIT ON A Q14000B
Q9100BMIX100K	FOR ECL 100K/TTL CIRCUIT ON A Q9100B
Q6000BMIX100K	FOR ECL 100K/TTL CIRCUIT ON A Q6000B
Q2100BMIX100K	FOR ECL 100K/TTL CIRCUIT ON A Q2100B



CHIP MACROS

FOR SINGLE POWER SUPPLY +5V CIRCUITS; ECL/TTL MIX:

Q14000BTTL10K	FOR +5V REF ECL 10K/TTL CIRCUIT ON A Q14000B
Q9100BTTL10K	FOR +5V REF ECL 10K/TTL CIRCUIT ON A Q9100B
Q6000BTTL10K	FOR +5V REF ECL 10K/TTL CIRCUIT ON A Q6000B
Q2100BTTL10K	FOR +5V REF ECL 10K/TTL CIRCUIT ON A Q2100B
Q14000BTTL100K	FOR +5V REF ECL 100K/TTL CIRCUIT ON A Q14000B
Q9100BTTL100K	FOR +5V REF ECL 100K/TTL CIRCUIT ON A Q9100B
Q6000BTTL100K	FOR +5V REF ECL 100K/TTL CIRCUIT ON A Q6000B
Q2100BTTL100K	FOR +5V REF ECL 100K/TTL CIRCUIT ON A Q2100B

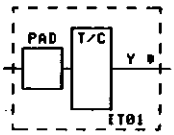


Section 7:

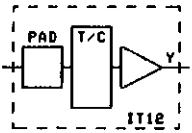
Quicksheets

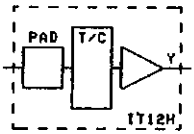
Q14000 BiCMOS
(903)

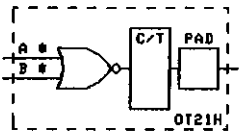
TTL

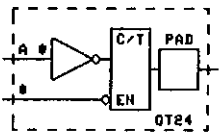


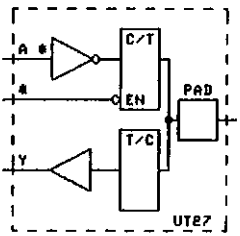
TTL I/O FOR +5V SYSTEMS

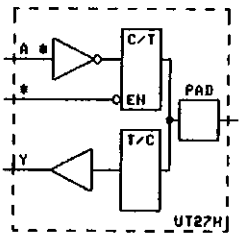






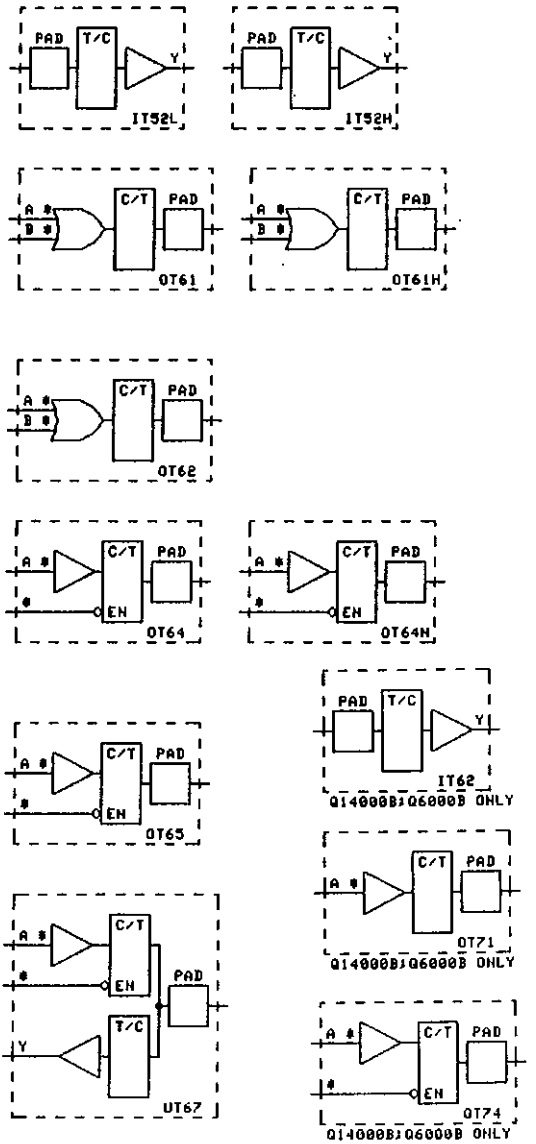




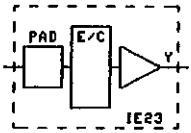


TTL MIX

TTLMIX FOR DUAL-SUPPLY SYSTEMS



ECL



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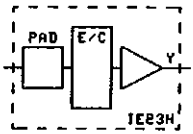

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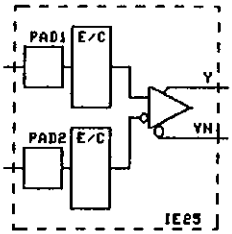

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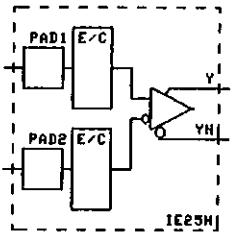

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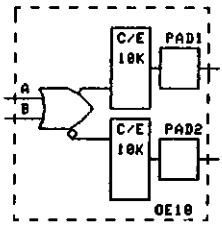

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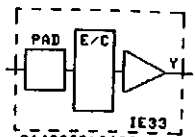
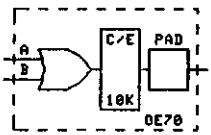


Q14000B:Q6000B ONLY



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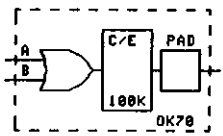
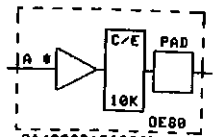
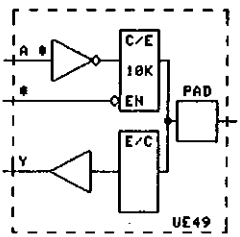


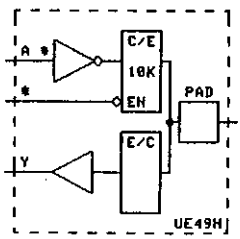
ECL 100K



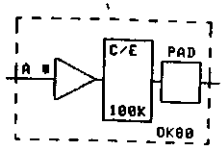
Q14000B:Q6000B ONLY



ECL 10K

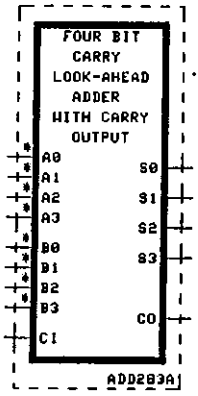


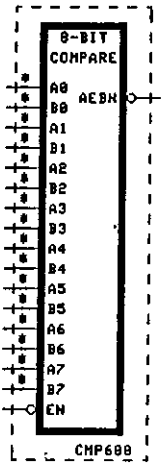
ECL 10K

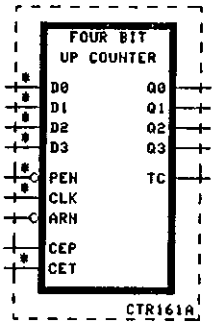


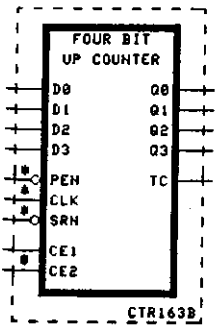
Q14000B:Q6000B ONLY

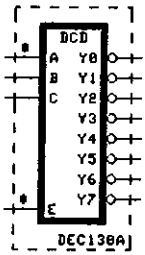
CORE MACROS

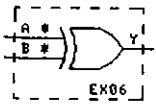

FOUR BIT
CARRY
LOOK-AHEAD
ADDER
WITH CARRY
OUTPUT
A0
A1
A2
A3
B0
B1
B2
B3
CI
S0
S1
S2
S3
CO
ADD283A

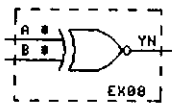

8-BIT
COMPARE
A0
B0
A1
B1
A2
B2
A3
B3
A4
B4
A5
B5
A6
B6
A7
B7
EN
AEBH
CMP688


FOUR BIT
UP COUNTER
D0
D1
D2
D3
PEN
CLK
ARN
CEP
CET
Q0
Q1
Q2
Q3
TC
CTR161A

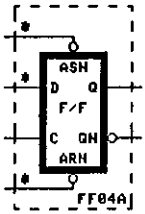

FOUR BIT
UP COUNTER
D0
D1
D2
D3
PEN
CLK
SRN
CE1
CE2
Q0
Q1
Q2
Q3
TC
CTR163B

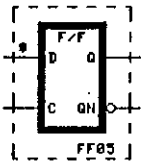

DCD
A
B
C
E
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
DEC138A

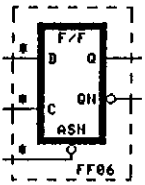

A
B
Y
EX06

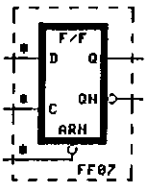

A
B
YN
EX08

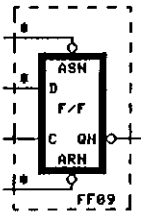
CORE MACROS

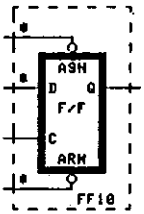

ASN
D Q
F/F
C QN
ARN
FF04A

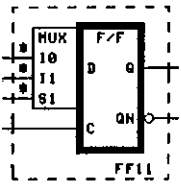

F/F
D Q
C QN
FF05

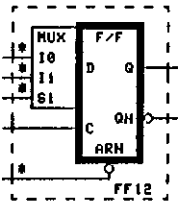

F/F
D Q
C QN
ASH
FF06


F/F
D Q
C QN
ARH
FF07


ASN
D
F/F
C QN
ARN
FF09


ASN
D Q
F/F
C
ARN
FF10


MUX
I0
I1
S1
F/F
D Q
C QN
FF11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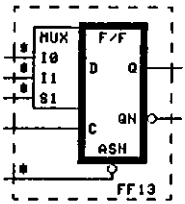
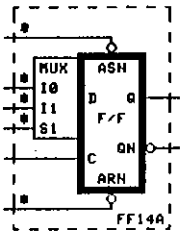
I0
I1
S1
F/F
D Q
C QN
ARN
FF12


MUX
I0
I1
S1
F/F
D Q
C QN
ASH
FF13


MUX
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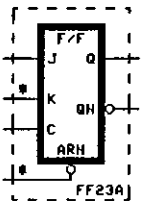
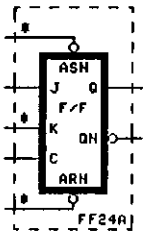
I1
S1
ASN
D Q
F/F
C QN
ARN
FF14A


F/F
J Q
K QN
C
ARN
FF23A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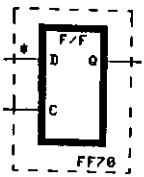
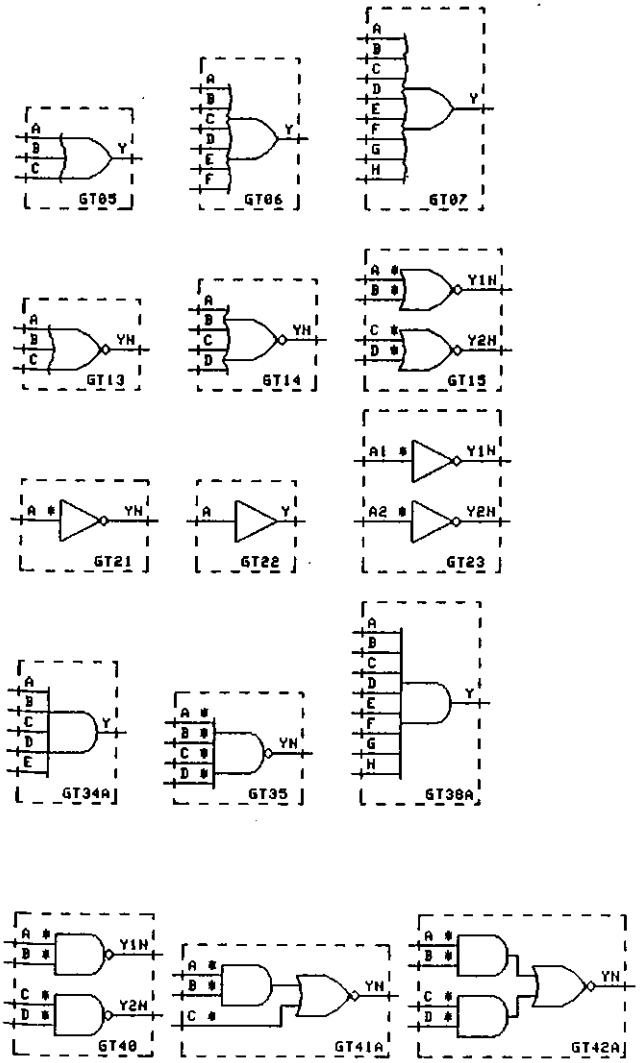
J Q
F/F
K QN
C
ARN
FF24A


F/F
D Q
C
FF70

CORE MACROS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B
C
Y
GT05
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B
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D
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Y
GT06
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D
E
F
G
H
Y
GT07
A
B
C
YN
GT13
A
B
C
D
YN
GT14
A #
B #
C #
D #
Y1N
Y2N
GT15
A #
YN
GT21
A
Y
GT22
A1 #
A2 #
Y1N
Y2N
GT23
A
B
C
D
E
F
Y
GT34A
A #
B #
C #
D #
YN
GT35
A
B
C
D
E
F
G
H
Y
GT38A
A #
B #
C #
D #
Y1N
Y2N
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B #
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YN
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A #
B #
C #
D #
YN
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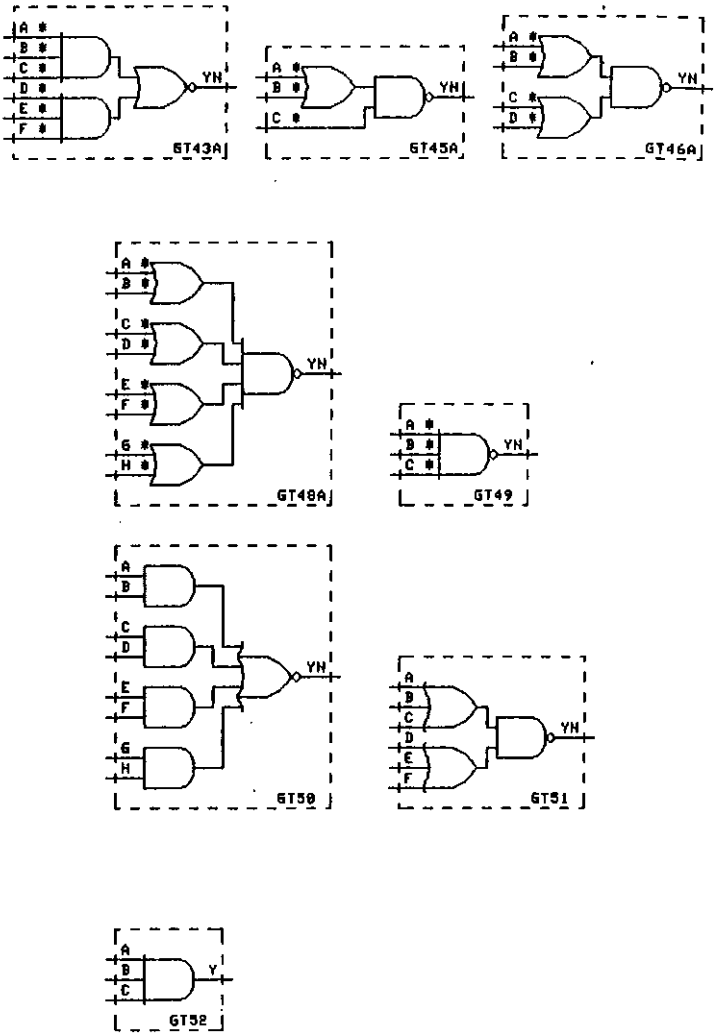
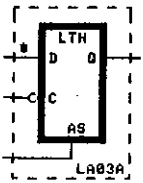
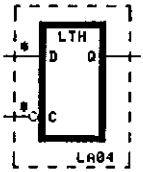
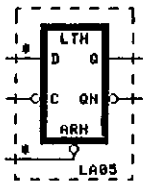
CORE MACROS

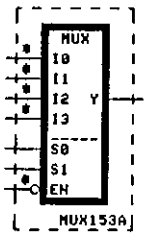


CORE MACROS


LTH
D
Q
C
AS
LA03A


LTH
D
Q
C
LA04


LTH
D
Q
C
QN
ARN
LA05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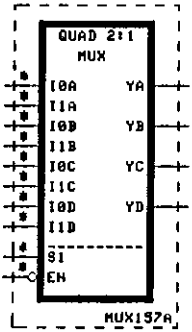
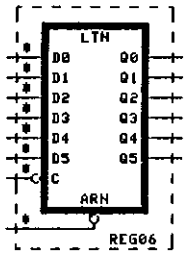
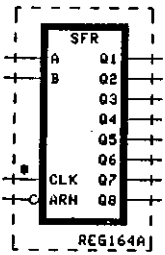
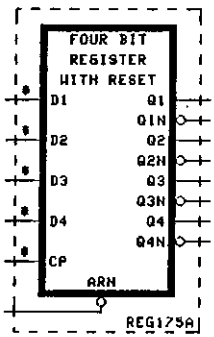
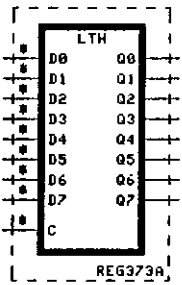
I2
I3
Y
S0
S1
EN
MUX153A

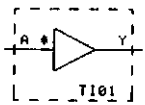

QUAD 2:1
MUX
I0A
I1A
I0B
I1B
I0C
I1C
I0D
I1D
YA
YB
YC
YD
SI
EN
MUX157A

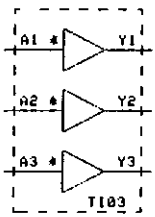

LTH
D0
D1
D2
D3
D4
D5
C
Q0
Q1
Q2
Q3
Q4
Q5
ARN
REG06


SFR
A
B
CLK
ARN
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
REG164A

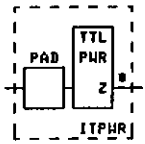

FOUR BIT
REGISTER
WITH RESET
D1
D2
D3
D4
CP
Q1
Q1N
Q2
Q2N
Q3
Q3N
Q4
Q4N
ARN
REG175A

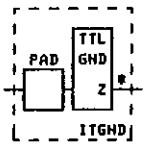

LTH
D0
D1
D2
D3
D4
D5
D6
D7
C
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
REG373A

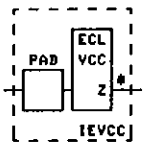

A
Y
TI01


A1
A2
A3
Y1
Y2
Y3
TI03

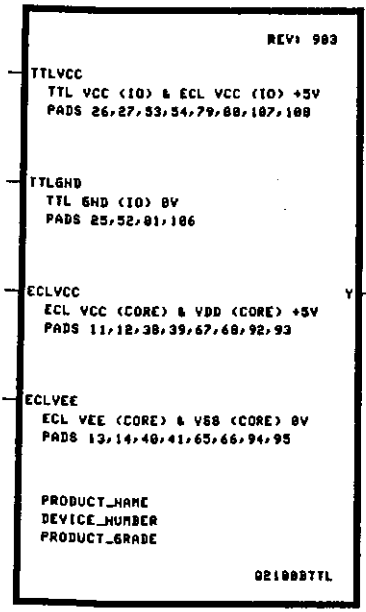
EXTRA POWER & GROUND

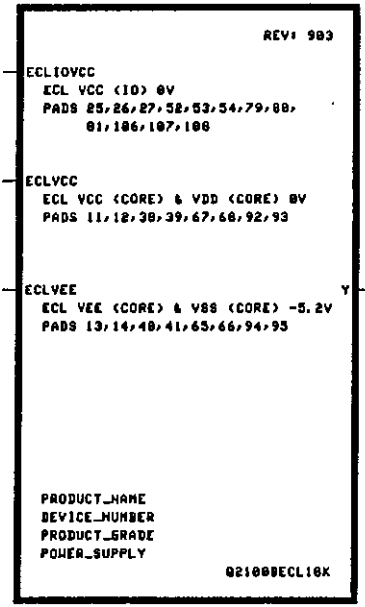


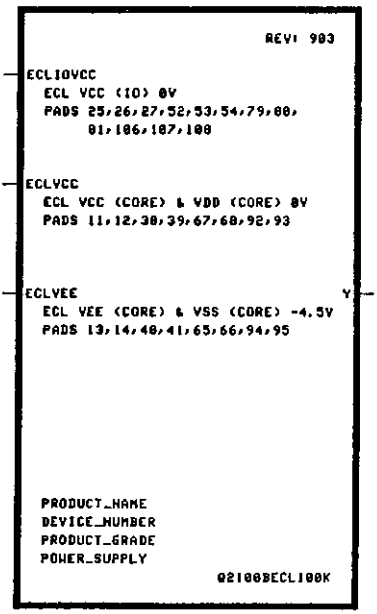




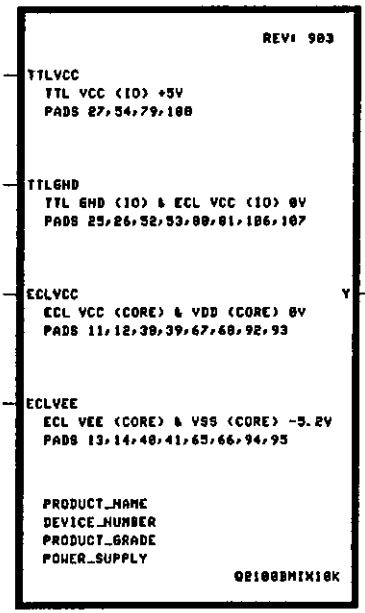
CHIP MACROS

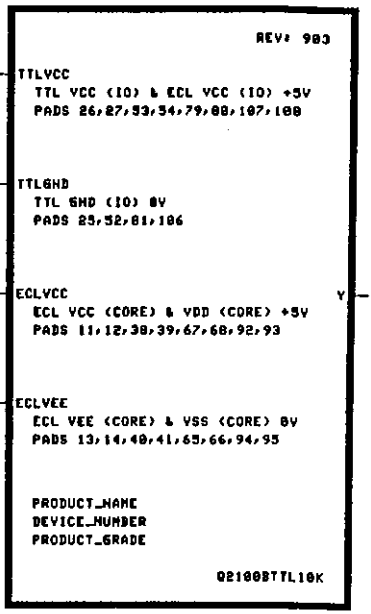

REV: 903
TTLVCC
TTL VCC (IO) & ECL VCC (IO) +5V
PADS 26,27,53,54,79,80,107,108
TTLGND
TTL GND (IO) 0V
PADS 25,52,81,106
ECLVCC
ECL VCC (CORE) & VDD (CORE) +5V
PADS 11,12,38,39,67,68,92,93
Y
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 13,14,40,41,65,66,94,95
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
Q2100BTTL

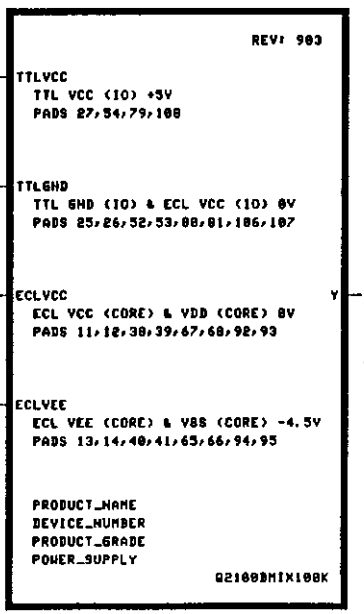

REV: 903
ECLIOVCC
ECL VCC (IO) 0V
PADS 25,26,27,52,53,54,79,80,
81,106,107,108
ECLVCC
ECL VCC (CORE) & VDD (CORE) 0V
PADS 11,12,38,39,67,68,92,93
ECLVEE
ECL VEE (CORE) & VSS (CORE) -5.2V
PADS 13,14,40,41,65,66,94,95
Y
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q2100BECL10K

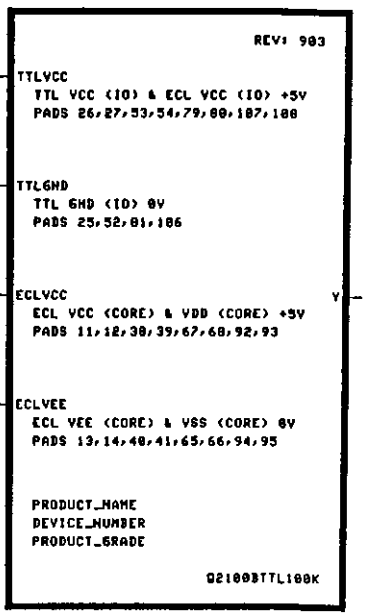

REV: 903
ECLIOVCC
ECL VCC (IO) 0V
PADS 25,26,27,52,53,54,79,80,
81,106,107,108
ECLVCC
ECL VCC (CORE) & VDD (CORE) 0V
PADS 11,12,38,39,67,68,92,93
ECLVEE
ECL VEE (CORE) & VSS (CORE) -4.5V
PADS 13,14,40,41,65,66,94,95
Y
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q2100BECL100K

CHIP MACROS

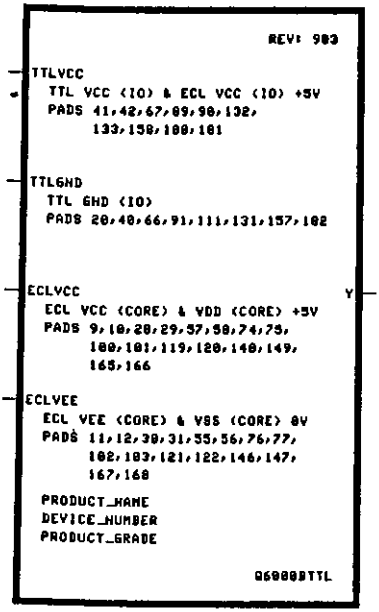

REV: 903
TTLVCC
TTL VCC (IO) +5V
PADS 27,54,79,100
TTLGND
TTL GND (IO) & ECL VCC (IO) 0V
PADS 25,26,52,53,80,81,106,107
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) 0V
PADS 11,12,38,39,67,68,92,93
ECLVEE
ECL VEE (CORE) & VSS (CORE) -5.2V
PADS 13,14,40,41,65,66,94,95
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q2100BMIX10K

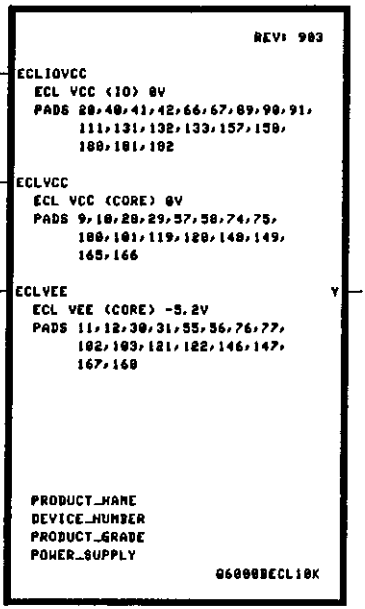

REV: 903
TTLVCC
TTL VCC (IO) & ECL VCC (IO) +5V
PADS 26,27,53,54,79,80,107,100
TTLGND
TTL GND (IO) 0V
PADS 25,52,81,106
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) +5V
PADS 11,12,38,39,67,68,92,93
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 13,14,40,41,65,66,94,95
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
Q2100BTTL10K


REV: 903
TTLVCC
TTL VCC (IO) +5V
PADS 27,54,79,100
TTLGND
TTL GND (IO) & ECL VCC (IO) 0V
PADS 25,26,52,53,80,81,106,107
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) 0V
PADS 11,12,38,39,67,68,92,93
ECLVEE
ECL VEE (CORE) & VSS (CORE) -4.5V
PADS 13,14,40,41,65,66,94,95
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q2100BMIX100K


REV: 903
TTLVCC
TTL VCC (IO) & ECL VCC (IO) +5V
PADS 26,27,53,54,79,80,107,100
TTLGND
TTL GND (IO) 0V
PADS 25,52,81,106
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) +5V
PADS 11,12,38,39,67,68,92,93
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 13,14,40,41,65,66,94,95
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
Q2100BTTL100K

CHIP MACROS


REV: 903
TTLVCC
TTL VCC (IO) & ECL VCC (IO) +5V
PADS 41,42,67,89,90,132,
133,158,180,181
TTLGND
TTL GND (IO)
PADS 20,40,66,91,111,131,157,182
ECLVCC
ECL VCC (CORE) & VDD (CORE) +5V
PADS 9,10,28,29,57,58,74,75,
180,181,119,120,148,149,
165,166
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 11,12,30,31,55,56,76,77,
182,183,121,122,146,147,
167,168
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
Q6000BTTL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ECL VCC (IO) 0V
PADS 20,40,41,42,66,67,89,90,91,
111,131,132,133,157,158,
180,181,182
ECLVCC
ECL VCC (CORE) 0V
PADS 9,10,28,29,57,58,74,75,
180,181,119,120,148,149,
165,166
ECLVEE
ECL VEE (CORE) -5.2V
PADS 11,12,30,31,55,56,76,77,
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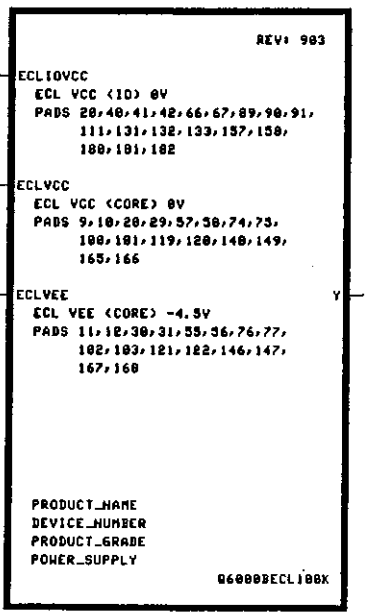
167,168
Y
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q6000BECL10K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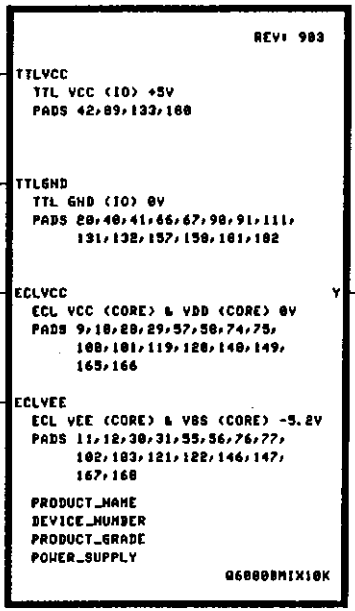
ECL VCC (IO) 0V
PADS 20,40,41,42,66,67,89,90,91,
111,131,132,133,157,158,
180,181,182
ECLVCC
ECL VCC (CORE) 0V
PADS 9,10,28,29,57,58,74,75,
180,181,119,120,148,149,
165,166
ECLVEE
ECL VEE (CORE) -4.5V
PADS 11,12,30,31,55,56,76,77,
182,183,121,122,146,147,
167,168
Y
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q6000BECL100K

CHIP MACROS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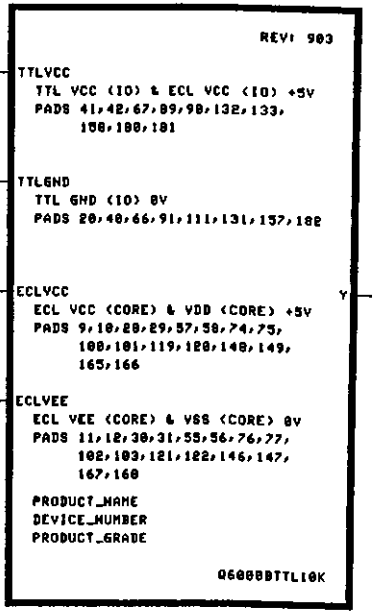
TTL VCC (IO) +5V
PADS 42,89,133,180
TTLGND
TTL GND (IO) 0V
PADS 20,40,41,66,67,90,91,111,
131,132,157,158,181,182
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) 0V
PADS 9,10,28,29,57,58,74,75,
100,101,119,120,140,149,
165,166
ECLVEE
ECL VEE (CORE) & VSS (CORE) -5.2V
PADS 11,12,30,31,55,56,76,77,
102,103,121,122,146,147,
167,168
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q6000BMIX10K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PADS 41,42,67,89,90,132,133,
158,180,181
TTLGND
TTL GND (IO) 0V
PADS 20,40,66,91,111,131,157,182
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) +5V
PADS 9,10,28,29,57,58,74,75,
100,101,119,120,140,149,
165,166
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 11,12,30,31,55,56,76,77,
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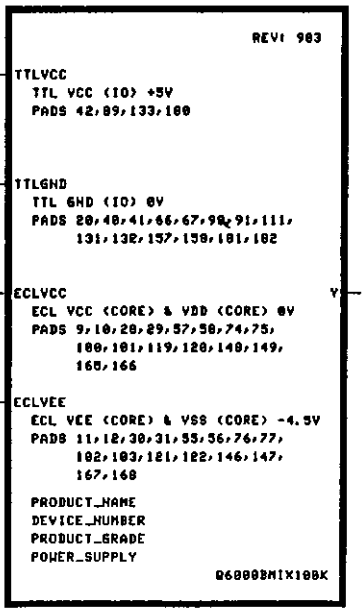
167,168
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
Q6000BTTL10K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TTL VCC (IO) +5V
PADS 42,89,133,180
TTLGND
TTL GND (IO) 0V
PADS 20,40,41,66,67,90,91,111,
131,132,157,158,181,182
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) 0V
PADS 9,10,28,29,57,58,74,75,
100,101,119,120,140,149,
165,166
ECLVEE
ECL VEE (CORE) & VSS (CORE) -4.5V
PADS 11,12,30,31,55,56,76,77,
102,103,121,122,146,147,
167,168
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
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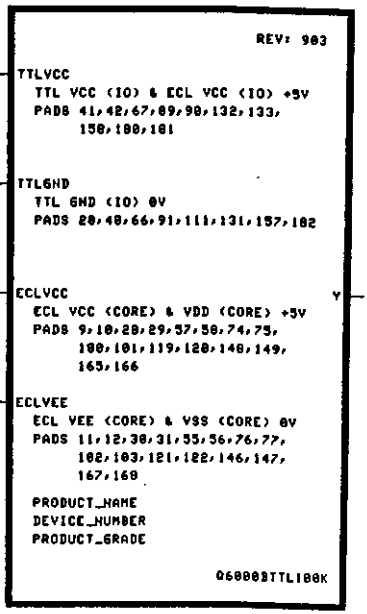
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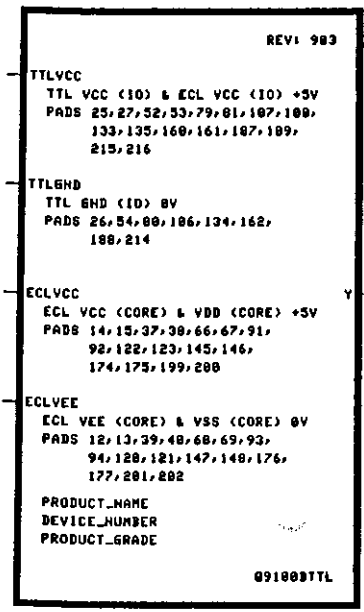
TTL VCC (IO) & ECL VCC (IO) +5V
PADS 41,42,67,89,90,132,133,
158,180,181
TTLGND
TTL GND (IO) 0V
PADS 20,40,66,91,111,131,157,182
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) +5V
PADS 9,10,28,29,57,58,74,75,
100,101,119,120,140,149,
165,166
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 11,12,30,31,55,56,76,77,
102,103,121,122,146,147,
167,168
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
Q6000BTTL100K

CHIP MACROS


REV: 903
TTLVCC
TTL VCC (IO) & ECL VCC (IO) +5V
PADS 25,27,52,53,79,81,107,108,
133,135,160,161,187,189,
215,216
TTLGND
TTL GND (IO) 0V
PADS 26,54,80,106,134,162,
188,214
ECLVCC
ECL VCC (CORE) & VDD (CORE) +5V
PADS 14,15,37,38,66,67,91,
92,122,123,145,146,
174,175,199,200
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 12,13,39,48,68,69,93,
94,120,121,147,148,176,
177,201,202
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
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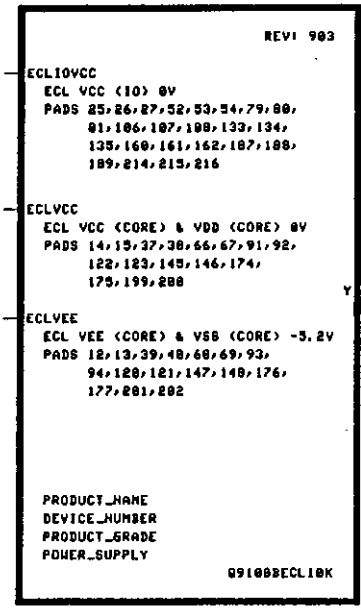
9100BTTL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81,106,107,108,133,134,
135,160,161,162,187,188,
189,214,215,216
ECLVCC
ECL VCC (CORE) & VDD (CORE) 0V
PADS 14,15,37,38,66,67,91,92,
122,123,145,146,174,
175,199,200
ECLVEE
ECL VEE (CORE) & VSS (CORE) -5.2V
PADS 12,13,39,48,68,69,93,
94,120,121,147,148,176,
177,201,202
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
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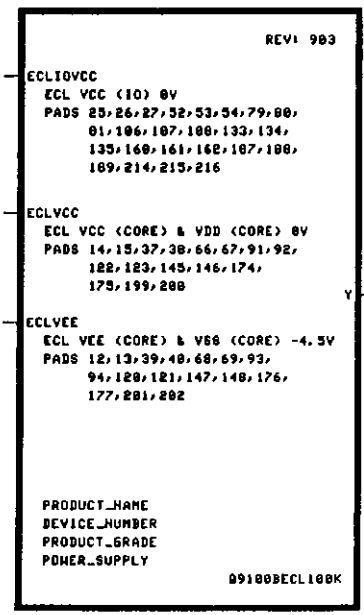
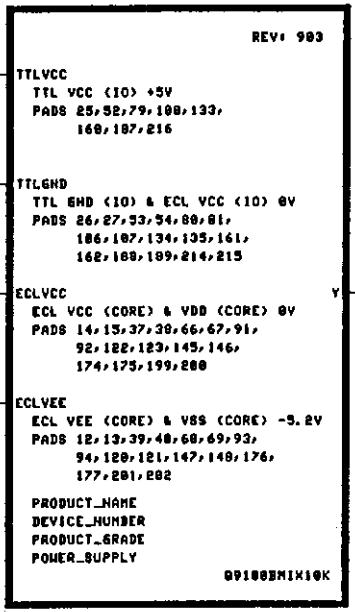
9100BECL10K


REV: 903
ECL10VCC
ECL VCC (IO) 0V
PADS 25,26,27,52,53,54,79,80,
81,106,107,108,133,134,
135,160,161,162,187,188,
189,214,215,216
ECLVCC
ECL VCC (CORE) & VDD (CORE) 0V
PADS 14,15,37,38,66,67,91,92,
122,123,145,146,174,
175,199,200
ECLVEE
ECL VEE (CORE) & VSS (CORE) -4.5V
PADS 12,13,39,48,68,69,93,
94,120,121,147,148,176,
177,201,202
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Y
9100BECL100K

CHIP MACROS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106,107,134,135,161,
162,188,189,214,215
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Y
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92,122,123,145,146,
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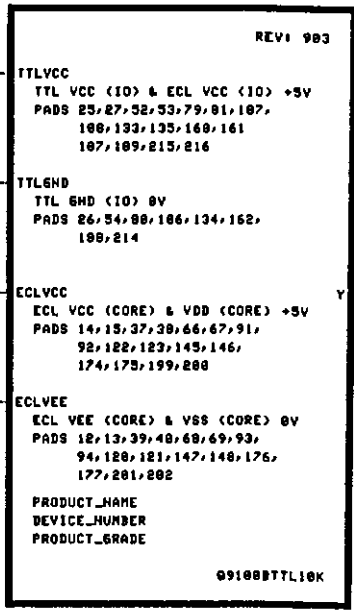
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q9100BMIX10K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188,214
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ECL VCC (CORE) & VDD (CORE) +5V
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ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
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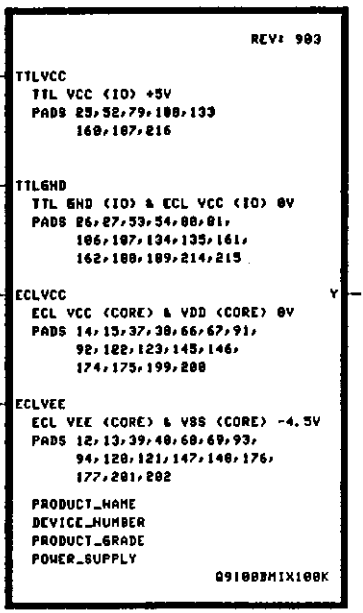
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106,107,134,135,161,
162,188,189,214,215
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) 0V
PADS 14,15,37,38,66,67,91,
92,122,123,145,146,
174,175,199,200
ECLVEE
ECL VEE (CORE) & VSS (CORE) -4.5V
PADS 12,13,39,40,68,69,93,
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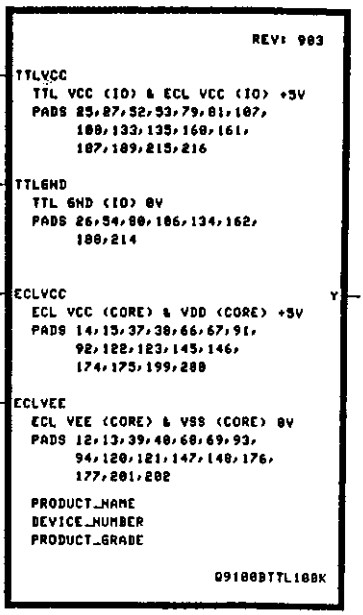
POWER_SUPPLY
Q9100BMIX100K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107,189,215,216
TTLGND
TTL GND (IO) 0V
PADS 26,54,80,106,134,162,
188,214
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) +5V
PADS 14,15,37,38,66,67,91,
92,122,123,145,146,
174,175,199,200
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 12,13,39,40,68,69,93,
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177,201,202
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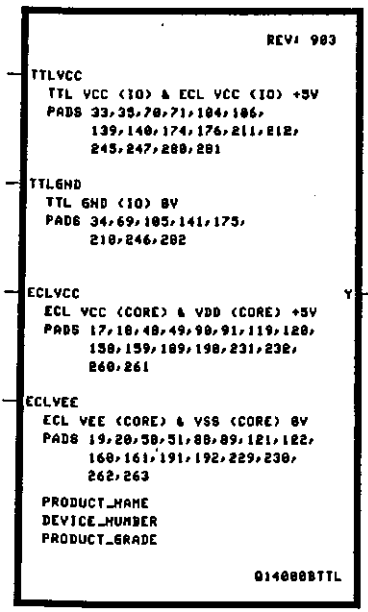
DEVICE_NUMBER
PRODUCT_GRADE
Q9100BTTL100K

CHIP MACROS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PADS 34,69,105,141,175,
210,246,282
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) +5V
PADS 17,18,48,49,90,91,119,120,
150,159,189,190,231,232,
260,261
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 19,20,50,51,88,89,121,122,
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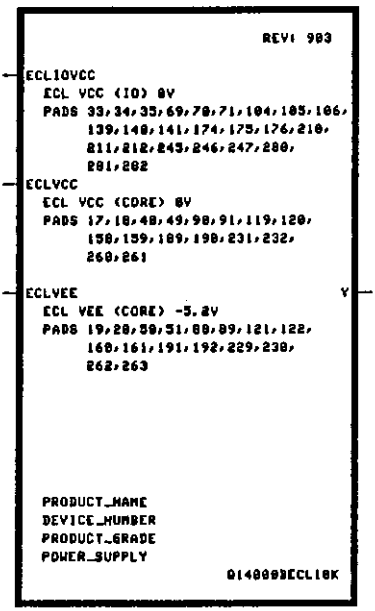
PRODUCT_GRADE
Q14000BTTL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281,282
ECLVCC
ECL VCC (CORE) 0V
PADS 17,18,48,49,90,91,119,120,
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260,261
ECLVEE
Y
ECL VEE (CORE) -5.2V
PADS 19,20,50,51,88,89,121,122,
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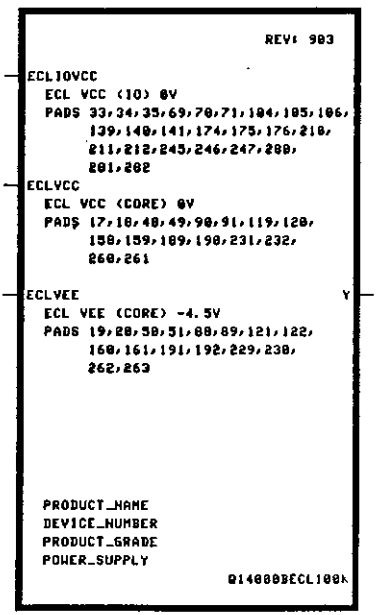
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ECL VCC (IO) 0V
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211,212,245,246,247,280,
281,282
ECLVCC
ECL VCC (CORE) 0V
PADS 17,18,48,49,90,91,119,120,
150,159,189,190,231,232,
260,261
ECLVEE
Y
ECL VEE (CORE) -4.5V
PADS 19,20,50,51,88,89,121,122,
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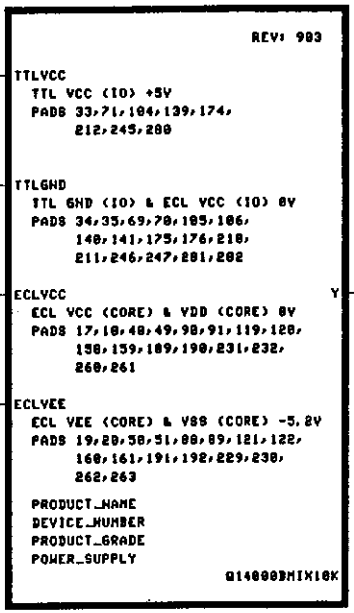
262,263
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q14000BECL100K

CHIP MACROS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TTL VCC (IO) +5V
PADS 33,71,104,139,174,
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TTLGND
TTL GND (IO) & ECL VCC (IO) 0V
PADS 34,35,69,70,105,106,
140,141,175,176,210,
211,246,247,281,282
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) 0V
PADS 17,18,48,49,90,91,119,120,
150,159,189,190,231,232,
260,261
ECLVEE
ECL VEE (CORE) & VSS (CORE) -5.2V
PADS 19,20,50,51,88,89,121,122,
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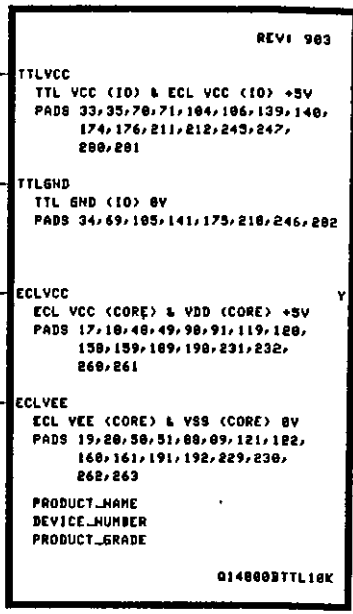
262,263
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q14000BMIX10K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TTL GND (IO) 0V
PADS 34,69,105,141,175,210,246,282
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) +5V
PADS 17,18,48,49,90,91,119,120,
150,159,189,190,231,232,
260,261
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 19,20,50,51,88,89,121,122,
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262,263
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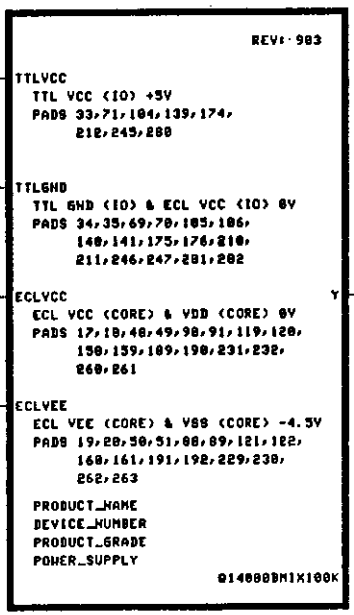
Q14000BTTL10K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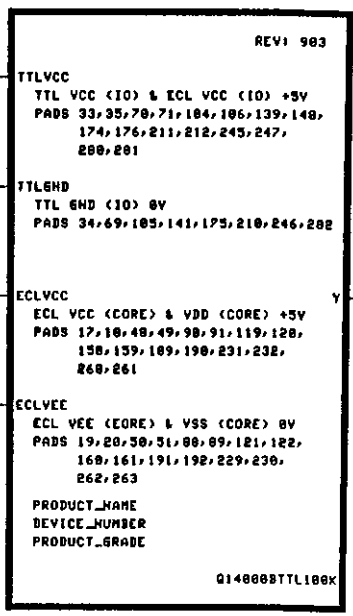
PADS 34,35,69,70,105,106,
140,141,175,176,210,
211,246,247,281,282
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) 0V
PADS 17,18,48,49,90,91,119,120,
150,159,189,190,231,232,
260,261
ECLVEE
ECL VEE (CORE) & VSS (CORE) -4.5V
PADS 19,20,50,51,88,89,121,122,
160,161,191,192,229,230,
262,263
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q14000BM1X100K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TTL VCC (IO) & ECL VCC (IO) +5V
PADS 33,35,70,71,104,106,139,140,
174,176,211,212,245,247,
280,281
TTLGND
TTL GND (IO) 0V
PADS 34,69,105,141,175,210,246,282
ECLVCC
Y
ECL VCC (CORE) & VDD (CORE) +5V
PADS 17,18,48,49,90,91,119,120,
150,159,189,190,231,232,
260,261
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 19,20,50,51,88,89,121,122,
160,161,191,192,229,230,
262,263
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
Q14000BTTL100K

Section 8:

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AMCCANN

VOLUME II, SECTION 8

APPENDIX C

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INTRODUCTION TO AMCCANN

AMCCANN (AMCC Annotation) allows the simulation to be performed with loading delays included for both internal nets and for output loads. Using Front-Annotation files in a simulation allows a more accurate estimate of system performance.

- The Front-Annotation delay file includes the loading delays on internal nets as follows:
  - Actual fan-out load delay
  - Actual wire-or load delay
  - Statistical estimate of the metal load delay based on the number of pins in the net.

- The Front-Annotation delay file includes the loading delays on output nets as follows:
  - Actual system load delay, system load defined by the user
  - Estimated package pin capacitive delay

Pre-layout, the AMCCANN software will provide Front-Annotation delay files to be used in simulation.

After layout is complete, the Back-Annotation program provides the metal load delay information based on the actual net length.

- The Back-Annotation delay file includes the loading delays on internal nets as follows:
  - Actual fan-out load delay
  - Actual wire-or load delay
  - Actual metal load delay from etch length, metal level, and edge direction

- The Back-Annotation delay file includes the loading delays on output nets as follows:
  - Actual system load delay, system load defined by the user
  - Actual package pin capacitive delay from packaging database

After layout, with CIRCUIT.PKG and the CORxxx.ews files available in the directory, the AMCCANN software will provide the Back-Annotation delay files that should be substituted for the Front-Annotation delay files in the simulations.

AMCCANN contains an AMCC user-interface designed to allow the user to supply information on the system capacitive load and package pin capacitance to the annotation software. The annotation delays files will then include the output net capacitive load delay.

AMCCANN should be run once prior to any simulation. It is possible to call AMCCANN and respond to the first prompt with "N", in which case defaults are assumed and the program proceeds.

- AMCCANN can be run successively, each previous edit session is cummulatively available in the data file OUTPUT.DLY. AMCCANN can be run as many times as required to fine-tune the simulation. The file OUTPUT.DLY is the data file created in the first session and then edited by successive executions.

- For drastic editing, the file output.dly can be deleted and the definition process started over.

- If there are no errors in erc/amccerc.lst, AMCCANN will run.

AMCCANN will calculate estimated wire delays and format a file for annotation into the simulation design file. AMCCANN will also prompt the user for an edit session (all default is one option). The user may enter package type, package pin capacitance and system load capacitance values for both global defaults, for individual pins and for groups of pins. Commentary data on toggle frequency and ECL load resistance may also be added.

Output load delays are computed from the data (stored in erc/output.dly) and added to the annotation delay files.

INPUT FILES

The required input files to the AMCCANN program are:

- The erc/circuit.sdi netlist

The optional input files to the AMCCANN program are:

- An existing erc/output.dly
- The package data file CIRCUIT.PKG
- The CORxxx.ews files

OUTPUT.DLY will exist if there has been a previous execution of AMCCANN. The first pass through AMCCANN creates ERC/OUTPUT.DLY. It is not intended as a human-readable file.

CIRCUIT.PKG will exist if place and route have been performed by AMCC and the file has been sent to the EWS (via magnetic media). It contains all placement information plus specific package pin capacitance information.

The CORxxx.ews files will exist if place and route have been performed by AMCC and the files have been sent to the EWS (via magnetic media).

The files CORxxx.ews, for core-delays, and CIRCUIT.PKG, containing package pad-post-pin and specific-pin package pin capacitance data, must be in the ERC sub-directory for DAISY or MENTOR users; in the AGIF sub-directory for VALID.

OUTPUT FILES

The output files produced are:

- The report file AMCCPKG.LST
- The data file OUTPUT,DLY
- Delay files are named FNTxxx.ews where xxx is replaced by MIN, NOM, COM or MIL and ews is the system notation, DAISY=DSY, VALID=VAL, MENTOR=MEN, etc. for Front-Annotation, or BCKxxx.ews for Back-Annotation.
- VALID users will also have the timing verifier files fntxxx.tim or bckxxx.tim.
- The error file AMCCANN.LST (review and discard)

The output report files are located in the erc subdirectory (agif on VALID). The annotation files are placed in the calling directory. For VALID, the *.val files are in the SIM subdirectory and the *.tim files in the TIME subdirectory if the run_dir and run_amcc scripts were used.

DEFAULT VALUES

The Tpd delays for the output macros in the Q14000, Q5000, Q20000 and future macro libraries are specified under "no load" conditions. AMCCANN supplies all loading delay for these macros.

AMCCANN uses a default system capacitive load of 15pF for TTL and 5pF for ECL. The user can specify new default values.

The default package is the package with the largest pin capacitance available for that array in the parameters supplied to the program. The user can specify a package.

The default package pin capacitance is either that specified for the default package, if the package choice was wrong or was defaulted, or that specified for the package selected. The user can specify new default values.

USER INTERFACE VALUES

• The program will prompt for a responce which can be as simple as defaulting all values or specifying global defaults for package pin capacitance, ECL system load and/or TTL system load, or as intricate as specifying different system and package capacitance loading for each of the primary output signals in the circuit.

WAYS TO SPECIFY CAPACITITIVE LOAD

package	default	SELECT FROM MENU	
			SPECIFY BY:
package pin capacitance	default	global	pin-specific
TTL system load	default	global	pin-specific
ECL system load	default	global	pin-specific

• The package is selected from the menu offered for that array. For a different package (by AMCC agreemeent), default the package selection and directly enter package-specific data via other menu prompts. The package, specified or defaulted to, will set the default value for package pin capacitance. There are three values, minimum, typical and maximum.

• The package pin capacitance may be specified as a global value (all package pin data defaults to this specified value). When a value is so specified, it is used as the minimum, typical and maximum values (i.e., all three are identical).

- The package pin capacitance may be specified for an individual pin or group of pins. When a value is so specified, it is used as the minimum, typical and maximum values (i.e., all three are identical).The frequency for any primary input or output may be specified (commentary documentation). Frequency should be entered for any TTL I/O toggling faster than 50MHz and any ECL I/O toggling faster than 100MHz.

- The ECL resistive loading for any ECL output may be specified (also commentary). Resistive loads should be specified when they do not match that assumed for the macro (25 or 50 ohms).

- A previously entered specific pin capacitance or load capacitance for a signal is deleted (reverting to the default value) by giving its name and typing an * for the new value.

DELAY FILES - ANNOTATION

DAISY, MENTOR: In the delay files produced, each net is identified by name (user-defined or default) and is followed by six numbers representing the min, typ and max net delay for both rising and falling edges. Only one file is referenced in the simulation at one time. These delay files provide the internal net interconnect delays due to fan-out, wire-ORs and metal loading. The metal load delay is estimated in the Front-Annotation files. The output net delays due to system and package pin capacitance loading is also computed.
VALID: The delay files contain a rising edge and a falling edge delay value in the fntxxx.val or bckxxx.val files, and a range for rising edge and a range for falling edge delays in the fntxxx.tim and bckxxx.tim files. The *.tim files DO NOT CONTAIN OUTPUT NETS. The VALID timing verifier cannot handle output net delays.

FRONT-ANNOTATION

When AMCCANN is completed, it will have generated the Front-Annotation files FNTMIL.ews or FNTCOM.ews, FNTNOM.ews and FNTMIN.ews (fntxxx.tim files for VALID), as well as the report file AMCCPKG.LST and the data file OUTPUT.DLY. All of these files are to be submitted.

BACK-ANNOTATION

AMCCANN software will take package data from CIRCUIT.PKG and system load data from OUTPUT.DLY to compute output load delays. The output load delay values will be added to the internal net loading delays in the CORxxx.ews files and the Back-Annotation delay files will be generated, called BCKxxx.ews.

The final version of ERC/AMCCPKG.LST will also be generated.

BICMOS PRODUCT GRADE

Note: The BiCMOS library has two commercial timing libraries, one for COMMERCIAL circuits running with a -4.5V power supply (COM4) and one for all other COMMERCIAL circuits (COM5). The Front-Annotation file is still named FNTCOM.ews and provides correct timing based on the ARRAY_FAMILY, PRODUCT_GRADE and the POWER_SUPPLY parameters.

CALLING AMCCANN

Netlist circuit.sdi must exist prior to calling AMCCANN. AMCCANN is called differently on eash EWS. Refer to Volume II, Section 7 for the specific instructions for the system to be used.

On all EWS, AMCCANN invocation exists as a menu option in the run_amcc shell script.

SCREEN PROMPTS

On calling AMCCANN, the screen will prompt:

```
  Need to Edit Package Pin Data?  (YES or NO)   : y

AMCC Delay Annotation VERSION  3.40
Loading Netlist ...
Welcome to the output loading system.

(0) Generate a report and exit.
(1) Change the package type.
(2) Edit the default package pin capacitance.
(3) Edit the default system capacitive load for TTL outputs.
(4) Edit the default system capacitive load for ECL outputs.
(5) Edit the system capacitive load for a specific pin or pins.
(6) Edit the package pin capacitance for a specific pin or pins.
(7) Edit the ECL Resistive Load for a specific pin or pins.
(8) Edit the Frequency for a specific pin or pins.

Enter the number of the item you wish to perform: 1
        0) OTHER.
        1) 84 leaded flat pack cavity up.
        2) 68  PGA cavity down
        3) 84 PGA cavity down
        4) 100 PGA cavity down
        5) 100 PGA cavity up
        6) 100 leaded chip carrier cavity up.
```

```
Type the number of the package that this design
will be using.
4                    <---- FIRST TIME OR A CHANGE

100-PGA-CD           <---- SELECTED PACKAGE


(0) Generate a report and exit.
(1) Change the package type.
(2) Edit the default package pin capacitance.
(3) Edit the default system capacitive load for TTL outputs.
(4) Edit the default system capacitive load for ECL outputs.
(5) Edit the system capacitive load for a specific pin or pins.
(6) Edit the package pin capacitance for a specific pin or pins.
(7) Edit the ECL Resistive Load for a specific pin or pins.
(8) Edit the Frequency for a specific pin or pins.

Enter the number of the item you wish to perform: 2

The current default value for package pin capacitance is
4.60 pf.

Enter <Retn> for no change or enter a new value: 5.3
```

- SELECTING "2" RESULTS IN A PROMPT THAT DEFINES THE EXISTING DEFAULT PACKAGE PIN CAPACITANCE AND PROMPTS FOR A NEW VALUE OR A CARRIAGE RETURN TO LEAVE THE CURRENT VALUE UNCHANGED.

- AS ANNOTATE SCANS THE OLD OUTPUT.DLY FILE, IT WILL REPORT ERRORS THAT WERE NOT YET FIXED (left uncorrected from a previous session).

- ALWAYS READ THE EXISTING AMCCPKG.LST BEFORE EDITING OUTPUT.DLY VIA THE AMCCANN SOFTWARE OR YOU MAY RECEIVE AN ERROR MESSAGE LIKE THIS:

```
Please notify an AMCC Applications Engineer.
A system load of less than five pf is not standard.
```

(0) Generate a report and exit.
(1) Change the package type.
(2) Edit the default package pin capacitance.
(3) Edit the default system capacitive load for TTL outputs.
(4) Edit the default system capacitive load for ECL outputs.
(5) Edit the system capacitive load for a specific pin or pins.
(6) Edit the package pin capacitance for a specific pin or pins.
(7) Edit the ECL Resistive Load for a specific pin or pins.
(8) Edit the Frequency for a specific pin or pins.

Enter the number of the item you wish to perform: 4

The current default value for ECL system capacitance is
5.00 pf.

Enter <Retn> for no change or enter a new value: 6

- SELECTING "4" RESULTS IN A PROMPT THAT DEFINES THE EXISTING DEFAULT ECL SYSTEM LOAD CAPACITANCE AND PROMPTS FOR A NEW VALUE OR A CARRIAGE RETURN TO LEAVE THE CURRENT VALUE UNCHANGED.

- SELECTION "3" WORKS IN THE SAME WAY FOR TTL

(0) Generate a report and exit.
(1) Change the package type.
(2) Edit the default package pin capacitance.
(3) Edit the default system capacitive load for TTL outputs.
(4) Edit the default system capacitive load for ECL outputs.
(5) Edit the system capacitive load for a specific pin or pins.
(6) Edit the package pin capacitance for a specific pin or pins.
(7) Edit the ECL Resistive Load for a specific pin or pins.
(8) Edit the Frequency for a specific pin or pins.

Enter the number of the item you wish to perform: 5

• SELECTING "5", THE SYSTEM PROMPTS WITH A LIST OF ALL OUTPUTS AND BIDIRECTIONAL SIGNALS:

OUT001 OUTC OUTE PARAM YOUTPT

• IT THEN PROMPTS FOR A LIST OF ONE OR MORE SIGNAL NAMES. A CARRIAGE RETURN WILL RETURN IT TO THE MAIN MENU.

Enter the signal name or signal names separated by spaces.

param

• WHEN A CARRIAGE RETURN IS DETECTED ON A NON-EMPTY LIST, THE SYSTEM PROMPTS FOR A NEW VALUE FOR THE PIN. THE EXISTING VALUE IS NOT DISPLAYED. REFER TO THE EXISTING AMCCPKG.LST FOR PREVIOUS EDIT SESSIONS.

Enter the new value (pf): 50

• THE SYSTEM REPROMPTS FOR A LIST:

Enter the signal name or signal names separated by spaces.

• ON CARRIAGE RETURN ON AN EMPTY LIST, THE MAIN MENU IS DISPLAYED.

(0) Generate a report and exit.
(1) Change the package type.
(2) Edit the default package pin capacitance.
(3) Edit the default system capacitive load for TTL outputs.
(4) Edit the default system capacitive load for ECL outputs.
(5) Edit the system capacitive load for a specific pin or pins.
(6) Edit the package pin capacitance for a specific pin or pins.
(7) Edit the ECL Resistive Load for a specific pin or pins.
(8) Edit the Frequency for a specific pin or pins.

Enter the number of the item you wish to perform: **6**

o SELECTING "6", THE SYSTEM PROMPTS WITH A LIST OF ALL OUTPUTS AND BIDIRECTIONAL SIGNALS:

OUT001 OUTC OUTE PARAM YOUTPT

Enter the signal name or signal names separated by spaces.

youtpt

Enter the new value (pf): 18

Enter the signal name or signal names separated by spaces.

• A "6" OPERATES THE SAME AS "5" EXCEPT THAT IT IS DEFINING A PACKAGE PIN CAPACITANCE RATHER THAN A SYSTEM LOAD.

(0) Generate a report and exit.
(1) Change the package type.
(2) Edit the default package pin capacitance.
(3) Edit the default system capacitive load for TTL outputs.
(4) Edit the default system capacitive load for ECL outputs.
(5) Edit the system capacitive load for a specific pin or pins.
(6) Edit the package pin capacitance for a specific pin or pins.
(7) Edit the ECL Resistive Load for a specific pin or pins.
(8) Edit the Frequency for a specific pin or pins.

Enter the number of the item you wish to perform: 7

• SELECTION "7" RESPONDS WITH A LIST OF ALL PRIMARY I/O SIGNALS.

DAT0	DAT1	DAT10	DAT11	DAT12
DAT13	DAT14	DAT15	DAT2	DAT3
DAT4	DAT5	DAT6	DAT7	DAT8
DAT9	EXTCLK	EXTRST	IN001	OUT001
OUTC	OUTE	PARAM	SELCT0	SELCT1
SELCT2	SELCT3	YOUTPT		

Enter the signal name or signal names separated by spaces.
param

• THE LIST IS ONE OR MORE SIGNALS

Enter the new value (Ohms): 40

• A NON-EMPTY LIST WILL PROMPT FOR AN ECL TERMINATION VALUE.

Enter the signal name or signal names separated by spaces.

(0) Generate a report and exit.
(1) Change the package type.
(2) Edit the default package pin capacitance.
(3) Edit the default system capacitive load for TTL outputs.
(4) Edit the default system capacitive load for ECL outputs.
(5) Edit the system capacitive load for a specific pin or pins.
(6) Edit the package pin capacitance for a specific pin or pins.
(7) Edit the ECL Resistive Load for a specific pin or pins.
(8) Edit the Frequency for a specific pin or pins.

Enter the number of the item you wish to perform: 8

• SELECTION "8" RESPONDS WITH A LIST OF ALL PRIMARY I/O SIGNALS.

DAT0	DAT1	DAT10	DAT11	DAT12
DAT13	DAT14	DAT15	DAT2	DAT3
DAT4	DAT5	DAT6	DAT7	DAT8
DAT9	EXTCLK	EXTRST	IN001	OUT001
OUTC	OUTE	PARAM	SELCT0	SELCT1
SELCT2	SELCT3	YOUTPT		

Enter the signal name or signal names separated by spaces.

extclk

• THE LIST IS ONE OR MORE SIGNALS

Enter the new value (MHz): 100

• A NON-EMPTY LIST WILL PROMPT FOR A FREQUENCY IN MHz.

Enter the signal name or signal names separated by spaces.

• ALWAYS, A SECOND, THIRD, ... LIST CAN BE ENTERED OR A CARRIAGE RETURN USED TO GO TO THE MAIN MENU.

```
(0) Generate a report and exit.
(1) Change the package type.
(2) Edit the default package pin capacitance.
(3) Edit the default system capacitive load for TTL outputs.
(4) Edit the default system capacitive load for ECL outputs.
(5) Edit the system capacitive load for a specific pin or pins.
(6) Edit the package pin capacitance for a specific pin or pins.
(7) Edit the ECL Resistive Load for a specific pin or pins.
(8) Edit the Frequency for a specific pin or pins.

Enter the number of the item you wish to perform: 0

Exiting and writing AMCCPKG.LST.
Processing MIN Front Annotation Delay File ...
Processing NOM Front Annotation Delay File ...
Processing MIL Front Annotation Delay File ...
All Done.

  ******  AMCCANN COMPLETED SUCCESSFULLY !!!  ********
```

DEFAULT SYSTEM CAPACITANCE

ECL	5pf
TTL	15pf

Use AMCCANN user-interface menu to set the default to another value or to set individual signals or groups of signals to different system capacitive load values. Values for ECL or TTL system capacitive loads assigned to signals on paths under timing correlation, AT speed analysis or AC test should match those used in computation of the specification for those paths.

SYSTEM LOAD SHOULD NOT BE SET BELOW 5pf. Consult AMCC for a waiver (PAR) for special cases.

DEFAULT PACKAGES; PACKAGE PIN CAPACITANCE
FOR ARRAYS (903) *

ARRAY	PACKAGE CODE	MIN pf	TYP pf	MAX pf
Q1300T	84_PGA_CD	3.4	4.2	13.3
QM1600T	149_PGA_CD	4.0	5.3	6.2
Q3500T	149_PGA_CD	4.0	5.3	6.2
Q5000T	225_PGA_CD	6.6	8.1	9.6
Q2100B	84_PGA_CD	3.4	4.2	13.3
Q6000B	169_PGA_CD	3.9	4.7	5.1
Q9100B	225_PGA_CD	6.6	8.1	9.6
Q14000B	301_PGA_CD	8.0	11.1	15.0

* VARIES BY RELEASE

The default package assigned to an array is the one with the largest package pin capacitance. Override a default selection by selecting a package from those available at the start of the AMCCANN session or by requesting menu option "(1) CHANGE THE PACKAGE TYPE". If "0) OTHER" was the package chosen, the default package pin capacitances will be in effect until new values are specified by the user.

Note: At this time, AMCCANN has no knowledge of signal pin requirements, therefore, if a package is selected that is too small for the circuit, AMCCANN will not issue any error messages. Verify that the correct package is being used. Refer to Section 5, Volume I for package selection procedures.

DEFAULT PACKAGE PIN CAPACITANCE BY PACKAGE

PACKAGE	CTR	MIN pf	TYP pf	MAX * pf	ARRAYS
84_LDFP	50	3.8	4.3	4.9	Q1300T, Q3500T, Q2100B
100_LDCC	50	3.8	4.3	4.9	Q1300T, QM1600T, Q3500T, Q2100B
100_LDCC	25	3.8	4.3	4.9	Q1300T (25 mil center)
132_LDCC	25	1.5	1.9	2.2	Q5000T, QM1600T, Q3500T, Q9100B, Q14000B
172_LDCC	25	2.4	3.0	3.6	Q6000B (in devel.) PRELIMINARY
196_LDCC	25	2.4	3.0	3.6	Q5000T, Q9100B, Q14000B
68_PGA_CD		2.5	3.5	6.9	Q1300T, Q2100B
84_PGA_CD		3.4	4.2	13.3	Q1300T, Q2100B
100_PGA_CD		3.2	3.8	4.6	Q1300T, QM1600T, Q3500T, Q2100B, Q6000B (in devel.)
100_PGA_CU		3.2	3.8	4.6	Q1300T, QM1600T, Q3500T
149_PGA_CD		4.0	5.3	6.2	QM1600T, Q3500T, Q5000T
169_PGA_CD		3.9	4.7	5.1	Q6000B, Q9100B, Q14000B
225_PGA_CD		6.6	8.1	9.6	Q5000T, Q9100B, Q14000B
301_PGA_CD		8.0	11.1	15.0	Q14000B

* MAX IS VALUE USED IN MIL or COM ANNOTATION FILE COMPUTATIONS
MIN IS VALUE USED IN MIN ANNOTATION FILE COMPUTATIONS
TYP IS VALUE USED FOR NOM ANNOTATION FILE COMPUTATIONS

Use AMCCANN user-interface menu to set the default package pin capacitances to another value or to set individual signals or groups of signals to different package pin capacitance values.

PACKAGE PIN CAPACITANCE SHOULD NOT BE SET TO ZERO. Consult AMCC for a waiver (PAR) for special cases.

Note: At this time, setting a package pin capacitance to a new value sets all three entries (min, typ, max) to the same value. Run AMCCANN twice for custom package pin capacitances: once for the maximum value on the pins and one for the minimum value. Default values will execute correctly.

OUTPUT.DLY

pkgkey	3 systtl_cap	20.00	sysecl_cap	6.00	pkgmin_cap	3.80	pkgtyp_cap	4.40	pkgmax_cap	4.90
EXTCLK	0.00	0.00	0.00	0.00	100.00					
OUT001	6.00	3.80	4.40	4.90						
OUTC	6.00	3.80	4.40	4.90	0.00	50.00				
OUTE	6.00	3.80	4.40	4.90						
PARAM	6.00	8.00	8.00	8.00	100.00					
YOUTPT	12.00	12.00	12.00	12.00	100.00	55.00				

Package name = 224-PGA-CD

Item #	Signal Name	Instance Name	Macro Name	PAD	Frq MHz	ECL R	System pf	Package Capacitance Min pf	Typ pf	Max pf
1	!DAT0	!S0001	!IT11H							
2	!DAT1	!S0002	!IT11H							
3	!DAT10	!S0011	!IT11H							
4	!DAT11	!S0012	!IT11H							
5	!DAT12	!S0013	!IT11H							
6	!DAT13	!S0014	!IT11H							
7	!DAT14	!S0015	!IT11H							
8	!DAT15	!S0016	!IT11H							
9	!DAT2	!S0003	!IT11H							
10	!DAT3	!S0004	!IT11H							
11	!DAT4	!S0005	!IT11H							
12	!DAT5	!S0006	!IT11H							
13	!DAT6	!S0007	!IT11H							
14	!DAT7	!S0008	!IT11H							
15	!DAT8	!S0009	!IT11H							
16	!DAT9	!S0010	!IT11H							
17	!EXTCLK	!S0021	!IE93		100.0					
18	!EXTRST	!S0022	!IE93							
19	!IN001	!E10000	!IE86							
20	!OUT001	!E00000	!OE87				6.0	3.80	4.40	4.90
21	!OUTC	!E0001	!OE87			50.0	6.0	3.80	4.40	4.90
22	!OUTE	!E00002	!OE87				6.0	3.80	4.40	4.90
23	!PARAM	!E04000	!OE81		100.0		6.0	8.00	8.00	8.00
24	!SELCT0	!S0020	!IT11H							
25	!SELCT1	!S0019	!IT11H							
26	!SELCT2	!S0018	!IT11H							
27	!SELCT3	!S0017	!IT11H							
28	!YOUTPT	!D0000	!OE80		100.0	55.0	12.0	12.00	12.00	12.00
29	!ITGND	!GNT03	!ITGND							
30	!ITGND	!GNT02	!ITGND							
31	!ITGND	!GNT01	!ITGND							
32	!ITPWR	!PW002	!ITPWR							

```
/* Daisy design pathname:  /USER/CLASS/MUX16  */
$CONTROL
MODE ADD
SECTION DELAY:N:6
$DELAY
/*                                  R I S E          F A L L          */
/*                                Typ  Min  Max    Typ  Min  Max     */
@MUX16/4:XSIG1          =       0    0    0      0    0    0  ;
@MUX16/4:XSIG2          =       0    0    0      0    0    0  ;
@MUX16/4:XSIG27         =      26   23   28     51   46   56  ;
@MUX16/4:XSIG42         =      26   23   28     51   46   56  ;
@MUX16/4:XSIG5          =       0    0    0      0    0    0  ;
@MUX16/4:XSIG54         =      26   23   28     51   46   56  ;
@MUX16/2:INP0           =      13   12   14     26   23   28  ;
@MUX16/2:INP1           =      13   12   14     26   23   28  ;
@MUX16/2:INP10          =      13   12   14     26   23   28  ;
@MUX16/2:INP11          =      13   12   14     26   23   28  ;
@MUX16/2:INP12          =      13   12   14     26   23   28  ;
@MUX16/2:INP13          =      13   12   14     26   23   28  ;
@MUX16/2:INP14          =      13   12   14     26   23   28  ;
@MUX16/2:INP15          =      13   12   14     26   23   28  ;
@MUX16/2:INP2           =      13   12   14     26   23   28  ;
@MUX16/2:INP3           =      13   12   14     26   23   28  ;
@MUX16/2:INP4           =      13   12   14     26   23   28  ;
@MUX16/2:INP5           =      13   12   14     26   23   28  ;
@MUX16/2:INP6           =      13   12   14     26   23   28  ;
@MUX16/2:INP7           =      13   12   14     26   23   28  ;
@MUX16/2:INP8           =      13   12   14     26   23   28  ;
@MUX16/2:INP9           =      13   12   14     26   23   28  ;
@MUX16/2:INTCLK         =      26   23   28     26   23   28  ;
@MUX16/2:INTON          =      13   12   14     26   23   28  ;
@MUX16/2:INTRST         =      26   23   28     26   23   28  ;
@MUX16/2:INTY0          =      13   12   14     26   23   28  ;
@MUX16/2:INTY1          =      13   12   14     26   23   28  ;
@MUX16/2:INTY2          =      13   12   14     26   23   28  ;
@MUX16/2:INTY3          =      13   12   14     26   23   28  ;
@MUX16/2:INTY4          =      13   12   14     26   23   28  ;
@MUX16/3:PARA1          =      13   12   14     26   23   28  ;
@MUX16/3:PARA10         =      13   12   14     26   23   28  ;
@MUX16/3:PARA11         =      13   12   14     26   23   28  ;
@MUX16/3:PARA12         =      13   12   14     26   23   28  ;
@MUX16/3:PARA13         =      13   12   14     26   23   28  ;
@MUX16/3:PARA14         =      13   12   14     26   23   28  ;
@MUX16/3:PARA15         =      13   12   14     26   23   28  ;
@MUX16/3:PARA16         =      13   12   14     26   23   28  ;
@MUX16/3:PARA17         =      13   12   14     26   23   28  ;
@MUX16/3:PARA18         =      13   12   14     26   23   28  ;
@MUX16/3:PARA19         =      13   12   14     26   23   28  ;
@MUX16/3:PARA2          =      13   12   14     26   23   28  ;
@MUX16/3:PARA20         =      13   12   14     26   23   28  ;
@MUX16/3:PARA3          =      13   12   14     26   23   28  ;
@MUX16/3:PARA4          =      13   12   14     26   23   28  ;
@MUX16/3:PARA5          =      13   12   14     26   23   28  ;
@MUX16/3:PARA6          =      13   12   14     26   23   28  ;
@MUX16/3:PARA7          =      13   12   14     26   23   28  ;
@MUX16/3:PARA8          =      13   12   14     26   23   28  ;
@MUX16/3:PARA9          =      13   12   14     26   23   28  ;
@MUX16/2:PARCLK         =      26   23   28     26   23   28  ;
@MUX16/2:PARRST         =      26   23   28     26   23   28  ;
@MUX16/2:SEL0           =      36   33   40     72   65   80  ;
@MUX16/2:SEL1           =      36   33   40     72   65   80  ;
@MUX16/2:SEL2           =      13   12   14     26   23   28  ;
@MUX16/2:SEL3           =      13   12   14     26   23   28  ;
@MUX16/4:OUT@@1         =      62   52   71     51   43   58  ;
@MUX16/4:OUTC           =      62   52   71     51   43   58  ;
@MUX16/4:OUTE           =      62   52   71     51   43   58  ;

@MUX16/4:PARAM          =      83   75   91     68   62   75  ;
@MUX16/2:YOUTPT         =     143  129  157    117  106  129  ;
$END
```

Front-Annotation file showing output nets at end

VALID - WHEN BIDIRECTIONALS ARE USED

AMCCANN annotation for bidirectional macros when a workaround is used (see VALID Volume II, Section 7) will be used as follows by the VALID simulator:

- The output net will be included when the circuit is in INPUT mode because it will be considered as an internal net (between the added input macro for PI and the actual bidirectional macro.

- The Tpd delay of the added input macro will also be included in this path.

- Only the output net delay will be used when the macro is in the OUTPUT mode.

Both the Tpd and the net delay (correctly adjusted for MIL, COM or MIN) must be subtracted from the path delays computed for bidirectional macros acting as inputs.

The path delays for bidirectional macros acting as outputs are correct.

The problem of the workaround is being addressed by VALID and AMCC.

VALID - TIMING VERIFIER

The VALID timing verifier does not handle output net delays (due to capacitve load). AMCCANN produces *.tim files that are correctly formatted for the timing verifier and that exclude the output nets.