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AMCC

Dear AMCC Customer,

We are pleased to provide you with the AMCC MacroMatrix software for the Q14000 BiCMOS Logic Array Series, which includes the macro library and design support software. We are excited about this new technology which provides the benefits of having speed, high density and low power on the same chip.

The macro library and design manual are individually registered to you. To request another copy of the Q14000 Design Manual, contact your local AMCC sales representative. A Q14000 Design Guide is available for those not actively doing a design.

Should you require additional assistance, please do not hesitate to call any of our application engineers at (619) 450-9333.


# Volume I
# Q14000 Series

## BiCMOS Logic Arrays

Applied MicroCircuits Corporation

# Q14000
# BiCMOS Series
# Design Manual

Includes: Q2100B, Q9100B
BiCMOS Logic Arrays

The material in this document
supercedes all previous
documentation issued for the
Q14000 BiCMOS Series Logic Arrays







M1401-0388

# Section 1:

# Introduction

# INTRODUCTION

This design manual provides a summary of the AMCC (Applied Micro Circuits Corporation) Q14000 Series BiCMOS Logic Arrays. Volume 1 is composed of the following sections:

- Section 1: Introduction
- Section 2: Design Methodology
- Section 3: Timing Analysis
- Section 4: External $t_{su}$, $t_h$
- Section 5: Power/Packaging
- Section 6: Macro Library Documentation
  - Section 6-1: TTL Interface
  - Section 6-2: TTLMIX Interface
  - Section 6-3: ECL Interface
  - Section 6-4: Internal Logic Macros
  - Section 6-5: Special Macros
- Section 7: Quicksheets
- Section 8: Index

It also includes information on:

- Product features
- Performance specifications
- Design Interface and support

and contains a listing of the macros currently available. The AMCC Packaging Brochure should also be referenced for further information on packaging.

The Q14000 Series supports the following arrays:

TABLE 1-1
SUPPORTED ARRAYS

- Q9100B
- Q2100B

Volume 1 of this design manual is intended as a self-contained design aid to allow the proper selection of an array for a particular design, to indicate the packaging available for that array, and to provide the designer with a better understanding of the capabilities of the Q14000 Series BiCMOS Logic Arrays.

Section 2 contains design rules specific to this array series. Interconnect rules and testing requirements are included in this section.

The macro summary and detailed macro specifications are presented in reference manual format in Section 6 with a rapid graphic reference provided via quicksheets in Section 7. Either a macro-conversion of an existing design, or the direct design of a circuit can be implemented using the available macros.

Volume 2 of this design manual is composed of the following sections:

- Section 1: Introduction
- Section 2: EWS-Specific Design Methodology
- Section 3: EWS Schematic Rules and Conventions
- Section 4: Vector Submission Rules and Guidelines
- Section 5: Design Validation
- Section 6: Design Submission
- Section 7: MacroMatrix® Installation
- Section 8: MacroMatrix User's Guide
- Section 9: AMCC Glossary
- Section 10: Index

Volume 2, Section 2 of this design manual contains the Engineering-workstation (EWS) design methodology, covering both the EWS-specific operations and the AMCC MacroMatrix support software.

Section 8 contains the MacroMatrix User's Guide which details the Engineering Rules Check (AMCCERC, a.k.a., ERC) software checks and error messages and probable causes. It also includes the Vector Rules Check (AMCCVRC) user's guide. Section 9 contains the MacroMatrix Installation and Operations manual, which summarizes the EWS-specific commands required for operation of the AMCC support software.

The Design Validation document in Section 5 details the engineering rules checks that must be reviewed prior to design submission. It is the basic outline of the design review AMCC performs prior to circuit acceptance. Fill in or check off items as indicated and submit the entire document as part of the design submission package. Additional copies can be obtained from AMCC.

The Design Submission Document in Section 6 is to be completed and submitted along with the design submission package. Additional copies can be obtained from AMCC.

The following trademarks are recognized by AMCC throughout this design manual:

- TEGAS V - General Electric Co.
- COPTR - General Electric Co.
- LOGICIAN - Daisy Systems Corp.
- GATEMASTER - Daisy Systems Corp.
- Mentor Graphics
- MacroMatrix - AMCC
- Tektronix/CAE Systems
- Valid Logic

## Q14000 SERIES DESCRIPTION

The AMCC Q14000 Series Logic Arrays provide an optimized systems approach to BiCMOS semi-custom applications. CMOS logic for low power is combined with bipolar drivers for high drive capability within each internal cell. Mixed-mode I/O is combined with an advanced, interactive CAD system-based design approach to provide a quick and cost-effective solution to discrete IC replacement. Manufacturing advantages gained from the use of the AMCC logic arrays include:

- Increased circuit density
- Increased system speed
- Reduced power
- Higher reliability
- Lower system cost
- Operation over both military and commercial temperature ranges

The AMCC Q14000 Series Logic Arrays Macro Library is supported on the Daisy, Mentor Graphics, Valid Logic and Tektronix/CAE Systems EWS. The designer can use any of these systems in conjunction with AMCC's MacroMatrix software package to perform schematic capture, Engineering Rules Checking (AMCCERC), simulation, automatic test pattern formatting (AMCCSIMFMT), AMCC Vector Rules Checking (AMCCVRC), Front-Annotation and Back-Annotation. Simulation, AMCCERC error checking, AMCCVRC rules checking, Front-Annotation and Back-Annotation are also supported on VAX/VMS systems with TEGAS 5.

The Q14000 Series arrays are BiCMOS arrays. They have the ability to externally interface to either Schottky TTL, ECL 10K or ECL 100K. ECL 10K or ECL 100K may be standard-reference or +5V reference ECL.

As an added feature, the Q14000 Series provides the ability to mix ECL 10K and TTL or ECL 100K and TTL on the same array. ECL 10K and ECL 100K outputs are also allowed on the same array, regardless of the ECL type used for input. For other combinations, please contact AMCC Marketing.

All of the interface options are realized through the choice of appropriate macros, and personalized with the metal masks only.

AMCC describes the density of its logic arrays in terms of equivalent gates (2-input NAND gates), which are a function of the density of the available macros and the number of cells available in any given array. The density of the Q14000 Series is described below.

TABLE 1-2
ARRAY DENSITY

| Array | Equivalent Gates |
|---|---|
| Q9100B | 9072 |
| Q2100B | 2160 |

The arrays in the Q14000 Series share a common macro function library which contains a wide selection of fully characterized logic functions varying from SSI to MSI densities. The higher functionality macros have correspondingly higher equivalent gate densities.

Examples of the basic logic functions include simple and complex gates, EXOR-nets, latches, decoders, MUXs, 4-bit counters, a 4-bit universal register, buffered input, high-speed ECL input, buffered and unbuffered output and ECL output macros which contain logic, buffers and output translation.

AMCC logic arrays are structured to allow the components spread across several cells to be interconnected into a single high-functionality MSI macro. These hard-wired MSI macros guarantee consistent and predetermined circuit performance. AMCC recommends that designers use the higher functionality MSI macros whenever possible.

Many interface macros in the Q14000 Series macro library have high-speed (H) options in addition to the standard (S) option of the macro. These macro options allow a designer to selectively program critical I/O paths with high-speed operation while implementing the remainder of the I/O in lower power standard-option macros.

## TYPICAL APPLICATIONS

Typical applications include high-speed computers, graphics, communications, test equipment and instrumentation. Designed to operate in the full MIL-SPEC temperature and voltage range, the Q14000 Series also has applications in radar, EW, avionics, guidance, flight simulation and other military systems.

## FEATURES

A summary of the features of the Q14000 Series includes:

- 9072 and 2160 equivalent gate versions
- 1.5-micron Bipolar/CMOS technology - N-type epitaxial for both NPN oxide-isolated bipolar and CMOS
- 2-layer metal to customize base array
- 100% autoplace and autoroute with up to 95% logic cell utilization
- Extensive macro library, upwardly compatible with the Q3500 and Q1500 Series library
- System-level multiple-cell MSI macros
- Schottky TTL, low-power Schottky TTL, ECL 10K and ECL 100K I/O compatibility
- Standard-reference ECL or +5V referenced ECL
- Speed/power programmable I/O macros
- On-chip translators for mixed mode interface
- Both ECL 10K and ECL 100K outputs may appear on the same array

- Lower overall worst-case multipliers than CMOS
- Fast on-off chip delays
- Low fan-out degradation
- High internal noise immunity
- Unused cells do not dissipate power
- Internal core uses no DC current despite bipolar drivers
- Multiple power supply options available
- Fully voltage- and temperature-compensated internal logic
- Full MIL operating range ($-55^{o}C$ ambient to $+125^{o}C$ case, $\pm 10\%$ power supply)
- Wide selection of packaging
- Supported on engineering workstations:
  - Daisy
  - Valid Logic
  - Mentor Graphics
  - Tektronix/CAE systems
- Supported on TEGAS 5
- Full CAD support, including post-autoroute, worst-case timing analysis

## DESIGN INTERFACE AND SUPPORT

The AMCC circuit development interface has been structured to be highly flexible with respect to the customer's desired level of involvement. The basic steps are summarized below:

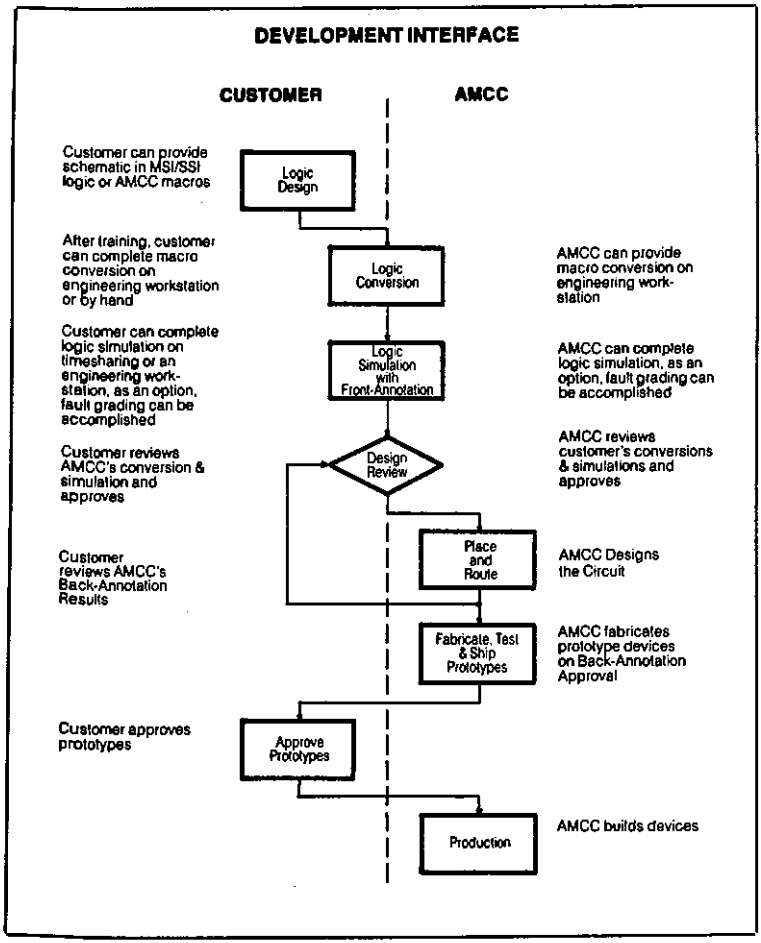



**FIGURE 1-1**

# Section 2:

# Design Methodology

Table of Contents

## DEVICE ARCHITECTURE

The AMCC logic arrays are formed from a customer specified design added to an AMCC pre-processed silicon base array. The base array for the Q14000 Series BiCMOS arrays is composed of two types of cells, I/O and Basic cells. Each cell consists of a number of uncommitted transistors and resistors.

TABLE 2-1
Q14000 SERIES CELL RESOURCE SUMMARY

| Cell Type | Quantity Q9100B | Q2100B |
|---|---|---|
| Logic (Basic cell) | 2268 | 540 |
| Interface (I/O) | 160 | 80 |

The basic cell layout of the arrays is demonstrated with the Q9100B, shown in Figure 2-1. Table 2-1 summarizes the internal cell resources and Table 2-2 summarizes the I/O resources for the Q14000 logic array series.

## MACRO CONFIGURATION

A customer design is described via schematics using the macros contained in the released library for the array series. Macros are individually configured in an array by interconnecting the components within a cell with the first layer metal to form the customer-selected macro functions. Macro placement is performed automatically by the AMCC proprietary CAD software.

# Q9100 DIE LAYOUT

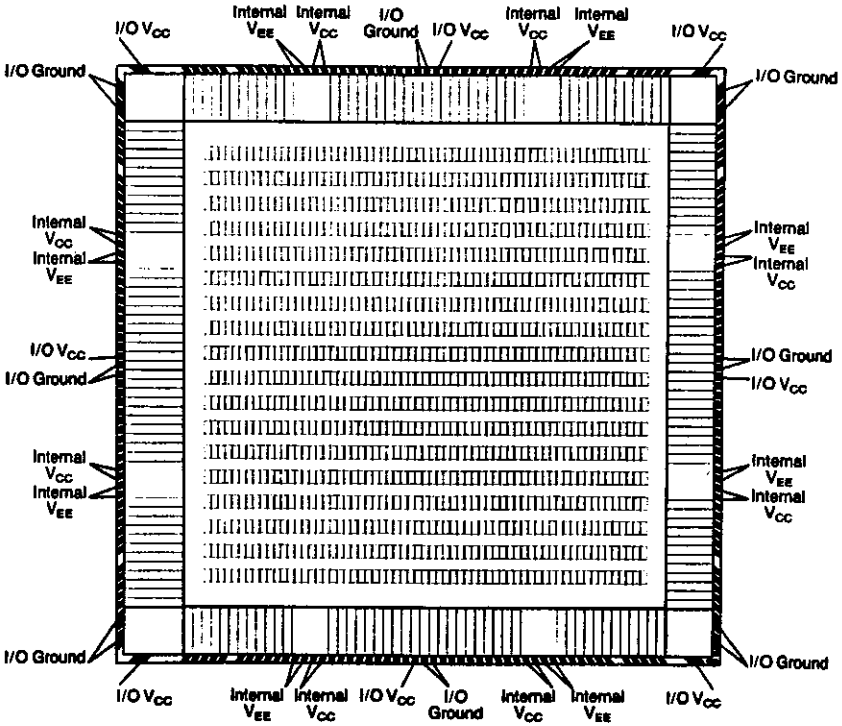



**FIGURE 2-1**

TABLE 2-2
I/O RESOURCES

| MODE | DESCRIPTION | Q9100B | Q2100B |
|---|---|---|---|
| TTL | I/O Cells | 160 | 80 |
| SYSTEM | $V_{CC}$ (+5V) | 32 | 16 |
| | GROUND | 24 | 12 |
| ECL | I/O Cells | 160 | 80 |
| SYSTEM | $V_{CC}$ ** | 40 | 20 |
| any | $V_{EE}$ * | 16 | 8 |
| MIXED | I/O Cells | 160 | 80 |
| TTLMIX | $V_{CC}$ (+5$V_{DC}$ NOM) | 8 | 4 |
| and ECL | $V_{EE}$ * | 16 | 8 |
| SYSTEM | TTL GROUND | 8 | 4 |
| | ECL $V_{CC}$ ** | 24 | 12 |
| MIXED | | | |
| +5V | I/O cells | 160 | 80 |
| SYSTEM | $V_{CC}$ (+5$V_{DC}$ NOM) | 32 | 16 |
| | GROUND | 24 | 12 |

* $V_{EE}$ is -5.2V FOR STD-REF ECL 10K
-4.5V FOR STD-REF ECL 100K
0V FOR +5V REF ECL 10K OR ECL 100K

** $V_{CC}$ is 0V FOR STD-REF ECL 10K
0V FOR STD-REF ECL 100K
+5V FOR +5V REF ECL 10K OR ECL 100K

## INTERCONNECTIONS AND ROUTING

Interconnections between macros (routing) use both the first and second layers of metal, following specific routing tracks. Routing is performed automatically by AMCC proprietary CAD software. To allow for a high logic cell utilization and an optimum layout for high-speed logic designs, a liberal allocation of first metal vertical routing tracks and second metal horizontal routing tracks have been incorporated into the architecture for each array.

Additionally, the AMCC CAD software has been designed to automatically transform a logic design implemented in AMCC macros into an efficient high performance layout design. If there are sensitive timing and/or skew constraints, AMCC can optionally offer preplacement of the macros implementing these critical areas.

The customization of the array is performed by adding the 2-layer metal interconnect, representing the macros and their interconnection, to the base array.

## BASIC CELLS

The internal logic cells, called Basic cells, utilize both CMOS and bipolar devices. The internal logic is performed in CMOS while the bipolar device pairs provide necessary drive capability.

The Basic cells are organized to support high-level logic functions such as latches, multiplexors, decoders, etc. Simple and complex gates can also be made from these cells.

## I/O CELLS

The interface to the arrays is accomplished in the 100% bipolar input/output cells on the Q14000 Series Logic Arrays. The I/O cells are located around the perimeter of the array. For all arrays, ECL- and TTL-translators and most of the required buffers are included in the I/O cells for external interfacing to both ECL and TTL. Each individual I/O cell is configurable to be either TTL, ECL 10K or ECL 100K.

## OVERHEAD CIRCUITRY

In addition to the cells, each array contains overhead circuitry: bias generators, voltage references and voltage regulators. Overhead circuitry is predefined by AMCC.

## INTERFACE OPTIONS

The array itself can be configured to be 100% TTL, 100% ECL 10K, 100% ECL 100K, TTL/ECL 10K or TTL/ECL 100K, with either dual power supplies or a single +5V supply available for either the 100% ECL or mixed mode I/O circuits. (See Table 2-3.) In addition, both ECL 10K and ECL 100K outputs may be usd on any given array. Only one type of ECL is allowed for input.

TABLE 2-3
POWER SUPPLY OPTIONS*

| | SINGLE POWER SUPPLY | | | DUAL POWER SUPPLY | |
|---|---|---|---|---|---|
| | +5V | -5.2V | -4.5V | +5V/-5.2V | +5V/-4.5V |
| 100% TTL | • | - | - | - | - |
| 100% ECL 10K | • | • | • | - | - |
| 100% ECL 100K | • | • | • | - | - |
| ECL 10K/TTL | • | - | - | • | • |
| ECL 100K/TTL | • | - | - | • | • |

* ECL 10K can be operated at ECL 100K voltages and visa versa

## INTERFACE GUIDELINES

A summary of the interface guidelines for the four I/O modes of operation are shown in Figure 2-2. Most of the I/O macros for the Q14000 Series include buffer functions, to simplify I/O selection. The designer should review the I/O options to determine where these options would enhance the circuit efficiency.

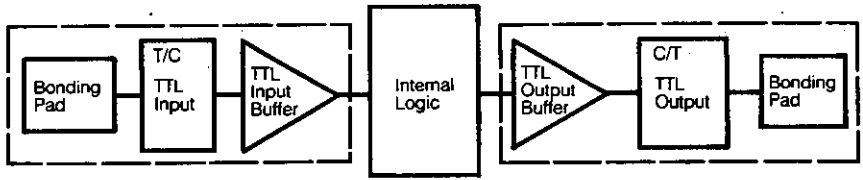
## MACRO SUMMARY

Refer to the macro summary and index (Section 6) for a list of the macros available for the Q14000 Series Logic Arrays. The library and its summary sheets are for use during macro conversion or when creating a new design directly from the available functions. If other macro functions are desired, please consult AMCC.

The macro summary in Section 6 is divided into six segments: TTL Interface, TTLMIX Interface, ECL Interface, Basic Logic Macros, MSI Macros and Special macros. The macros are in alphabetical order within those sections.

## Q14000 SERIES INTERFACE MACRO GUIDELINES

**100% TTL INTERFACE**
**Single +5V Power Supply**



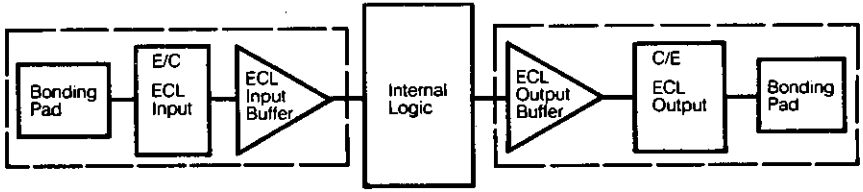

**Q14000 SERIES INPUT:**
- Use TTL interface macros
- TTL input macros contain necessary buffers internally

**Q14000 SERIES OUTPUT:**
- Use TTL interface macros
- TTL output macros contain necessary buffers internally.

**FIGURE 2A**

## Q14000 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

**100% ECL INTERFACE**
**Single −5.2V, −4.5V**
**or +5V Power Supply**



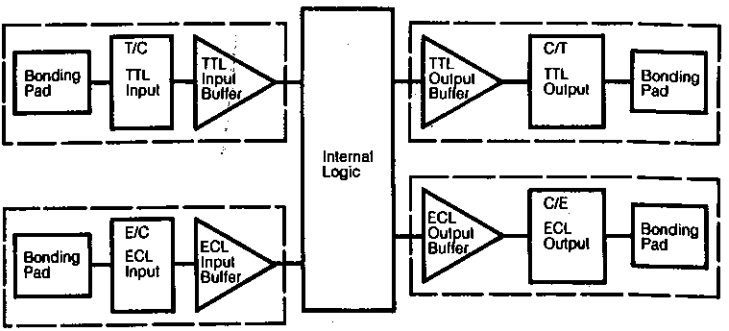

**Q14000 SERIES INPUT:**
- Use ECL interface macros (IExx)
- ECL input macros contain necessary buffer internally.
- Same macro for either +5V, −5.2V or −5.4V supply

**Q14000 SERIES OUTPUT:**
- Use ECL interface macros
- ECL available in 50 ohm terminations only
- ECL output macros contain necessary buffers internally
- Supports both ECL 10K (OExx) and ECL 100K (OKxx)
- Same macro for either +5V, −5.2V or −4.5V supply
- No limit on number of 50 ohm outputs

**FIGURE 2B**

## Q14000 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

**MIXED ECL/TTL INTERFACE**
**Single +5V Power Supply**



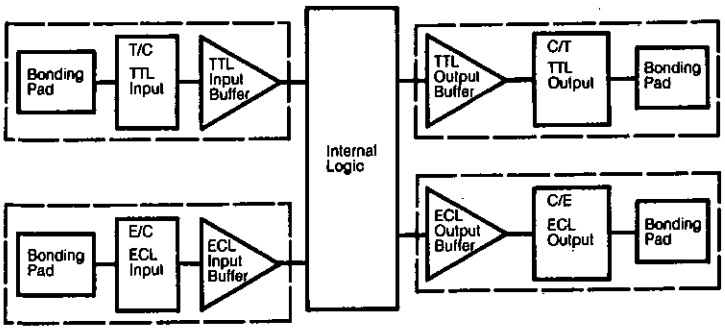

**Q14000 SERIES INPUT:**
- TTL: Identical to guidelines for 100% TTL circuits
- ECL: Identical to guidelines for 100% ECL circuits

**Q14000 SERIES OUTPUT:**
- TTL: Identical to guidelines for 100% TTL circuits
- ECL: Identical to guidelines for 100% ECL circuits

**FIGURE 2C**

## Q14000 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

**MIXED ECL/TTL INTERFACE**
**+5V and −5.2V Power Supply**
**or +5V and −4.5V Power Supply**




**Q14000 SERIES INPUT:**
- TTL: Identical to guidelines for 100% TTL circuits except use TTLMIX macros
- ECL: Identical to guidelines for 100% ECL circuits

**Q14000 SERIES OUTPUT:**
- TTL: Identical to guidelines for 100% TTL circuits except use TTLMIX macros
- ECL: Identical to guidelines for 100% ECL circuits

**FIGURE 2D**

## I/O MACROS

Interface macros are documented in Sections 6-1, 6-2 and 6-3. All signals going on or off the chip require the use of an appropriate interface macro.

TABLE 2-4
I/O MACRO DOCUMENTATION INDEX

| Section | Interface Macro Type |
|---|---|
| 6-1 | TTL for 100% TTL<br>TTL for ECL/TTL with +5V |
| 6-2 | TTL for ECL/TTL,<br>dual power supplies |
| 6-3 | ECL, any |

For +5V only circuits, the TTL macros are selected from the TTL section, Section 6-1. For dual power supply circuits, the TTL macros are selected from the TTLMIX section, Section 6-2. The ECL macros are selected from the ECL section, Section 6-3. The same ECL macros are available for use with standard reference voltage or for +5V reference voltage circuits.

### TTL INPUT (ITxx macros)

Q14000 Series TTL input macros contain input buffers. TTL level detection is performed in this input macro. For circuits with a single +5V power supply, the buffer provides the signal buffering required to drive internal circuits. For dual power supply circuits, the buffer also provides signal translation from TTL input levels to the internal CMOS signal level needed by the array, which operates with a negative power supply.

## TTL OUTPUT (OTxx macros)

The Q14000 Series arrays provide 20mA current sink, 1mA current source capability. The TTL output is differentially driven by the buffered logic that is part of the TTL output macro.

The Q14000 Series arrays handle TTL totem-pole, open-collector and 3-stated output options. The 3-state output macro enable pin may be driven by any internal-level logic signal (the output of an input or internal logic macro). The signal driving the enable pin must be named on the schematic and must be listed in the simulation signal format.

## BIDIRECTIONAL TTL (UTxx macros)

The Q14000 Series I/O cell supports bidirectional I/O. The input and output functions follow the same design methodology as the ITxx and OTxx macros. The bidirectional macro enable pin may be driven by any internal-level logic signal (the output of an input or internal logic macro). The signal driving the enable pin must be named on the schematic and must be listed in the simulation signal format.

Bidirectional macros are placed in specifically designed I/O cells, limited to 20 on the Q2100B and 40 on the Q9100B arrays.

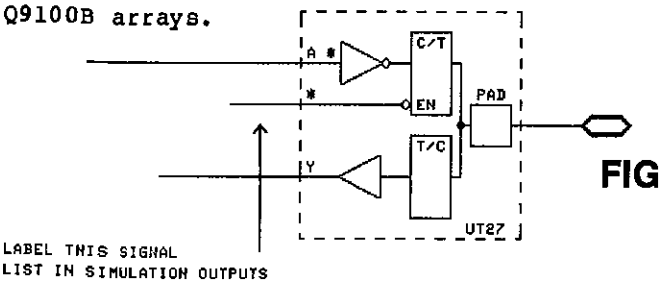



FIGURE 2-3

### ECL INPUT (IExx macros)

ECL input macros contain an RC compensation network and an input buffer. ECL inputs function in the same manner on circuits which have +5V referenced ECL input with a single +5V power supply.

### ECL OUTPUT (OExx, OKxx macros)

All ECL outputs require a buffer, and the buffer is included in the output macro. The Q14000 Series ECL output buffers drive 50 ohm ECL outputs.

ECL output macros are grouped by logic function in Section 6. A specific version of the macro (OExx or OKxx) is selected based on ECL type.

### SIMULTANEOUSLY SWITCHING MACROS

The inputs to an internal macro are considered to be switching simultaneously if they change within the macro propagation delay, i.e., one input changes while a previous input change is still propagating through the macro. For output macros, TTL outputs are considered to be simultaneously switching if they switch within 3ns of each other. ECL outputs are considered to be simultaneously switching if they switch within 2ns of each other.

TABLE 2-5
ECL MACRO SELECTION

| Q14000 Series | ECL 10K +5V REF | ECL 10K GND REF | ECL 100K +5V REF | ECL 100K GND REF |
|---|---|---|---|---|
| INPUTS | IExx | IExx | IExx | IExx |
| OUTPUTS | OExx | OExx | OKxx | OKxx |
| Bi-direc. | UExx | UExx | UKxx | UKxx |

BIDIRECTIONAL ECL (UExx, UKxx macros)

The Q14000 Series I/O cell supports bidirectional ECL I/O. The input and output functions follow the same design methodology as the IExx and OExx/OKxx macros. The macro enable pin may be driven by any internal-level logic signal (the output of an input or internal logic macro). The signal driving the enable pin must be named on the schematic and must be listed in the simulation signal format.

Bidirectional macros are placed in specifically designed I/O cells, limited to 20 on the Q2100B and 40 on the Q9100B arrays.

+5V REFERENCED ECL/TTL

AMCC offers the option of having ECL 10K or ECL 100K available with the use of a single +5V power supply. The ECL logic threshold levels are shifted, but retain their high-speed characteristics. This +5V referenced ECL mode allows the partitioning of a high-speed TTL design into multiple AMCC devices using a single +5V supply, while providing high-speed ECL I/O between the arrays on the same PC board and full system TTL compatibility.

## ALTERNATIVE ECL TERMINATIONS

The standard ECL termination is 50ohms tied to $V_{TT}$, where $V_{TT}$ = -2.0V for standard reference ECL. An alternative termination is 80ohms to ground with 130 ohms to $V_{EE}$ where $V_{EE}$ = -5.2V. For other termination configurations, consult AMCC.

## POWER BUSSES

The power busses supporting the internal array are isolated from the busses supporting the peripheral I/O cells to minimize the effect of noise coupling between the core and the I/O. The TTL and the ECL ground busses are kept isolated on the chip.

When necessary, there are macros available to provide extra TTL power (ITPWR), TTL ground (ITGND), and ECL power or ground (IEVCC), depending on the reference voltage.

## ADDING EXTRA TTL $V_{CC}$ - TTL GROUND PAIRS (ITPWR-ITGND)

As a design guideline for 100% TTL circuits and for mixed mode ECL/TTL circuits, the designer should allocate a minimum of one additional TTL $V_{CC}$ pad and one TTL GROUND pad to any quadrant of the chip that has more than eight (8) simultaneously switching TTL outputs.

An additional pair is required for each additional eight (8) simultaneously switching outputs in that same quadrant. (See Table 2-6.)

## ADDING EXTRA ECL IO VCC (IEVCC)

As a design guideline for any standard reference or +5V reference ECL circuit, the designer should allocate a minimum of one additional ECL VCC pad to any quadrant of the chip that has more than eight (8) simultaneously switching ECL outputs.

An additional ECL VCC (IEVCC) pad is required for each additional eight simultaneously switching ECL outputs in that same quadrant. (See Table 2-6.)

TABLE 2-6
ADDITIONAL POWER/GROUND
Q14000 SERIES

| # OF SIMULTANEOUSLY SWITCHING TTL OUTPUTS PER QUADRANT | ADD TTL $V_{CC}$ - TTL GROUND ADDED ITPWR - ITGND PAIRS |
|---|---|
| 0 - 8 | 0 |
| 9 - 16 | 1 ( 2 pads) |
| 17 - 24 | 2 ( 4 pads) |
| 25 - 32* | 3 ( 6 pads) |

| # OF SIMULTANEOUSLY SWITCHING ECL OUTPUTS PER QUADRANT | ADDED IEVCC |
|---|---|
| 1 - 8 | 0 |
| 9 - 16 | 1 ( 1 pad ) |
| 17 - 24 | 2 ( 2 pads) |
| 25 - 32 | 3 ( 3 pads) |
| 33 - 36* | 4 ( 4 pads) |

* There is a MAXIMUM of 40 I/O cells per quadrant in the largest array (the Q9100B). For this array, the SSO limit in a quadrant for TTL is 32 TTL SSO + 6 power-ground pairs. For this array, the SSO limit in a quadrant for ECL is 36 ECL SSO + 4 ECL VCC pads.

## SPECIFYING ADDITIONAL POWER AND GROUND

When additional power and ground pads are desired, the power macros, ITPWR or IEVCC, and the ground macros, IEVCC or ITGND, are placed on the schematic in the quantity desired. IEVCC will be considered a power pad for +5V REF ECL circuits and a GROUND pad for STD REF ECL circuits.

The added power and ground macros each occupy one I/O cell and use its pad. Added ground and power pads must be interspersed with the simultaneously switching signals.

Inclusion of the requirements for extra power and ground is part of the required design submission documentation.

## SWGROUP PARAMETER

When the added power and ground is for simultaneously switching circuits, use the macro parameter SWGROUP to tag these macros to the group to which they belong. The ERCs cannot issue error or warning messages on insufficient power or ground if the parameter is not used.

Note: The current AMCCERC algorithm is conservative when the number of simultaneously switching outputs exceeds what can be placed in a single quadrant of the array.

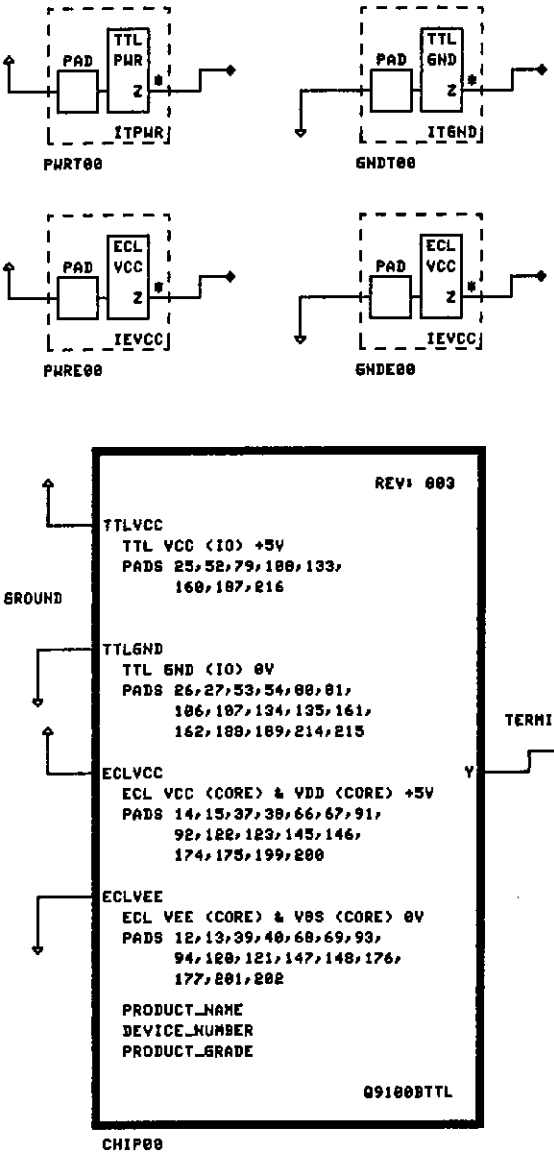
## CHARACTERIZING THE ARRAY - THE CHIP MACROS

The AMCC EWS schematic convention for the specification of the array and its I/O mode, power supply, product grade, and circuit identification (MILitary or COMmercial) is through the use of a CHIP MACRO. Note that the chip macro POWER_SUPPLY parameter allows the user to specify -5.2V, -4.5V or +5V for ECL circuits. The chip macros carry array-specific information used by AMCC MacroMatrix software in processing the design.

Refer to EWS Schematic Rules and Guidelines (Section 3 in Volume II) for placement and hook-up procedures. Volume I, Section 6-6 also documents the chip macros and their parameters.

The chip macros each carry the pads designated for use by the fixed power ($V_{CC}$) and ground ($V_{EE}$) pads required for that particular array and the specified I/O mode. Any power and ground pads added by the user are in addition to the fixed power and ground requirements.

Signals cannot be placed on the pads designated as being fixed power or ground pads. All fixed power and ground pads must be used. Fixed power and ground pads provide the minimum number of power and grounds for the array.




# CHIP-POWER/GROUND

# FIGURE 2-4

AMCCERC - POPULATION

- TOTAL ARRAY PADS

The AMCC MacroMatrix Population ERC check will correctly reflect the cell count and the total pad count for the design independent of the package selected. The population ERC will report this number as the number of "external pins" used by a circuit, the sum of all fixed power and ground, all added power and ground and all interface signals. The total pad count for the design is used in determining package selection. The final number of package pins may be less-than, equal-to or greater-than the total number of array pads used by the design.

TABLE 2-7
TOTAL PADS

| ARRAY | FIXED POWER-GROUND PADS | SIGNAL I/O PADS | TOTAL EXTERNAL PADS |
|---|---|---|---|
| Q9100B | 56 | 160 | 216 |
| Q2100B | 28 | 80 | 108 |

AMCCERC TECHNOLOGY CHECK

The AMCC MacroMatrix ERC technology ERC report will list errors due to improper selection of macros based on the I/O mode selected via the chip macro.

## INTERNAL FAN-OUT

Each internal macro output pin is specified to drive a maximum fan-out load. Maximum fan-out limits are specified for individual macros in the macro documentation in Section 6. The fan-out ERC checks for excessive fan-out loading.

## DERATING FAN-OUT LIMITS

For clock or distortion-sensitive paths, at speeds up to 100MHz, the maximum fan-out for each macro output pin in the path must be derated by 20%. For clock paths at speeds equal to or greater than 100MHz, the maximum fan-out should be derated by 40%. The fan-out ERC will check for a derated fan-out load limit if the FOD net parameter has been used. AMCC requires the use of the FOD parameter on all clock nets.

TABLE 2-8
DERATING GUIDELINE

| OPERATING SPEED: | DERATE BY: | FOD VALUE |
|---|---|---|
| < 100MHz | 20% | 20 |
| ≥ 100MHz | 40% | 40 |

## STATIC SIGNALS

When an internal macro has an unused pin or it is desired to tie an internal macro input pin to "1" or to "0", the pin is tied to global VSS ("0") or VDD ("1"), not to global GROUND.

When an output or bidirectional macro has an unused input pin, the pin is tied to global GROUND and not to VSS or VDD. Global GROUND is a logic zero. To tie one of these pins to logic "1", they must be driven by a macro.

VDD and VSS are connected to the internal VDD and VSS busses but are not counted in the internal pin count. Global GROUND is not connected to anything, i.e., it is allowed to float. It is not counted in the internal pin count.

To help the designer, the AMCC MacroMatrix ERC Hook-up check will detect global GROUND, VSS and VDD improper interconnect.

## INTERNAL CELL UTILIZATION

To insure routability, the recommended maximum internal cell utilization (cell population) for arrays in the Q14000 Series is 95%. Starting designs should target a 70% internal cell utilization to allow for the typical 20% design expansion during debug, re-design, enhancement, and testing logic additions. Designs in excess of 95% internal cell utilization for these arrays are considered risky if their internal pin count also exceeds recommended limits.

Compute internal cell utilization by first summing the number of L cells used by the circuit, and then by dividing that sum by the number of L cells available for the particular array.

TABLE 2-9
RECOMMENDED MAXIMUM
INTERNAL CELL UTILIZATION
L CELLS

| ARRAY | % |
|---|---|
| Q9100B | 95 |
| Q2100B | 95 |

AMCC MacroMatrix ERC software computes the internal cell utilization. The software generates an error if cell utilization exceeds recommended limits or exceeds 100%.

## INTERNAL PIN COUNT

The internal pin count is another measure of the routability of a circuit on a given array.

- Prior to schematic capture, the internal routable pin count should be estimated and used to determine the required array.

- After capture, the AMCC MacroMatrix ERC software provides a detailed report on the internal pin count of the circuit. For a captured circuit, refer to the limits in Table 2-10.

TABLE 2-10
MAXIMUM INTERNAL PIN COUNT
I/O AND L CELLS

| ARRAY | LIMIT |
|---|---|
| Q9100B | 8000 |
| Q2100B | 2200 |

- A circuit with an actual internal pin count that is less than the limit is routable.

- A circuit with an actual pin count that is 1-10% over the limit is considered risky (may have problems).

- A circuit with an actual pin count of 11-18% over the limit is considered very risky and may not successfully route.

- A circuit with an actual pin count of 18% or more over the limit is considered unroutable and a redesign is required if a larger array cannot be used.

## Q14000 SERIES BASIC DESIGN RULES AND GUIDELINES

Once the macros have been selected, and the basic circuit defined, the designer should review the circuit prior to submission to AMCC to verify that basic design rules have not been violated. Some of these rules and design checks are listed below.

Guidelines are suggestions to help ensure first-design success; rules are design requirements that cannot be violated. For further information, refer to the Design Submission and Design Validation documents, Section 6 and Section 5 of Volume II of this design manual.

- Fan-out - no macro drives more than its rating
- Fan-out derating - critical clock or distortion sensitive paths have derated clock loading: 20% up to 100MHz; 40% for $\geq$ 100MHz. Use the FOD parameter to allow ERC checking.
- Fan-out - no macro output pin is to drive more than one input pin of a gate within a macro. Driving multiple inputs of a gate from the same source results in loss of noise immunity.
- Fan-out - do not derate 3-state enable drivers.
- Fan-in - any macro with an asterisk on an input pin has been checked for fan-in > 1.
- Pin-restrictions - any macro with an asterisk has been cross-checked to be certain that it is connected to or driven from a legal macro connection.
- Unused macro input pins - INTERFACE MACROS EWS convention is to ground any unused inputs unless the macro documentation indicates that a pin cannot be grounded. (Grounded signals assume low level logic and physically float.)

- Unused macro input pins - INTERNAL MACROS
  EWS convention and design requirements dictate that unused internal macro input pins be tied to VDD or VSS.

- Pin connections - Make certain that input and output pins are properly connected, including PAD connections.

- Bidirectional signals - Be certain that bidirectional macro pins have been connected to a bidirectional connector (EWS convention). Refer to Volume II, Section 7 for additional information.

- Grounded output pins - These are not allowed.

- Terminated input pins - These are not allowed.

- Macro type - Check that the proper TTL I/O macros were chosen based on the circuit type.

- Macro type - Check that the proper ECL versions of the ECL macros were chosen based on the circuit type.

- Signal names - Check that all connections - intra-page, inter-page, off-chip and 3-state and bidirectional enables - have been properly named. Refer to Volume II, Section 3 for naming conventions and rules.

- Cell utilization - Do not violate the internal cell utilization limit without AMCC approval.

- Internal pin count - Do not exceed the array limit and supply AMCC with a total internal pin count.

- Additional power and ground - Provide additional power and ground pins as needed by using the ITPWR, ITGND and IEVCC macros on the schematic. Use the SWGROUP macro parameter to allow the simultaneously switching output ERC check.

- When leaded chip carriers are to be used, care should be taken to supply sufficient ground pins to allow separation of any signals where cross-talk may be of concern, e.g., between input and output signals. Spare pins should be grounded.

- Total PAD count - Do not exceed the maximum pad count limit for the array. ITGND, IEVCC, and ITPWR macros use cells and pads and are counted.

- Power - Compute the maximum worst case power. Combine the power dissipation of the interface macros with the power computed for the internal macros. Include any ECL static output power.

- Packaging - Verify that the package selected is appropriate for the environment and junction temperature (compute based on power).

- Critical paths - Compute and clearly identify the critical paths.

- Generate and include reports on macro occurrence, current and power; fan-out; pin count; etc. as indicated in the Design Submission and Design Validation documents. (AMCC MacroMatrix ERC software generates most of these reports.) Refer to Section 8, Volume II.

- Use a chip macro to characterize the circuit as to array, ECL type and power supply. Follow the rules in AMCC EWS Schematic Rules and Conventions. Refer to Section 3, Volume II.

- Complete simulation documentation must be submitted with the design, including source files. Refer to the Design Submission and Design Validation documents.

- For guidance in constructing simulation vectors, refer to the AMCC document:
  Vector Submission Rules and Guidelines.
  Refer to Section 4, Volume II.

## POWER BUS DISTRIBUTION AND DECOUPLING

Optimal Power Bus Distribution and Decoupling is dependent on a number of interactive device and system variables, including the package design used, the number of simultaneous switching outputs on the device, output loading, the amount of switching noise contributed by other system components, the number of power busses and the design of the system and module power distribution.

AMCC recommends the use of multi-layer PC boards that provide dedicated low impedence power and ground planes. Besides maintaining a constant characteristic impedence for transmission lines, the planes provide for a low impedence return path to the ECL or TTL circuitry and act as an electromagnetic shield for the signal lines. The distributed capacitance will also improve noise margins by minimizing "ground bounce" and crosstalk.

The 2-layer PC boards, on the other hand, may require successive approximations to optimize the system noise margins and reduce external noise from being fed back into the chip through the power and ground pins. This approach should only be attempted in lower performance systems.

The I/O ECL $V_{CC}$ and the Internal $V_{CC}$ package pins should be tied together as close to the chip as possible, using good high frequency practices. When mixed I/O is combined with multiple power busses, the TTL GND and ECL $V_{CC}$ (0V) can be tied directly together at the chip on multi-layer boards.

For 2-sided boards, the location will be system dependent and may require some experimentation. The primary considerations are the amount of simultaneous switching, the signal/ground pin ratio and the isolation between the TTL and ECL signal lines (and return paths).

Low frequency (bulk) decoupling is generally provided in the range of 0.5 to 2.0 uf/WATT, while high frequency by-passing should be 100 to 1,000 pF/quadrant. The by-pass capacitors are generally placed as close to the chip as possible using high frequency techniques to minimize the inductance in the leads, traces, feed-throughs and components.

The AMCC Q14000 performance boards use a 1uf tantalum capacitor in parallel with a 470pf ceramic chip capacitor for each of the Internal $V_{EE}/V_{CC}$ pairs. This same combination is used for any $V_{CC}$ or additional $V_{CC}$ package pins with excellent results.

## TESTABILITY

Concepts of testing and testability must be considered from the beginning of any circuit design. AMCC encourages: (1) the use of testability techniques in circuit design; (2) the use of testability analysis early in the design process so that testability problems can be corrected by design; (3) the use of fault grading to assess test vector fault coverage; and (4) an understanding of the capabilities of today's advanced test equipment in the development of semi-custom circuits.

## STRUCTURED DESIGN

Structured approaches to ensure circuit testability such as LSSD, Scan Path and BILBO are generally driven by an overall system philosophy to testing. While AMCC does not promote one structured technique over another, other measures during design can improve circuit testability. AMCC does promote the use of overall structured design procedures, including functional modularity, bus architectures and clear documentation.

## TESTABILITY ANALYSIS

All testability measures have one common goal: to enhance controllability and observability of the circuit. It is a grade on the logic design itself. Controllability is a measure of the ease in setting a particular node to a logic level of zero or one, while observability determines the ease of propagating the node's state to one or more primary outputs.

After a netlist has been created and logic simulation has verified correct functional performance, testability can be verified by running testability analysis programs such as DTA (DAISY) or COPTR (TEGAS).

## FUNCTIONAL SIMULATION

The object of functional testing is to detect a single SA1 or SA0 fault in the circuit if one exists. This ideally requires sufficient vectors to "cover" all possible fault locations. The percent of coverage is the fault grade of the vector set. To this end, one approach is to cycle all inputs and outputs through 1-0 and 0-1 transitions as a first check after initialization. (This should cycle all internal nodes as well.) This $2^n$ (n = number of inputs) brute force approach is not necessary. Minimum vector test sets and minimum vector test sequences will cover 100% of all observable faults.

Functional simulation vector fault-grading can be performed using the TEGAS simulator. Fault-grading is used to verify that the simulation bit vectors sufficiently exercise nodes within the circuit to assure that the outgoing product matches the customer specification. Insufficient fault coverage as determined in a fault grading run may require the addition of vectors to the set developed to evaluate logical functionality.

AMCC recommends the creation of a sufficient number of vectors to achieve a fault coverage of 90% or higher, and is prepared to perform the fault grading task upon request.

For guidelines in performing functional simulation, refer to Vector Submission Rules and Guidelines in Section 4, Volume II of this design manual.

AMCCVRC Vector Rules Checker must be run against the AMCCSIMFMT (AMCC Simulation Format) maximum worst-case sampled simulation output file.

AT-SPEED SIMULATION

In addition to functional simulation, the customer must perform an at-speed simulation and timing analysis for all critical (i.e., timing-sensitive) paths in the circuit. Refer to the above referenced document.

AC TESTS SIMULATION

AC path propagation delay tests require simulation vectors to initialize the circuit path to be measured and to support the measurement of the path. Provided the start and stop addresses are clearly documented, all AC tests may be grouped in one simulation file. Each AC test path must be clearly documented. A test path is defined as a single input to a single output. Refer to (708 REV A) of the previously referenced document.

If the path propagation delay to be measured is less than 10ns typical, consult AMCC.

## DESIGN FOR TESTABILITY

Some specific design suggestions for improved circuit testability are:

- Become familiar with the macro library BEFORE beginning the macro conversion or design.
- Use synchronous rather than asynchronous circuits whenever possible - functional tests are synchronous.
- Partition the design (use structured design techniques) into smaller, testable sections, usually along a functional boundary.
    - Use degating logic to isolate modules for test.
    - Use modular architecture, bus structures.
    - Break up long counters (>8).
- Don't bury states.
- Use transparent latches instead of flip/flops where possible and use I/O latches instead of flip/flops.
- Use macros, especially flips/flops and latches, with RESET or SET controls where possible to simplify initialization.
- Avoid feedback loops.
    - If unavoidable, provide a means to break up feedback loops during test (degating, enables).
- Avoid redundant logic - minimize! - or add test points to unmask masked faults.
- Avoid derived clocks - they complicate testing.
- Design in test points, especially in sequential logic. Add test points to improve controllability and observability. Perform testability analysis.
- If I/O pins are limited, use demultiplexors to control and multiplexors to observe internal nodes with otherwise poor observability (buried states).

- Any 3-state enable control signal that is internally generated must be externally observable, and should be externally controllable during test.
- Add parity trees for error detection. Or use Scan Path Design to simplify test sequence generation or use Level Sensitive Scan Design to simplify test sequence generation. Keep test generation in mind while designing the circuit.

## DESIGN FOR RELIABILITY

Some specific design suggestions for improved circuit reliability are:

- Become familiar with the macro library BEFORE beginning the macro conversion or design.
- Be aware of "glitch" circuits. Do not use potential glitch circuits to drive clock inputs.
- Avoid one-shot pulse generators.
- Avoid gated and derived clocks.
- Avoid race and hazard conditions. (PRINT_ON_CHANGE files can help identify these.) These are generated by having a signal follow two or more paths to a common circuit element (a.k.a. reconvergent fan-out.)
- Avoid feedback loops.
    - If unavoidable, provide a means to break up feedback loops during test (using degating, enables).
- Avoid feedback paths between registers. If present, compute the worst-case set-up and hold times and verify operation. (Feedback from the ECL output macros must be handled with care if used to input to internal latches and flip/flops.)
- Add sufficient GROUND for the number of simultaneously switching outputs and distribute among these outputs (similar to distributed ground in a ribbon cable). Add additional extra ground if there are extra I/O pins available.
- Add extra $V_{CC}$ as needed for the number of simultaneously switching outputs.
- Properly derate fan-out on all distortion-sensitive paths and all clock paths. Keep clock path loading balanced.

# Section 3:

# Timing Analysis

## COMPUTING PROPAGATION DELAY

The macros selected, the options of those macros, the loading on the macros, and the final layout of the circuit are all factors in the propagation delay of any path. The loading may be the interconnect capacitance or the external load capacitance due to system loading and package pin capacitance.

There are two approaches that can be used to compute propagation delay: Front-Annotation, where a statistical estimate of metal delays based on net sizes is used; and Back-Annotation, where the actual metal delay is used in the computation.

- PRELIMINARY COMPUTATION - PRIOR TO CAPTURE

The path propagation delays can be estimated using the statistical wire delay tables ($L_{net}$), fan-out loading ($L_{fo}$) and the appropriate k-factors (k) for the macros chosen. The equation for the typical extrinsic (load) delay for a single net is shown below and discussed in detail on the following pages.

$$t_{ex} = k * ( L_{fo} + L_{net} )$$

The sum of all typical intrinsic macro delays in the path ($t_{in}$; specified as Tpd in the macro documentation) and all extrinsic loading ($t_{ex}$) is then multiplied by the proper ANNOTATED worst-case timing multiplication factor.

- FRONT-ANNOTATION - AFTER CAPTURE

After schematic capture, Front-Annotation software is available to provide the designer with a file of rising and falling edge delays per net (expressed as NOM, MIN and MAX). By incorporating this file into the simulation database, the designer can obtain a statistical estimate of circuit performance.

- BACK-ANNOTATION - AFTER LAYOUT

The most accurate method of computing a circuit propagation delay requires that the circuit be completed through layout. Back-annotation software adds the actual metal delay and fan-out delays into the path. Back-annotation must be run and accepted as final prior to the generation of the actual silicon arrays. The Back-Annotation program provides a file which includes the ACTUAL metal delays in a net.

AMCC guarantees that the silicon will match (will not be slower than) the results of the Back-Annotation.

- TYPICAL INDIVIDUAL MACRO PROPAGATION DELAY

AMCC macro documentation specifies typical, unloaded macro path propagation delays (Tpd) for each path through a macro. Some macro specifications include a different delay for a rising edge (Tpd-+) than for a falling edge (Tpd+-). Three-state macros have specifications for high-Z representative switching delays $T_{PHZ}$, $T_{PZH}$, $T_{PZL}$ and $T_{PLZ}$.

The actual macro path delay will be a function of: state of the input data (low data may have different set-up and hold times than high data); multiple inputs changing state (e.g., when several OR/NOR inputs change simultaneously on an internal macro, the delay increases).

To account for some of these path delay variations, the AMCC macro specifications have been expanded to show the model behavior in more detail. The specifications are interpreted as follows:

Non-inverting:
- Tpd++ rising edge input; rising edge output
- Tpd-- falling edge input; falling edge output

Inverting:
- Tpd+- rising edge input; falling edge output
- Tpd-+ falling edge input; rising edge output

All AMCC EWS simulation models are accurate to within 10ps (two decimal place accuracy when measured in ns).

AMCC macro specifications, as documented in the Design Guides and Design Manuals for the individual array series, show the typical propagation delay for a path through a macro for nearly all of the possible conditions. Multiplexer specifications are simplified.

- INTRINSIC SET-UP AND HOLD TIMES

The intrinsic set-up and hold times for the latches, flip/flops and MSI macros that include one or more of these types of devices, are specified in the macro summary in Section 6. The parameters represent the behavior of the macro as observed at its input and output nodes. Set-up time (Tsu) is the time that a signal must be stable prior to the active clock edge. Hold time (Th) is the time that a signal must be held after the active clock edge.

- RECOVERY TIME

Recovery time (Trec) is specified for any latch or flop/flop which has a set or reset. It is the length of time that a reset/set signal has to have been inactive prior to an active clock edge. Clocking within the recovery time period will result in unpredictable behavior.

Note: Set-up time, hold time, recovery time and minimum pulse width are all specified as typical values and must be multiplied by the appropriate worst-case delay multiplication factor.

• EFFECT OF LOADING ON OUTPUT MACRO DELAYS

For output macros, Tpd is specified for a no load. The actual capacitive load driven will be the sum of the system load and the package pin capacitance. The capacitive load is converted to ns using the constants in Table 3-1. For TTL or ECL output loads up to but less than 100pf, use Table 3-1. For TTL or ECL output loads over 100pf, consult AMCC.

TABLE 3-1
OUTPUT LOADING DELAYS
CAPACITIVE LOADING

| | |
|---|---|
| TTL | 55ps/pf |
| ECL | 45ps/pf |

$$Td_{TTL\ LOAD} = \frac{[(\text{system C load}) + (\text{package pin C})] * 55ps/pf}{1000}$$

$$Td_{ECL\ LOAD} = \frac{[(\text{system C load}) + (\text{package pin C})] * 45ps/pf}{1000}$$

The delay adjustment values for both TTL and ECL output capacitive loading are typical and must be multiplied by the worst-case multiplier for the selected operating conditions, therefore, at this step, the nominal case capacitive load delay should be added to the nominal path propagation delay.

- COMPUTING THE LOADING DELAY FOR A NET
  - FRONT ANNOTATION

The method for manual computation of the effect of load units on the propagation path is:

For each net:

$$t_{ex} = k * (L_{fo} + L_{net})$$

where k = the k factor for the series and the macro option as listed in Section 6. An overview of k-factors is listed in Table 3-2.

$L_{fo}$ = the sum of the electrical fan-out loads in a net. (Pins with a fan-in of 2 count as 2 electrical loads)

$L_{net}$ = the estimated metal delay from Table 3-3, indexed by the sum of the number of pins in the net minus 1 (i.e., index by [net size - 1]) (Pins with a fan-in of 2 count as 1 physical load)

TABLE 3-2
TYPICAL k FACTORS - Q14000 *

| | | ns/LU |
|---|---|---|
| INTERNAL MACROS: | | |
| $k_{up}$ | S-option | 0.025 - 0.045 |
| $k_{down}$ | S-option | 0.025 - 0.045 |
| INTERFACE (I/O) MACROS: | | |
| $k_{up}$ | S-option | 0.025 |
| $k_{down}$ | S-option | 0.030 |
| $k_{up}$ | H-option | 0.025 |
| $k_{down}$ | H-option | 0.030 |

* Refer to Section 6 for the k-factors for a specific macro.

• COMPUTING $L_{net}$

Compute the statistical metal estimate by counting the physical pins in the net (driving or source pins and destination pins), subtracting one (1), and using this number as the index to the following table. The number listed under a specific array is the estimate for the load units due to metal in the net.

TABLE 3-3
FRONT-ANNOTATION
Q14000 SERIES
STATISTICAL WIRE LOADS
$L_{net}$

| INDEX 1-30 | | | INDEX 31-60 | | |
|---|---|---|---|---|---|
| PINS -1 | Q2100B | Q9100B | PINS -1 | Q2100B | Q9100B |
| 1 | 1.00 | 1.18 | 31 | 9.64 | 25.95 |
| 2 | 1.58 | 2.20 | 32 | 9.85 | 26.70 |
| 3 | 2.06 | 3.17 | 33 | 10.05 | 27.45 |
| 4 | 2.50 | 4.11 | 34 | 10.25 | 28.20 |
| 5 | 2.89 | 5.02 | 35 | 10.45 | 28.94 |
| 6 | 3.26 | 5.92 | 36 | 10.65 | 29.69 |
| 7 | 3.61 | 6.80 | 37 | 10.84 | 30.43 |
| 8 | 3.94 | 7.67 | 38 | 11.03 | 31.17 |
| 9 | 4.26 | 8.53 | 39 | 11.22 | 31.90 |
| 10 | 4.57 | 9.37 | 40 | 11.41 | 32.64 |
| 11 | 4.87 | 10.21 | 41 | 11.60 | 33.37 |
| 12 | 5.16 | 11.04 | 42 | 11.79 | 34.10 |
| 13 | 5.44 | 11.87 | 43 | 11.97 | 34.83 |
| 14 | 5.71 | 12.69 | 44 | 12.15 | 35.56 |
| 15 | 5.97 | 13.50 | 45 | 12.33 | 36.29 |
| 16 | 6.23 | 14.31 | 46 | 12.51 | 37.01 |
| 17 | 6.49 | 15.11 | 47 | 12.69 | 37.74 |
| 18 | 6.74 | 15.91 | 48 | 12.87 | 38.46 |
| 19 | 6.98 | 16.70 | 49 | 13.05 | 39.18 |
| 20 | 7.22 | 17.49 | 50 | 13.22 | 39.90 |
| 21 | 7.46 | 18.28 | 51 | 13.40 | 40.62 |
| 22 | 7.69 | 19.06 | 52 | 13.57 | 41.33 |
| 23 | 7.92 | 19.84 | 53 | 13.74 | 42.05 |
| 24 | 8.15 | 20.61 | 54 | 13.91 | 42.76 |
| 25 | 8.37 | 21.38 | 55 | 14.08 | 43.47 |
| 26 | 8.59 | 22.15 | 56 | 14.25 | 44.18 |
| 27 | 8.80 | 22.91 | 57 | 14.42 | 44.89 |
| 28 | 9.02 | 23.68 | 58 | 14.58 | 45.60 |
| 29 | 9.23 | 24.44 | 59 | 14.75 | 46.01 |
| 30 | 9.44 | 25.19 | 60 | 14.91 | 47.01 |

• COMPUTING $L_{fo}$

Compute $L_{fo}$ by adding the sum of the electrical load of all loads driven. If a destination pin has a fan-in of 2, it counts as two electrical loads and as one physical pin. A destination may appear to have two physical loads internal to the macro. In these cases, the macro documentation will clearly identify the fan-in load represented by that pin. Physical fan-out internal to the macro does not affect the physical pin count.

WORST-CASE DELAY MULTIPLICATION FACTORS

Once the sum of all of the intrinsic and extrinsic propagation delays in a path or path segment is computed and adjusted for any external high-capacitive loading (system load and package pin capacitance), then the result must be multiplied to obtain the worst-case delay as follows:

$$Tpd_{typical} * M.F. = Tpd_{worst\text{-}case}$$

Multiplication factors are shown in Table 3-4. The worst-case multipliers take into account the following:

- Process variations
- Temperature variations
- Voltage variations
- Signal skew

TABLE 3-4
WORST-CASE DELAY MULTIPLICATION FACTORS
WORST-CASE MULTIPLIERS FOR FRONT- AND BACK-ANNOTATION
WCM

| | | INTERFACE | INTERNAL |
|---|---|---|---|
| MINIMUM | min. | 0.70 | 0.70 |
| | typ. | 0.78 | 0.78 |
| | max. | 0.86 | 0.86 |
| NOMINAL | min. | 0.90 | 0.90 |
| | typ. | 1.00 | 1.00 |
| | max. | 1.10 | 1.10 |
| COMMERCIAL** | min. | 1.11 | 1.27 |
| | typ. | 1.23 | 1.41 |
| | max. | 1.35 | 1.55 |
| MILITARY*** | min. | 1.19 | 1.59 |
| | typ. | 1.32 | 1.77 |
| | max. | 1.45 | 1.95 |

** $T_j \leq 130^{\circ}$
*** $T_j \leq 150^{\circ}$

TABLE 3-5
APPLICATION RULES FOR THE WORST-CASE DELAY MULTIPLIER

- Set-up time, hold time, recovery time and minimum pulse width are multiplied by a worst-case delay multiplier.

- Macro intrinsic delays and extrinsic delays are multiplied by the worst-case delay multipliers.

- The worst-case multipliers used for the extrinsic net delays should be consistent with the macro type of the macro driving the net, i.e., nets driven by the input macros shoud use the interface macro worst-case delay multiplier.

- The worst-case delay multiplier for the extrinsic delay caused by output load capacitance is the interface macro worst-case delay multiplier.

- Delay multipliers at a given operating condition represent 20% on-chip signal tracking.

## SELECTING THE CORRECT WORST-CASE DELAY MULTIPLIER

Commercial worst-case timing multipliers are for circuits operating in the 0°C ambient to 70°C ambient temperature range with a ±5% power supply variation and a junction temperature maintained at ≤130°C. Violation of any of these three parameters requires the use of the Military timing multipliers.

Military worst-case timing multipliers are for circuits operating in the -55°C ambient to +125°C case temperature range with a ±10% power supply variation and a junction temperature maintained at ≤150°C. If any of these parameters are violated, the military timing multipliers will no longer apply. Consult AMCC.

## MINIMUM PROPAGATION DELAY

AMCC does not specify minimum circuit delays. However, a guideline for minimum propagation delay is 70% of the typical path delay (the annotated worst-case minimum multiplier is 0.70). Note that both the interface and the internal macros use the same worst-case minimum multiplier.

Where the performance of a circuit would be affected by excessive speed in an array, the minimum performance requirements must be clearly documented in the design submission.

• RESULT

The interface macros, both input and output, use a different worst-case delay multiplier than the internal macros. The nets driven by interface macros use the interface macro worst-case delay multiplier. The nets driven by the internal macros use the internal macro worst-case delay multiplier.

To find path propagation delay, first add the intrinsic and extrinsic delays of the input and output macros for the path and multiply the sum by the correct interface worst-case delay multiplier. The extrinsic delay for an output macro is the delay caused by the system capacitive load and the package pin capacitance.

Second, total the intrinsic and extrinsic delays for all internal macros in the path and multiply the sum by the proper internal worst-case delay multiplication factor. Sum this result with the one found for the interface macros to find the total path propagation delay.

ASYMMETRY IN THE WORST-CASE PATH

Each potentially critical path must be evaluated for worst-case conditions. Both the propagation delay of a rising edge input signal and that of a falling edge input signal must be computed and compared for pulse stretch and pulse shrink. For multiple-input macros, the worst-case specification may be with one or more inputs switching or not. The worst potential circuit behavior represented by the macro specifications must be reviewed.

Minimum pulse-width requirements must be verified and the minimum path delay adjusted as necessary to meet these requirements.

In some cases the minimum delay may be the worst case. AMCC MacroMatrix releases contain the NOMINAL, MAXIMUM-MILITARY, MAXIMUM-COMMERCIAL and MINIMUM timing libraries for the array series.

AMCC design submission requirements include the simulation of the circuit for both the maximum worst-case (MIL or COM) and the minimum worst-case for functional, at-speed and AC test simulations.

It is up to the designer to provide siulation vectors that will exercise the correct worst-case conditions for the macros in the critical path, whether it is for one input on a macro switching and the others remaining constant or for multiple simultaneously-switching inputs on a macro.

If there is a difference in the functional or AC test simulation results between the maximum and the minimum worst-case timing, hazard and race conditions are indicated and must be evaluated.

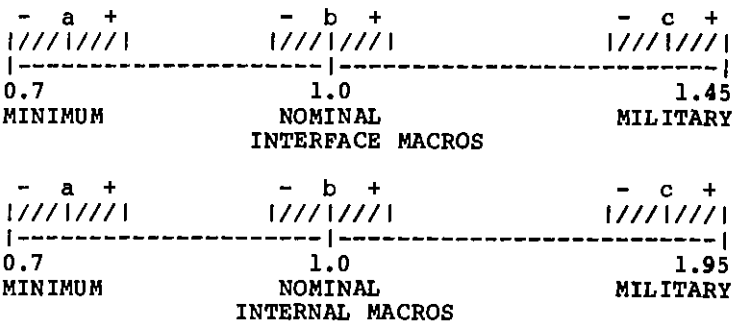
## INTERNAL SIGNAL TRACKING

Many factors affect the signal delay tracking within the array. These factors include such things as relative position within the device, process variations, power supply variations, operating temperature and the characteristics of the various macros.

In BiCMOS, for interface macros, a "like structure" is defined as a similar macro type with the same option and fan-out load limits. For internal macros on Basic cells, the macros must actually be identical to be considered a "like structure".

- For like structures, for the same edge (both rising or both falling), and with placement on adjacent rows or cells within a quadrant, the tracking will be ±2.5%.
- For like structures, for the same edge (both rising or both falling), and with a random placement, the tracking will be ±5%.
- For unlike structures, for the same edge (both rising and falling), and with a random placement, the tracking will be ±10%. (See Table 3-4.)

EXAMPLE OF TRACKING FOR THREE OPERATING CONDITIONS:




From the diagram, for unlike structures, 1.1 * c = 1.45 for an interface macro, 1.1 * c = 1.95 for an internal macro.

## SIGNAL BALANCING; DISTORTION MINIMIZATION

The case where two paths are required to be identical in performance is common. The best results are obtained when the macros are identical macros and are identically loaded, including wire load. Since placement cannot be assumed to be able to solve all problems in all cases, the judicious use of parallel structures (such as buffer trees) to reduce loading in a path and the use of pulse distortion minimization techniques, such as inversion of the signal at each macro, will help.

For ECL output operation at 100MHz and above, pulse distortion minimization methods should be used. These include: 1) signal inversion on alternating macros; 2) short interconnect, a function of fan-out and metal length; and 3) balanced rising-edge and falling-edge k-factors.

The final anaylsis for pulse stretch and shrink and balanced path delays must be performed using Back-Annotation.

## MAXIMUM OPERATING FREQUENCY

The Q14000 Series is capable of supporting high I/O switching rates. The following is a summary of I/O and internal logic performance capabilities:

TABLE 3-6
MAXIMUM OPERATING FREQUENCY
PULSE WIDTH GUIDELINES
Q14000 SERIES BiCMOS ARRAYS

| TYPE OF I/O: | COM MHz | COM PW-ns | MIL MHz | MIL PW-ns |
|---|---|---|---|---|
| TTL INPUT - S-OPTION | 65 | 7.69 | 60 | 8.33 |
| - H-OPTION | 90 | 5.55 | 85 | 5.88 |
| TTL OUTPUT - S-OPTION | 50 | 10.00 | 45 | 11.11 |
| - H-OPTION | 65 | 7.69 | 60 | 8.33 |
| ECL INPUT - S-OPTION | 110 | 4.54 | 100 | 5.00 |
| - H-OPTION | 180 | 2.77 | 165 | 3.02 |
| ECL OUTPUT - S-OPTION | 110 | 4.54 | 100 | 5.00 |
| - H-OPTION | 180 | 2.77 | 165 | 3.02 |
| INTERNAL MACRO - F/F FAST | 180* | 2.40 | 165 | 3.02 |
| - F/F SLOW | 174 | 2.86 | 138 | 3.62 |
| - OTHER ** | 165 | 3.02 | 130 | 3.84 |

* limited by maximum driver frequency

**Gate macros GT01, GT02, GT03, GT11, GT12, GT33, GT44, and GT47 have a maximum frequency of 65MHz MILITARY and 82MHz COMMERCIAL. Their pulse width requirements are 3.93ns TYPICAL, 6.09ns COMMERCIAL and 7.66ns MILITARY. For faster versions of these macros please consult AMCC.

Flip/flop, latch, counter and shift register documentation includes typical pulse width specifications. Pulse width is computed based on a 50% duty cycle. Selected MSI macros (those with flip/flops or latches with feedback paths) also carry specifications for maximum operating frequency.

To achieve the maximum toggle frequency for the fast flip/flops, they must be directly driven by ECL interface macros. There is no timing error generated by the timing analysis programs on the EWS simulators when a macro is driven faster than it is specified to run.

## FRONT-ANNOTATION LOAD UNITS

The Front-Annotation statistical wire load unit table was calculated using the following:

$$LU = a * \left( \frac{\text{fan-out}}{\text{loads}} \right)^{**b}$$

TABLE 3-7
FRONT-ANNOTATION LOAD UNITS

| | Q2100B | Q9100B |
|---|---|---|
| a | 1.00 | 1.18 |
| b | 0.66 | 0.90 |

## BACK-ANNOTATION LOAD UNITS

The Back-Annotation delay file is derived using the following:

TABLE 3-8
BACK-ANNOTATION DELAY MULTIPLIERS

| | | |
|---|---|---|
| first layer metal | 1.20 | LU/mm |
| second layer metal | 3.00 | LU/mm |

# Section 4:

# External Tsu, Th

## EXTERNAL SET-UP and HOLD TIMES

When the input to the data or the clock or both pins on a flip/flop or a latch are supplied from an external signal, then the external set-up and hold times must be computed. The computations must be for worst-case and account for processing skew.

To meet design submission requirements, both the maximum worst-case (1.45 and 1.95 or 1.35 and 1.55) and the minimum worst-case (0.70) equations may need to be computed to determine the worst-case window for external set-up and hold times. Both rising edge input and falling edge input path propagation must be evaluated.

Use the MILITARY or COMMERCIAL equations for set-up time when $t_D + t_{Dinput} - 0.82 * (t_C + t_{Cinput}) \geq 0$. Use the MINIMUM equations for set-up time when $t_D + t_{Dinput} - 0.82 * (t_C + t_{Cinput}) < 0$.

Use the MILITARY or COMMERCIAL equations for hold time when $t_C + t_{Cinput} - 0.82 * (t_D + t_{Dinput}) \geq 0$. Use the MINIMUM equations for hold time when $t_C + t_{Cinput} - 0.82 * (t_D + t_{Dinput}) < 0$.

Results computed or derived from simulations using Front-Annotation data cannot be considered as the circuit specification.

When computing the set-up time, it is desirable to assume that the data propagation path delay is the worst-case maximum and that the clock path propagation delay is a worst-case minimum for the operating conditions. The generic equation is:

$$t_{su_{external}} = WCMmax * (t_D + Tsu_{macro}) - WCMmin * t_C$$

For the Q14000 Series and its dual multipliers, the equation becomes:

$$t_{su_{external}} = WCMmax_{interface} * t_{Dinput} + WMCmax_{core} * t_D - WCMmin_{interface} * t_{Cinput} - WCMmin_{core} * t_C + WCMmax_{core} * T_{su(macro)}$$

When computing the hold time, it is desirable to assume that the data propagation path delay is the worst-case minimum and that the clock path propagation delay is a worst-case maximum for the operating conditions. The generic equation is:

$$t_{h_{external}} = WCMmax * (t_C + Th_{macro}) - WCMmin * t_D$$

For the Q14000 Series and its dual multipliers, the equation becomes:

$$t_{h_{external}} = WCMmax_{interface} * t_{Cinput} + WMCmax_{core} * t_C - WCMmin_{interface} * t_{Dinput} - WCMmin_{core} * t_D + WCMmax_{core} * T_{h(macro)}$$

The equations are based on the 20% variation in on-chip signal tracking discussed earlier in this design manual.

Table 4-1 provides the external set-up and hold equations for the Q14000 BiCMOS Series Arrays for the four defined operating conditions. Figure 4-1 illustrates the delay paths. Table 4-2 provides the definitions for the terms used in the text, the equations and in the figure.

TABLE 4-2
TERMINOLOGY DEFINITIONS

Defining a "memory macro" as a latch, a flip/flop or an MSI containing one or the other, the terms used in the equations are defined in Table 4-2.

$t_D$ = NOMINAL data path propagation delay from the circuit input and up to the memory macro data input pin; EXCLUDING the interface macro intrinsic delay and the extrinsic net delay for the net driven by the interface macro, computed using Front Annotation methodology prior to layout, Back Annotation after layout.

$t_{Dinput}$ = NOMINAL delay due to interface macro intrinsic delay on data path plus the extrinsic net delay for the net driven by the interface macro, computed using Front Annotation methodology prior to layout, Back Annotation after layout.

$t_C$ = NOMINAL clock path propagation delay from the circuit input and up to the memory macro clock input pin; EXCLUDING the interface macro intrinsic delay and the extrinsic net delay for the net driven by the interface macro, computed using Front-Annotation methodology prior to layout, Back-Annotation after layout.

$t_{Cinput}$ = NOMINAL delay due to interface macro intrinsic delay on clock path plus the extrinsic net delay for the net driven by the interface macro, computed using Front Annotation methodology prior to layout, Back Annotation after layout.

$Tsu_{macro}$ = Tsu as specified in Section 6 (specified as typical)

$Th_{macro}$ = Th as specified in Section 6 (specified as typical)

The specific worst-case multipliers (WCMmax and WCMmin) are based on the operating conditions and the type of macro involved. The bipolar interface macros use one multiplier and the CMOS core uses another.

WCMmax = MILmax, COMmax or MINmax
WCMmin = MILmin, COMmin or MINmin — See Table 4-3

TABLE 4-1
SET-UP AND HOLD EQUATIONS - BiCMOS Q14000 SERIES ARRAYS

| | | |
|---|---|---|
| MILITARY OPERATING RANGE | $t_{su_{external}}$ | $= 1.45 * t_{Dinput} + 1.95 * t_D - 1.19 * t_{Cinput} - 1.59 * t_C + 1.95 * T_{su(macro)}$ |
| | $t_{h_{external}}$ | $= 1.45 * t_{Cinput} + 1.95 * t_C - 1.19 * t_{Dinput} - 1.59 * t_D + 1.95 * T_{h(macro)}$ |
| COMMERCIAL OPERATING RANGE | $t_{su_{external}}$ | $= 1.35 * t_{Dinput} + 1.55 * t_D - 1.11 * t_{Cinput} - 1.27 * t_C + 1.55 * T_{su(macro)}$ |
| | $t_{h_{external}}$ | $= 1.35 * t_{Cinput} + 1.55 * t_C - 1.11 * t_{Dinput} - 1.27 * t_D + 1.55 * T_{h(macro)}$ |
| MINIMUM OPERATING RANGE | $t_{su_{external}}$ | $= 0.86 * (t_D + t_{Dinput}) - 0.70 * (t_C + t_{Cinput}) + 0.86 * T_{su(macro)}$ |
| | $t_{h_{external}}$ | $= 0.86 * (t_C + t_{Cinput}) - 0.70 * (t_D + t_{Dinput}) + 0.86 * T_{h(macro)}$ |

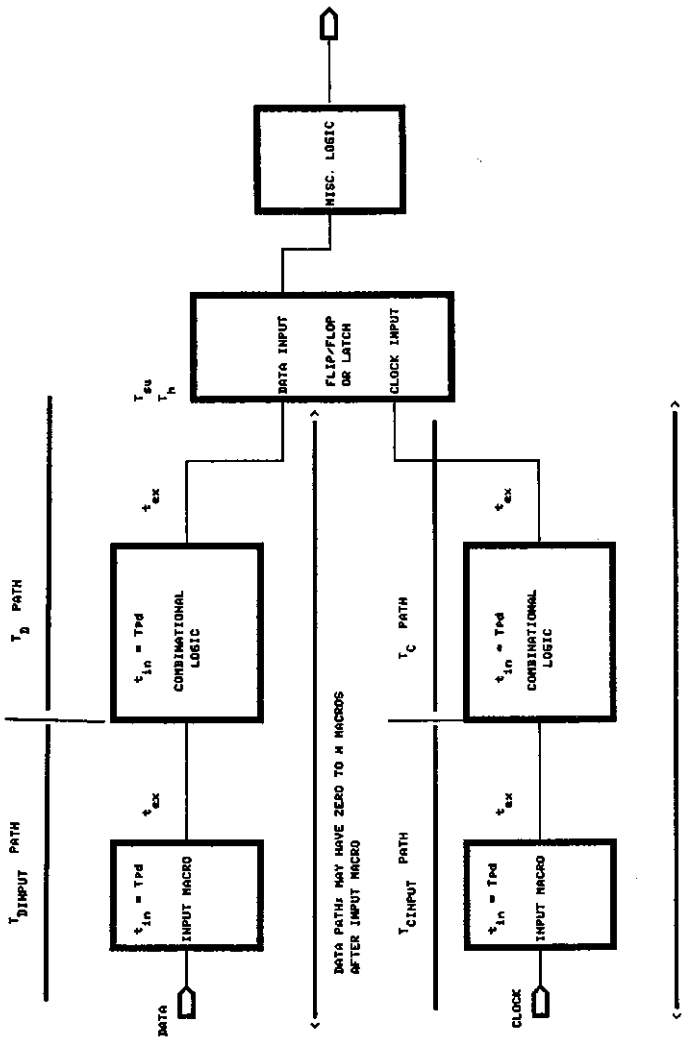

MISC. LOGIC
DATA INPUT
FLIP-FLOP OR LATCH
CLOCK INPUT
$T_{su}$
$T_h$
$T_D$ PATH
$T_{DINPUT}$ PATH
$t_{ex}$
$t_{in}$ = Tpd
COMBINATIONAL LOGIC
INPUT MACRO
DATA
DATA PATHS MAY HAVE ZERO TO N MACROS AFTER INPUT MACRO
$T_C$ PATH
$T_{CINPUT}$ PATH
CLOCK
CLOCK PATHS MAY HAVE ZERO TO N MACROS AFTER INPUT MACRO

FIGURE 4-1

Table 4-3 provides a complete summary of the worst-case timing multipliers for the four operating conditions. For each operating condition there is a maximum, a nominal and a minimum multiplier. The minimum multiplier is 90% of the typical multiplier. The maximum multiplier is 110% of the typical multiplier. The maximum timing variation possible on a single array is 20%.

There is one multiplier for the internal macros and one for the core macros. **CAUTION:** there is a tendency to interchange the interface and core macro worst-case delay multipliers.

TABLE 4-3
WORST-CASE TIMING MULTIPLIERS

| ARRAY SERIES: -> | | Q14000 | ambiguity | abbreviations |
|---|---|---|---|---|
| | | | | WCMmin |
| Operating | | \| | \| | WCMtyp |
| Conditions: | | ↓ | ↓ | WCMmax |
| MINIMUM OPERATING RANGE (All macros) | minimum typical maximum | 0.70<br>0.78<br>0.86 | 0.9*typ<br>typ<br>1.1*typ | MINmin<br>MINnom<br>MINmax |
| NOMINAL OPERATING RANGE (All macros) | minimum typical maximum | 0.90<br>1.00<br>1.10 | 0.9*typ<br>typ<br>1.1*typ | NOMmin<br>NOMnom<br>NOMmax |
| COMMERCIAL OPERATING RANGE (INTERFACE) | minimum typical maximum | 1.11<br>1.23<br>1.35 | 0.9*typ<br>typ<br>1.1*typ | COMmin<br>COMnom<br>COMmax |
| COMMERCIAL OPERATING RANGE (CORE) | minimum typical maximum | 1.27<br>1.41<br>1.55 | 0.9*typ<br>typ<br>1.1*typ | COMmin<br>COMnom<br>COMmax |
| MILITARY OPERATING RANGE (INERFACE) | minimum typical maximum | 1.19<br>1.32<br>1.45 | 0.9*typ<br>typ<br>1.1*typ | MILmin<br>MILnom<br>MILmax |
| MILITARY OPERATING RANGE (CORE) | minimum typical maximum | 1.59<br>1.77<br>1.95 | 0.9*typ<br>typ<br>1.1*typ | MILmin<br>MILnom<br>MILmax |

# Section 5:

# Power/Packaging

Table of Contents ..... 5-2

## INTRODUCTION

The worst-case power as it relates to junction temperature is used to examine the packaging and the heat-sink requirements of the final product. There are two steps to computing the worst-case power dissipated by the BiCMOS logic array: interface macro power and internal macro power.

## MACRO OPTIONS

TTL macros and most ECL interface macros in the Q14000 Series macro library have the H-option as well as the standard S-option (low power) available. TTLMIX interface macros have the S-option. Internal logic macros have the S-option.

## AMCC MacroMatrix MACRO OCCURRENCE REPORTS

The AMCC ERC software will compute the power dissipation for the interface macros, including overhead current and ECL static power dissipation for ECL output macros. The internal macros will be listed in a table to allow the designer to evaluate their contribution to power based on their individual frequency of operation.

## INTERFACE (I/O) MACRO POWER DISSIPATION

The total worst-case interface current is a function of the macros used, the options selected for those macros, and the overhead current, which is a function of the array chosen.

An unused I/O cell does not dissipate power. An interface macro uses the full current as specified in the Design Guide Macro Summary.

The total worst-case interface current, including overhead current, multiplied by the worst-case current multiplier for the operating conditions results in the worst-case current dissipated by the interface macros:

$$(\text{SUM OF MACROS } I_{CC} + \text{OVERHEAD } I_{CC}) * \text{WCCM} = I_{CCwc}$$
$$(\text{SUM OF MACROS } I_{EE} + \text{OVERHEAD } I_{EE}) * \text{WCCM} = I_{EEwc}$$

Multiply the worst-case current with the appropriate worst-case voltage:

$$I_{EEwc} * V_{EEwc} = P_{EEwc}$$
$$I_{CCwc} * V_{CCwc} = P_{CCwc}$$

Sum the results with any ECL output macro static power dissipation to obtain the total worst-case power dissipation for the interfaced macros.

$$P_{EEwc} + P_{CCwc} + P_{ECLoutputs} = P_{Interface}$$

This procedure is detailed on the following pages.

COMPUTING THE MAXIMUM WORST CASE POWER - INTERFACE
COMPUTE THE TOTAL TYPICAL MACRO CURRENT

- MACRO OCCURRENCE TABLE - INTERFACE MACROS

A macro occurrence table for interface logic macros can be constructed prior to design capture to assist in the computation of internal and total circuit current and power dissipation. At the minimum, a macro occurrence table for the interface macros should provide:

- A list of the different interface macros differentiated by option;
- The number of times each macro appears on the schematics;
- The current ($I_{CC}$ or $I_{EE}$) for one instance of the macro;
- The total current due to the n occurrences of the macro;
- The sums of the $I_{CC}$ and $I_{EE}$ currents.

- ADD THE OVERHEAD CURRENT

The overhead current is the base array current dissipated by the internal regulators, reference generators, selected I/O mode (TTL, ECL, MIXED), and power supply configuration (+5V, -5.2V, dual supply or other). Find the overhead current from the Overhead Current Drain as specified for the array. A summary of the overhead current drain is provided in Table 5-1.

TABLE 5-1
AMCC BiCMOS ARRAYS TYPICAL OVERHEAD CURRENT (mA)

| CHIP V | TTL MODE $I_{CC}$,mA | ECL MODE $I_{EE}$,mA | MIXED MODE $I_{EE}/I_{CC}$,mA | +5V REF ECL/TTL $I_{CC}$,mA | |
|---|---|---|---|---|---|
| Q9100B | 132 | 117 | 121/22 | 140 | ECL 10K |
| Q9100B | 132 | 121 | 125/22 | 143 | ECL 100K |
| Q2100B | 101 | 87 | 90/22 | 109 | ECL 10K |
| Q2100B | 101 | 87 | 91/22 | 109 | ECL 100K |

Add the overhead current drain to the appropriate current dissipation sum already computed:

$$\text{SUM OF MACROS } I_{CC} + I_{CC}|_{\text{OVERHEAD}}$$
$$\text{SUM OF MACROS } I_{EE} + I_{EE}|_{\text{OVERHEAD}}$$

- MULTIPLY BY THE WORST-CASE CURRENT MULTIPLIER (WCCM)

Multiply the results by the appropriate worst-case current multiplier to obtain the worst-case $I_{CC}$ and worst-case $I_{EE}$ current. Unless the circuit uses a single-power supply these two sums must be kept separate.

$$(\text{SUM OF MACROS } I_{CC} + \text{OVERHEAD } I_{CC}) * \text{WCCM} = I_{CCwc}$$
$$(\text{SUM OF MACROS } I_{EE} + \text{OVERHEAD } I_{EE}) * \text{WCCM} = I_{EEwc}$$

THE WORST-CASE CURRENT MULTIPLIER - INTERFACE MACROS

For the Q14000 Series, the worst-case current multiplier for the interface macros, WCCM, is the constant 1.54 for MILITARY and 1.35 for COMMERCIAL grade circuits. The worst-case current multiplier is used to compute the worst-case values for all specified interface macro currents and to compute the worst-case value for the overhead current.

TABLE 5-2
WORST-CASE CURRENT MULTIPLIER

| | |
|---|---|
| MILITARY | 1.54 |
| COMMERCIAL | 1.35 |

- MULTIPLY BY THE WORST-CASE VOLTAGE

The worst-case voltage is dependent on whether the circuit is COMMERCIAL or MILITARY. The typical variation is shown in Table 5-3. For COMMERCIAL circuits, the voltage variation is usually ±5%. For MILITARY circuits, the voltage variation is usually ±10%.

TABLE 5-3
WORST-CASE VOLTAGE

| NOMINAL | COMMERCIAL | MILITARY |
|---|---|---|
| +5.0V | +5.25V | +5.5V |
| -5.2V | -5.46V | -5.72V |
| -4.5V | -4.8V | -4.8V |

Multiply the worst-case current with the appropriate worst-case voltage:

$$I_{EEwc} * V_{EEwc} = P_{EEwc}$$
$$I_{CCwc} * V_{CCwc} = P_{CCwc}$$

- ECL STATIC POWER

The equation used by the AMCC MacroMatrix ERC software to compute ECL static power dissipation for ECL outputs is:

$P_{ECLoutputs}$ = XXmA * 1.3V * NUMBER_OF_ECL_OUTPUTS

where XX is the current based on the termination. If there is more than one termination, the power for each is computed and summed to find the total $P_{ECLoutputs}$.

The 1.3V term represents the absolute average of the -0.8V to -1.8V (NOM) voltage drop in the output transistor. This is considered to be the statistical worst-case for this function.

- ECL OUTPUT TERMINATION CURRENT

Table 5-4 provides the ECL output termination currents used by the AMCC MacroMatrix ERC software to compute the general case. The currents shown are the average current (average of $I_{OH}$ and $I_{OL}$).

TABLE 5-4
ECL 10K/100K TERMINATION CURRENT

| TERMINATION: | CURRENT: | STANDARD MACRO: | ADJUST POWER COMPUTATION: |
|---|---|---|---|
| 25ohm | 28.0mA | NO | YES |
| 50ohm | 14.0mA | YES | NO |
| 100ohm | 7.0mA | NO | YES |
| 200ohm | 3.5mA | NO | YES |

* the average current (average of $I_{OH}$ and $I_{OL}$)
* for termination to -2V

If ECL output load resistances used is other than that specified for the macro, the actual current value must be computed for use in this equation. The ERC software will correctly compute the ECL static output power for 50ohm and 25ohm termination macros.

Note that the duty cycle of the outputs will also affect the final value.

TABLE 5-5
MACRO TERMINATIONS THIS RELEASE

| MACRO | TERMINATION |
|---|---|
| OE70 | 50ohms |
| OK70 | 50ohms |
| UE49 | 50ohms |

- SUM THE RESULT

If there are ECL outputs, compute the ECL static power dissipation and add to the sum. The result is the total worst-case power dissipated by the interface macros for the circuit on the target array.

Sum the results of the macro computations with any ECL output macro static power dissipation to obtain the total worst-case power dissipation for the interfaced macros.

$$P_{EEwc} + P_{CCwc} + P_{ECLoutputs} = P_{Interface}$$

## INTERNAL MACRO POWER DISSIPATION

- MACRO OCCURRENCE TABLE - INTERNAL LOGIC

A macro occurrence table for internal logic macros can be constructed prior to design capture to assist in the computation of internal and total circuit current and power dissipation. At the minimum, a macro occurrence table for the internal logic should provide:

- A list of the different macros differentiated by option;
- The number of times each macro appears on the schematics;
- The number of cells used by each macro
- The number of cells due to n occurrences of the macro
- The frequency at which these macros operate.

It is not necessary to precisely list each individual frequency for each individual macro. Some approximations may be used without adversely affecting accuracy. In the general case, the main power dissipation will not be in the internal macros.

- COMPUTING AN ESTIMATE OF INTERNAL CELL POWER DISSIPATION

The equation used to compute internal cell power dissipation for a given group of macros switching at the same frequency is:

$P_{internal_{wc}}$ = F * 0.2 * G * 20 microwatt/gate-MHz

where: F = the highest frequency in MHz for the macros in the group

0.2 = 20% of the gates switching (estimate)

G (internal gate count) = 4 * internal cell count

The internal cell count is the number of Basic cells used by the design.

By computing this equation for each frequency-group and summing the result, an estimate of the worst-case power dissipation for the internal macros is obtained. Use the same equation for MILITARY and COMMERCIAL computations.

FINAL RESULT

The sum of the estimated total power dissipated by all internal macro frequency groups and the total worst-case power dissipated by the interface macros is the total worst-case power dissipated by the circuit.

## THERMAL COEFFICIENTS - I/O AREA

The temperature coefficients for the interface (I/O macro) area of the Q9100B and Q2100B arrays are shown in Table 5-6.

TABLE 5-6
TEMPERATURE COEFFICIENTS
BiCMOS ARRAYS

| | $TC_{macro}$ (°C) | |
|---|---|---|
| MACRO TYPE: | INPUT | OUTPUT |
| ECL (ANY SYSTEM) | 0.03 | 0.0 |
| TTL (+5 SYSTEM) | -0.07 | -0.3 |
| TTLMIX (DUAL SUPPLY SYSTEM) | -0.10 | -0.2 |

The overall temperature coefficient for the chip I/O area is a weighted average:

$$TC_{chip} = \sum_{\text{all types}} \frac{n * TC_{macro}}{\text{TOTAL NUMBER OF I/O MACROS}}$$

where n = the number of macros of a given type

$TC_{macro}$ = the temperature coefficient for that type

The thermal coefficient is used to derate the I/O current when the temperature is higher or lower than specified. The worst-case current is computed at the maximum temperature for the operating range. Should the part be guaranteed to operate at a lower temperature, then the current may be derated using the temperature coefficient as computed.

## PACKAGE SELECTION

AMCC offers an assortment of packages for the Q14000 Series Logic Arrays shown in Tables 5-8 for the Q2100B and Table 5-9 for the Q9100B. Table 5-7 summarizes the pad limits for the arrays.

Package selection requires that the designer have two computations completed: 1) the total maximum worst-case power dissipation; and 2) the total number of pads required for the design.

The designer also needs the current AMCC Packaging Brochure, which lists the package options for the bipolar arrays as well as the tables providing the $\Theta_{jc}$ and $\Theta_{ja}$ and the reductions possible with forced air and heatsinks.

For the BiCMOS Q14000 Array Series, the number of fixed power and ground pins is less than the number of fixed power and ground pads - two power (ground) pads are bonded out to one power (ground) pin sufficient times to effect the required reduction. For added power and ground pins, they reside on signal pads and are bonded to signal pin positions.

TABLE 5-7
Q14000 SERIES ARRAYS TOTAL PADS

| ARRAY NAME | FIXED POWER-GROUND PADS | CIRCUIT I/O PIN LIMIT | TOTAL CHIP PADS |
|---|---|---|---|
| Q9100B | 56 | 160 | 216 |
| Q2100B | 28 | 80 | 108 |

TABLE 5-8
Q2100B PACKAGES

| PACKAGE NAME | COMMENTS | SIGNAL PINS | POWER/GROUND PINS |
|---|---|---|---|
| 68 PGA | CAVITY DOWN | 48 | 20 |
| 84 PGA | CAVITY DOWN | 64 | 20 |
| 100 PGA | CAVITY UP | 80 | 20 |
| 100 PGA | CAVITY DOWN | 80 | 20 |
| 100 LDCC | 0.050 CENTER | 80 | 20 |

TABLE 5-9
Q9100B PACKAGES

| PACKAGE NAME | COMMENTS | SIGNAL PINS | POWER/GROUND PINS | |
|---|---|---|---|---|
| 132 LDCC | 0.025 CENTER | 92 | 40 | |
| 168 PGA | CAVITY DOWN | 132 | 36 | * |
| 196 LDCC | 0.025 CENTER | 156 | 40 | * |
| 224 PGA | CAVITY DOWN | 160 | 52 | |

* IN DEVELOPMENT

Consult AMCC for your particular array-package combination after an estimate of the required number of array pads has been made. The number of pads required by the circuit is provided as the "EXTERNAL PIN COUNT" by the AMCC MacroMatrix ERC software Population Check Report version (708) and is the sum of all signals, all power (fixed and added) and all ground (fixed or added) pads as indicated on the schematics.

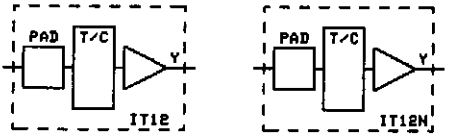
Compute the junction temperature for the product grade (MILITARY or COMMERCIAL) based on the specified operating environment, i.e., temperature; heat sink, if any; air flow, if any; etc.

# Section 7:

# Quicksheets

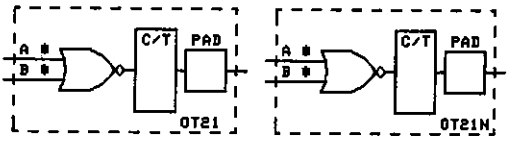
Q14000 BiCMOS (803)

# TTL INPUT

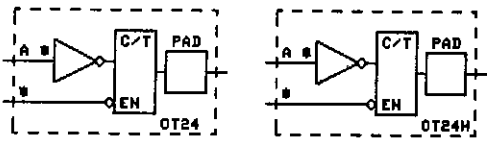



BUFFERED INPUT

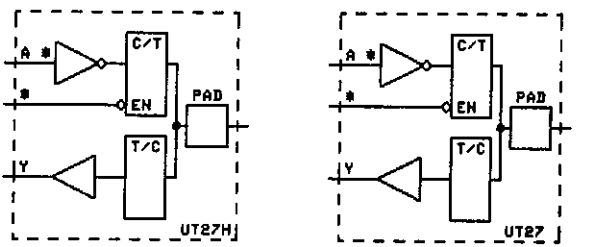
# TTL OUTPUT




OR-BUFFER OUTPUT

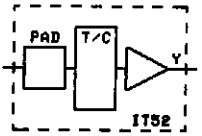



BUFFERED OUTPUT, 3-STATE




BUFFERED I/O BIDIRECTIONAL

# TTLMIX INPUT

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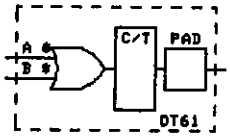
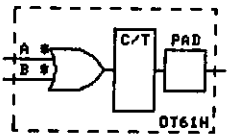
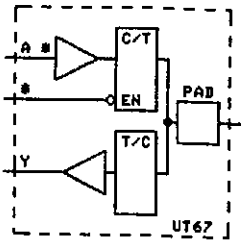
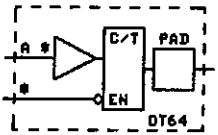
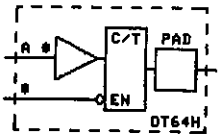



NOT IN (801) RELEASE




NOT IN (801) RELEASE

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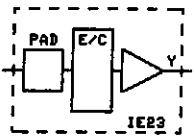


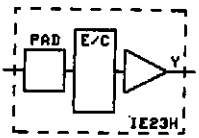

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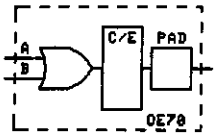
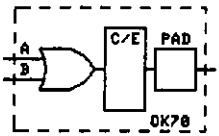
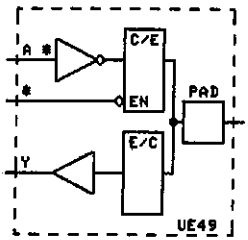
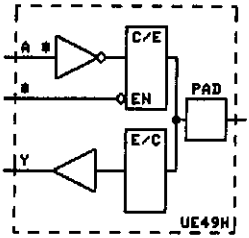
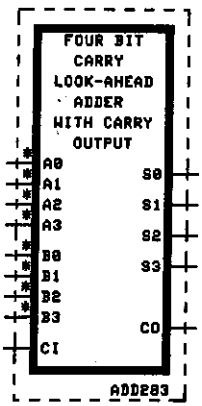


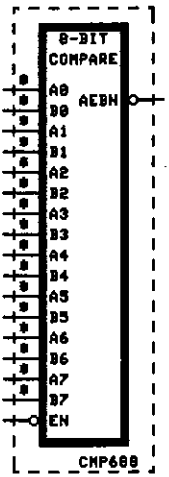



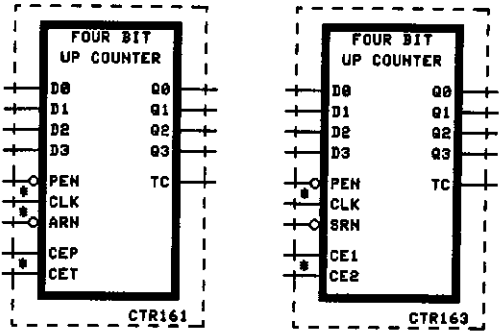

## ADDER



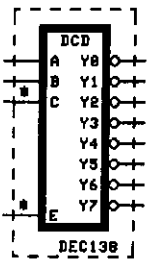

## COMPARATOR



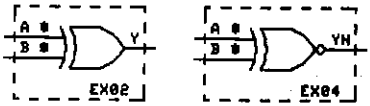
# COUNTERS



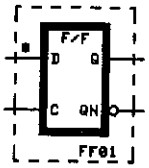

# DECODER

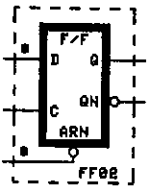


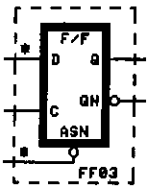

# EXOR/EXNOR

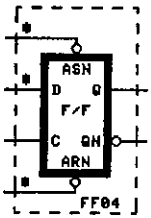


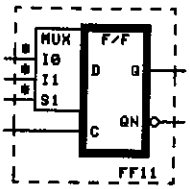
# FLIP/FLOPS

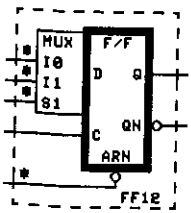

F/F
D
Q
C
QN
FF01

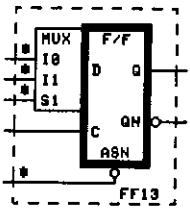

F/F
D
Q
C
QN
ARN
FF02


F/F
D
Q
C
QN
ASN
FF03


ASN
D
Q
F/F
C
QN
ARN
FF04


MUX
I0
I1
S1
F/F
D
Q
C
QN
FF11


MUX
I0
I1
S1
F/F
D
Q
C
QN
ARN
FF12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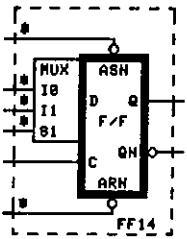
I1
S1
F/F
D
Q
C
QN
ASN
FF13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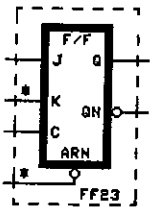
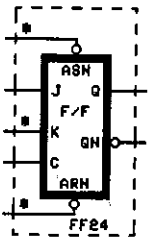
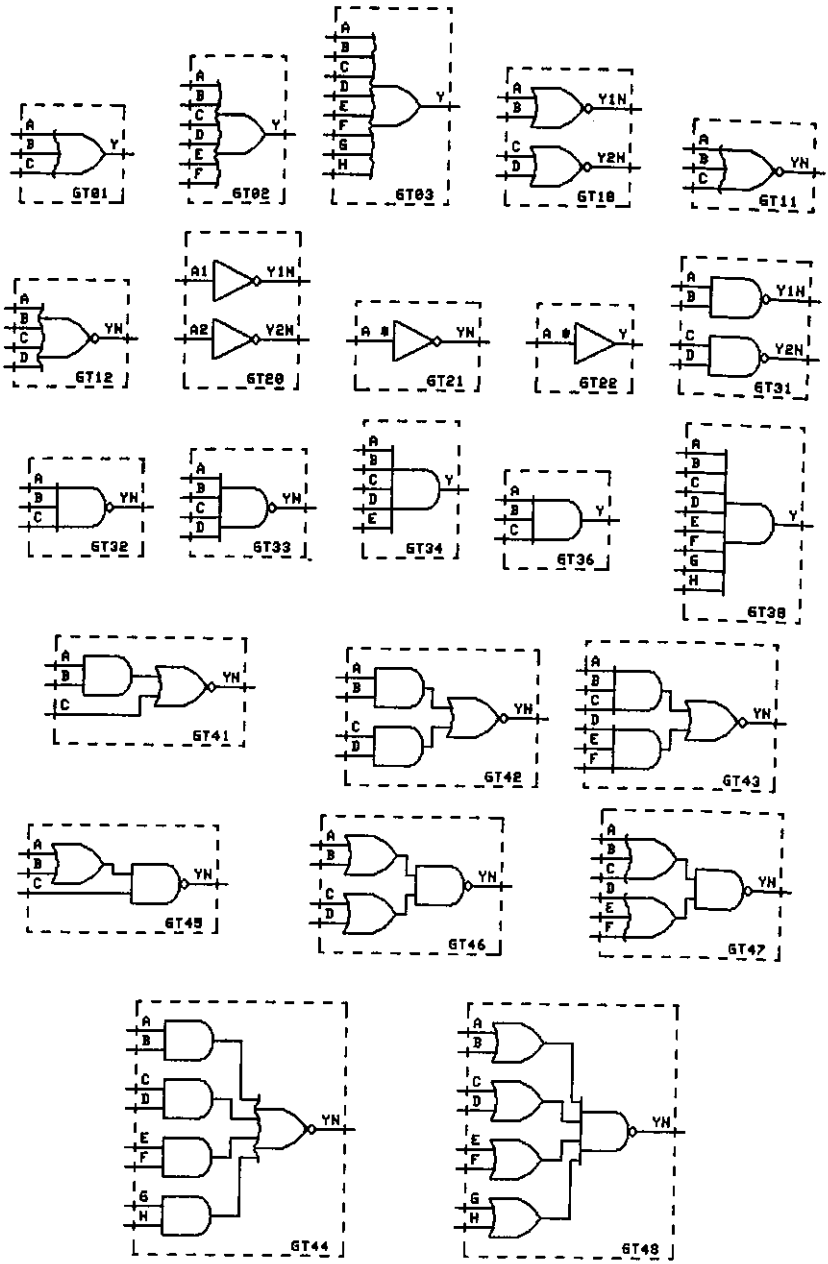
I1
S1
ASN
D
Q
F/F
C
QN
ARN
FF14


F/F
J
Q
K
QN
C
ARN
FF23


ASN
J
Q
F/F
K
QN
C
ARN
FF24

# GATES


A
B
C
Y
GT01
A
B
C
D
E
F
Y
GT02
A
B
C
D
E
F
G
H
Y
GT03
A
B
Y1N
C
D
Y2N
GT10
A
B
C
YN
GT11
A
B
C
D
YN
GT12
A1
A2
Y1N
Y2N
GT20
A
B
YN
GT21
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B
Y
GT22
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B
Y1N
C
D
Y2N
GT31
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YN
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GT34
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B
C
Y
GT36
A
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C
D
E
F
G
H
Y
GT38
A
B
C
YN
GT41
A
B
C
D
YN
GT42
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D
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F
YN
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B
C
YN
GT45
A
B
C
D
YN
GT46
A
B
C
D
E
F
YN
GT47
A
B
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D
E
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G
H
YN
GT44
A
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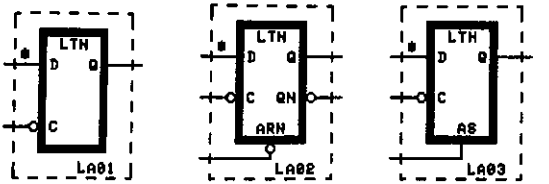
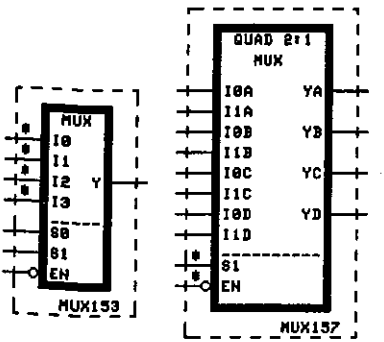
C
D
E
F
G
H
YN
GT48

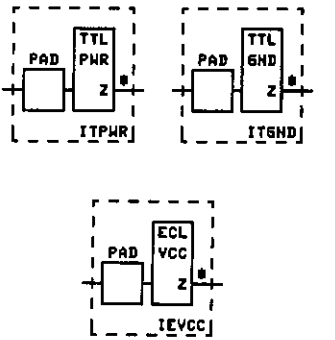
# LATCHES



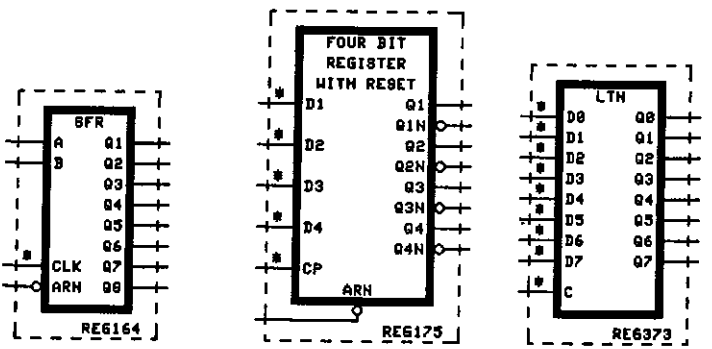

# MULTIPLEXORS




# MISCELLANEOUS

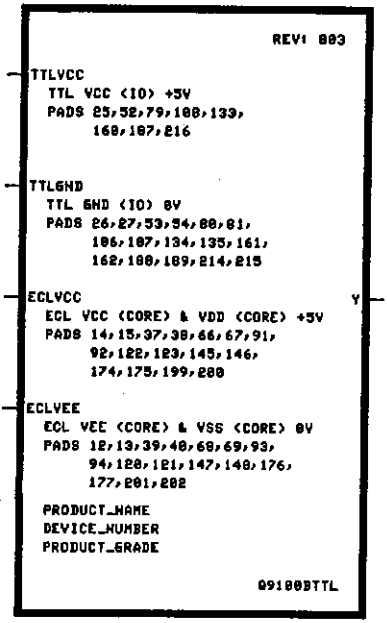


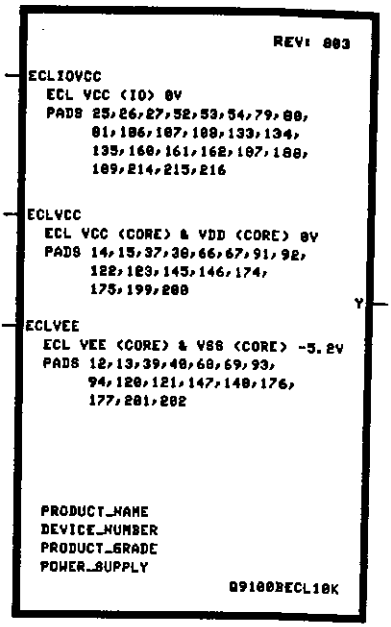

# REGISTERS



# CHIP MACROS




REV: 803
TTLVCC
TTL VCC (IO) +5V
PADS 25,52,79,108,133,
160,187,216
TTLGND
TTL GND (IO) 0V
PADS 26,27,53,54,80,81,
106,107,134,135,161,
162,188,189,214,215
ECLVCC
ECL VCC (CORE) & VDD (CORE) +5V
PADS 14,15,37,38,66,67,91,
92,122,123,145,146,
174,175,199,200
Y
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 12,13,39,40,68,69,93,
94,120,121,147,148,176,
177,201,202
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
99100BTTL


REV: 803
ECLIOVCC
ECL VCC (IO) 0V
PADS 25,26,27,52,53,54,79,80,
81,106,107,108,133,134,
135,160,161,162,107,188,
189,214,215,216
ECLVCC
ECL VCC (CORE) & VDD (CORE) 0V
PADS 14,15,37,38,66,67,91,92,
122,123,145,146,174,
175,199,200
Y
ECLVEE
ECL VEE (CORE) & VSS (CORE) -5.2V
PADS 12,13,39,40,68,69,93,
94,120,121,147,148,176,
177,201,202
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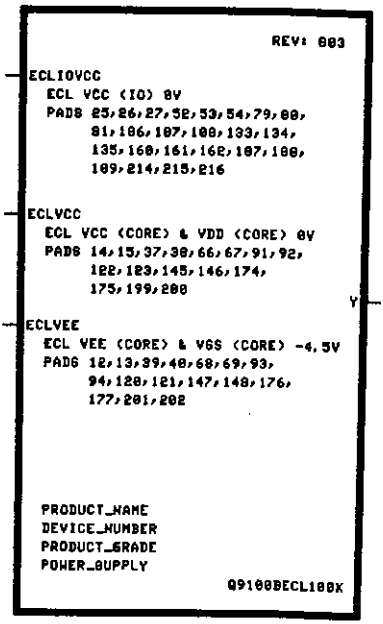
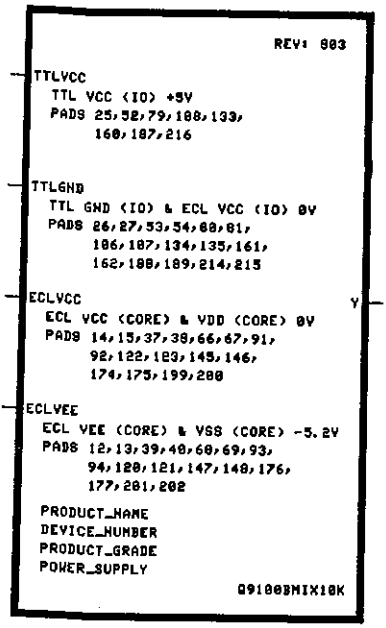
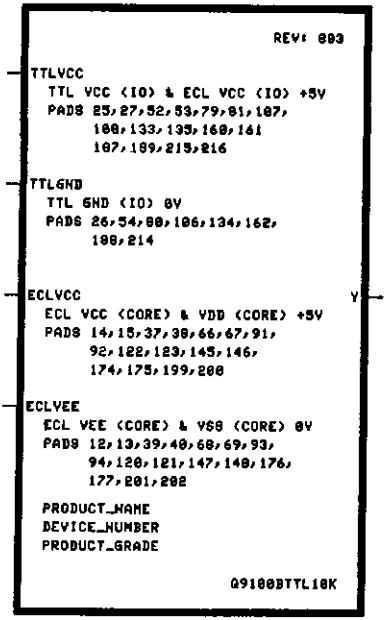
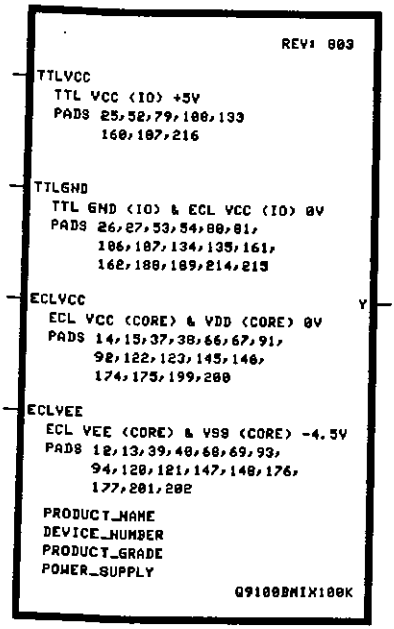
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
99100BECL10K

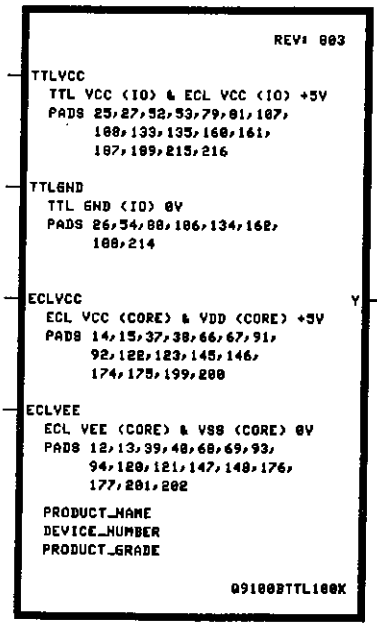

REV: 803
ECLIOVCC
ECL VCC (IO) 0V
PADS 25,26,27,52,53,54,79,80,
81,106,107,108,133,134,
135,160,161,162,107,188,
189,214,215,216
ECLVCC
ECL VCC (CORE) & VDD (CORE) 0V
PADS 14,15,37,38,66,67,91,92,
122,123,145,146,174,
175,199,200
Y
ECLVEE
ECL VEE (CORE) & VSS (CORE) -4.5V
PADS 12,13,39,40,68,69,93,
94,120,121,147,148,176,
177,201,202
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
99100BECL100K

# CHIP MACROS


REV: 003
TTLVCC
TTL VCC (IO) +5V
PADS 25,52,79,108,133,
160,187,216
TTLGND
TTL GND (IO) & ECL VCC (IO) 0V
PADS 26,27,53,54,80,81,
106,107,134,135,161,
162,188,189,214,215
ECLVCC
ECL VCC (CORE) & VDD (CORE) 0V
PADS 14,15,37,38,66,67,91,
92,122,123,145,146,
174,175,199,200
Y
ECLVEE
ECL VEE (CORE) & VSS (CORE) -5.2V
PADS 12,13,39,40,68,69,93,
94,120,121,147,148,176,
177,201,202
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q9100BMIX10K


REV: 003
TTLVCC
TTL VCC (IO) & ECL VCC (IO) +5V
PADS 25,27,52,53,79,81,107,
108,133,135,160,161
107,189,215,216
TTLGND
TTL GND (IO) 0V
PADS 26,54,80,106,134,162,
188,214
ECLVCC
ECL VCC (CORE) & VDD (CORE) +5V
PADS 14,15,37,38,66,67,91,
92,122,123,145,146,
174,175,199,200
Y
ECLVEE
ECL VEE (CORE) & VSS (CORE) 0V
PADS 12,13,39,40,68,69,93,
94,120,121,147,148,176,
177,201,202
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
Q9100BTTL10K


REV: 003
TTLVCC
TTL VCC (IO) +5V
PADS 25,52,79,108,133
160,187,216
TTLGND
TTL GND (IO) & ECL VCC (IO) 0V
PADS 26,27,53,54,80,81,
106,107,134,135,161,
162,188,189,214,215
ECLVCC
ECL VCC (CORE) & VDD (CORE) 0V
PADS 14,15,37,38,66,67,91,
92,122,123,145,146,
174,175,199,200
Y
ECLVEE
ECL VEE (CORE) & VSS (CORE) -4.5V
PADS 12,13,39,40,68,69,93,
94,120,121,147,148,176,
177,201,202
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q9100BMIX100K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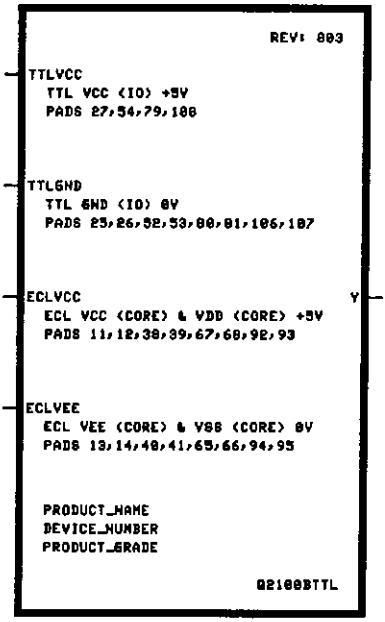
DEVICE_NUMBER
PRODUCT_GRADE
Q9100BTTL100K

# CHIP MACROS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PRODUCT_GRADE
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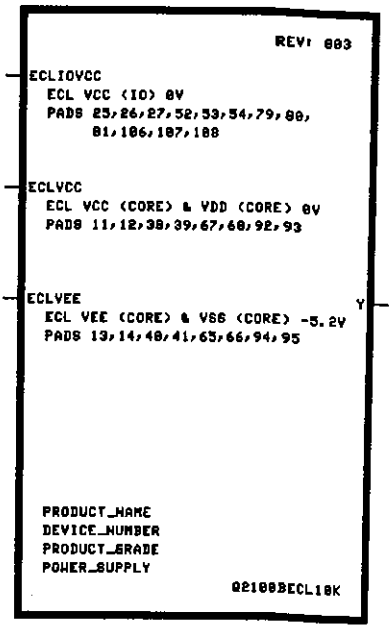
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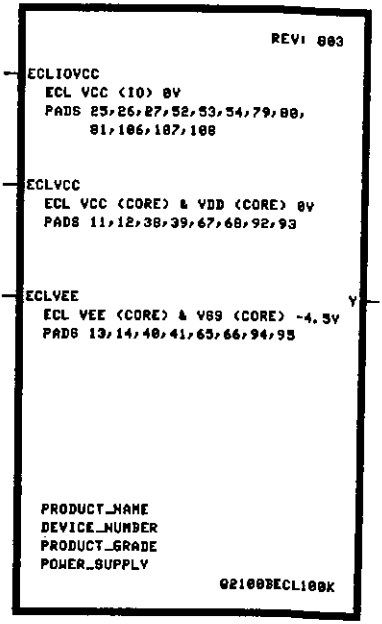
DEVICE_NUMBER
PRODUCT_GRADE
POWER_SUPPLY
Q2100BECL10K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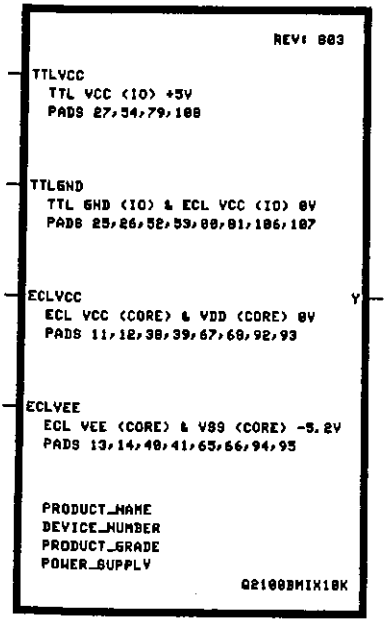
PRODUCT_GRADE
POWER_SUPPLY
Q2100BECL100K

# CHIP MACROS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ECLVEE
ECL VEE (CORE) & VSS (CORE) -5.2V
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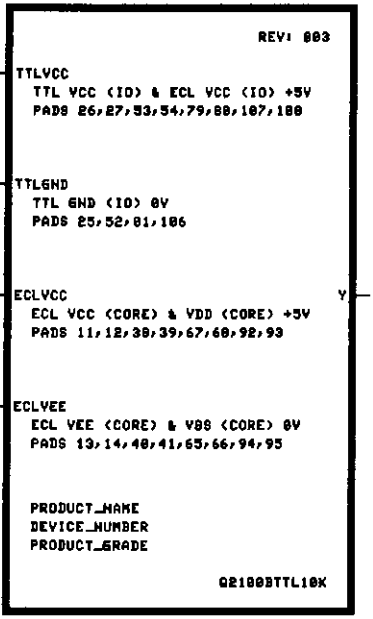
PRODUCT_GRADE
POWER_SUPPLY
Q2100BMIX10K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ECL VCC (CORE) & VDD (CORE) +5V
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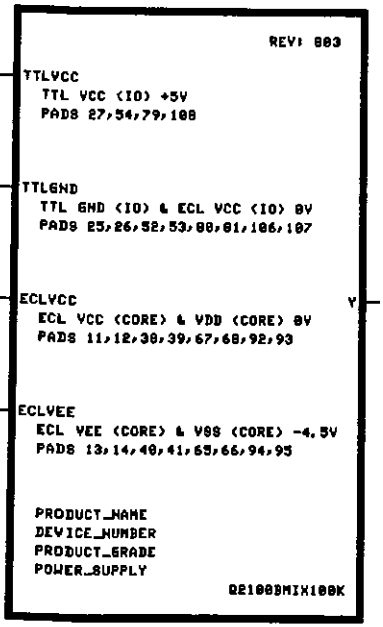
PRODUCT_GRADE
Q2100BTTL10K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ECLVEE
ECL VEE (CORE) & VSS (CORE) -4.5V
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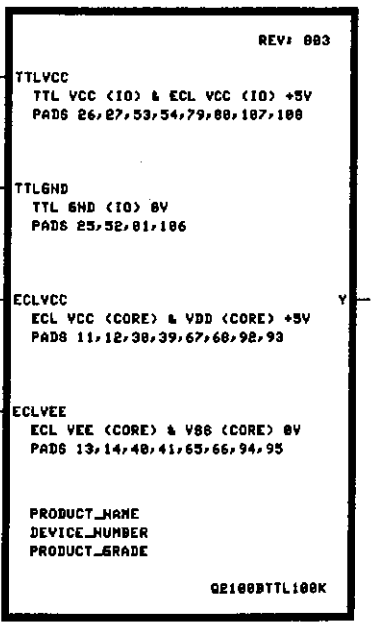
Q2100BMIX100K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ECL VCC (CORE) & VDD (CORE) +5V
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ECL VEE (CORE) & VSS (CORE) 0V
PADS 13,14,40,41,65,66,94,95
PRODUCT_NAME
DEVICE_NUMBER
PRODUCT_GRADE
Q2100BTTL100K

# Section 8:

# Index

# Section 9:

# AMCC Glossary

*3-level gating*
Circuit design technique used internally in the AMCC Q3500S Series logic arrays.

*AC test*
Testing performed with a tester and the packaged part and designed to sample the timing characteristics of the actual die to verify the timing of the actual circuit as produced. Only a few tests are needed since all paths will be similarly affected by the processing and environment and all timing delays constrained to be within a 20% range.

*AGIF*
AMCC generic interface format; used as the means of communicating between a workstation and the AMCC proprietary software tools. The AGIF netlist is called CIRCUIT.SDI.

*ALU*
The arithmetic-logic unit; where data is processed according to the instruction under execution.

*AMCCAD*
AMCC automated design place and route system software.

*AMCCANN*
AMCC Annotation software.

*AMCCERC*
AMCC Engineering Rules Check software.

*AMCCSIMFMT*
AMCC simulation format preparation software. AMCCSIMFMT is EWS-specific.

*AMCCVRC*
AMCC vector rules checker software program.

*Annotation*
The process of adding extrinsic delays into a simulation data base.

*AR*
Asynchronous reset.

*AS*
Asynchronous set.

*ASIC*

Application-specific integrated circuit; generally appled to semicustom ICs.

*Astable*

A circuit with two quasi-stable states; an oscillator.

*At-speed simulation*

A simulation designed to examine the timing integrity of a circuit design.

*Autoplace, auto place*

Macro placement on internal array cells is performed automatically by software.

*Autoroute, auto route*

Interconnection of the macros is performed automatically by software.

*B cell*

Buffer cell; can be used for some logic macros as well. Located around the periphery of the internal cell block in AMCC Q700 Series arrays and in the Q1500A Array; capable of a higher row current limit (three times greater) than the logic cells.

*Back-annotation*

The method of simulation of a circuit after layout, where the loading on a particular net is the sum of the actual fan-out load (electrical load), the actual wire-OR load (electrical load) and the actual metal used to interconnect the pins. The load is a function of the array (die-size) and is accurate within measurement device parameters.

*Bandwidth*

Frequency range of performance for a device (as in the bandwidth of an amplifier).

*BiCMOS array*

A bipolar interface with CMOS core.

*Bidirectional*

Capable of moving in either of two directions at any given time.

*Bidirectional I/O cells*

See I/O cells.

*Binary*
The base two number system where each digit is a power of two. The allowed digits are 1 and 0. In circuit representations of a binary equation the digits 0 and 1 are also called LOW and HIGH or TRUE and FALSE, the equivalent values of which depend on the polarity of the system.

*Bipolar*
One silicon technology used in ICs; radiation-resistant, faster than CMOS at the expense of higher power dissipation.

*Bit*
One Boolean digit; 0 or 1. X or # are the symbols used for "Don't care" and U is used for undefined or unknown.

*Bit-slice*
Two or more bits wide devices such as the AM2901 4-bit ALU, AM29203 4-bit ALU, AM2910 sequences; method of partitioning a design into modules.

*Byte*
Originally meant enough bits to represent a character (code dependent in size); by default a byte is now usually taken as 8 bits. In 16-bit architectures, it is half a word.

*Bundle*
A group of single wires; a bus.

*CAD*
Computer-Aided Design.

*CAE*
Computer-Aided Engineering.

*CAI*
Computer-Aided Instruction.

*CAM*
Computer-Aided Manufacturing.

*Cell*
The smallest uniform repeatable unit on a logic array; there may be more than one type on a given array.

*Cell utilization*
A measure (in %) of the number of internal cells actually used in a design (accessible by a designer). The suggested limit is 85% for the Q700, Q3500 and Q5000 Series.

*Chip*
Slang for integrated circuit; the die in an IC.

*Circuit*
A logical function or functions constructed from electrical devices.

*Circuit building block*
The basic unit available to simplify circuit design. SSI, MSI, LSI and VLSI represent the evolution of hardware building blocks.

*Circuit density*
A measure of the number of equivalent 2-input NOR gates a design would require, such as 700, 1500, 2000, 3500, 5000 and 20000.

*Clock, CLK*
Clock signal; in many AMCC macros the rising edge is taken as the active edge. Either edge may be the clocking or active edge in a circuit or a macro; complex systems use both edges to operate latches and registers.

*Common clock*
Reference to using the same clock signal on all devices on a board or all functions within a semicustom array. A single common clock is the preferred and the simplest method of design. It is also easier to test.

*Configurable cells*
Able to be altered to fit a particular application.

*Conventional ECL*
Standard REF ECL, ECL 10K or ECL 100K, voltage supplies are -5.2V (ECL 10K) or -4.5V (ECL 100K).

*Critical path*
The longest path (largest propagation and loading delay) through a circuit.

*Custom macro*
One that is designed specifically to meet the customer's requirement and is not currently in the released macro library.

*Delay offset*
Lag.

*Design element*
Basic part of a design.

*Demultiplexor*
Demux; a decoder; a device that allows one or more input lines to select between n output lines where the number of inputs is less than the number of outputs.

*Design rule verification*
ERC software performs the function of circuit-level design rule verification, or verification that electrical restrictions have not been violated. Wafer fabrication design rules are a set of electrical and minimum physical parameters which can be guaranteed for the process.

*Device specification*
Document summarizing parametric, functional, AC, environmental, test and packaging agreements as accepted and approved by both the customer and AMCC.

*Die*
The silicon chip itself; plural is dice.

*Differential ECL inputs*
Pairing of true and complement signals to allow dual-rail communication for increased noise immunity. Required for remote signals, off-board communication with +5V REF ECL and when operating at 200MHz and higher (series dependent).

*Driver*
An internal macro which provides extra drive capability, extra current and can handle extra loads. AMCC arrays have drivers capable of 15, 18, 25 and higher fan-out loads.

*Dual-in-line*
DIP; Type of package with leads perpendicular to the cavity and spaced .100 inch from each other on the same side and .300, .400 or .600 apart from the leads on the opposite side. Many low external pin count ($\leq$64) circuits are packaged in DIPs.

*+5V REF ECL*

The voltage supplies are +5V and GND; for use with TTL I/O in a mixed I/O mode design.

*ECL*

Emitter-coupled logic. ECL is extremely high-speed. The normal power supply is -5.2V for ECL 10K and -4.5V for ECL 100K. Logical one is -0.8V; logical zero is -1.80V for -5.2V ECL 10K (an average voltage magnitude of 1.3V). The speed comes from the fact that the transistors within the gates are never driven into saturation, eliminating the time required for the transistors to come out of saturation.

*ECL 10K*

ECL whose DC parametrics vary with temperature; ECL using a power supply of -5.2V.

*ECL 100K*

ECL using a power supply of -4.5V; it is temperature- compensated but yields a DC parametric constant over the temperature range.

*ECL, pseudo*

This is +5V REF ECL, either ECL 10K or ECL 100K operated with a TTL power supply of +5V, to allow ECL functions on a TTL board.

*Emitter-follower*

A circuit used to provide drive after the logic portion of an ECL circuit; the voltage gain of an emitter- follower is close to unity.

*Equivalent gates*

BiCMOS-2 input NAND; Bipolar-2 input NOR.

*ERC*

Engineering Rules Checks or engineering reports and checks. Support software on the various EWS designed to flag misconnects, naming errors, improper wire-ORs, excessive fan-out, GND checks, etc.and to generate reports on macro usage, current dissipation and loading.

*Etch*

Used to refer to the metalization interconnects.

*EWS*

Engineering workstation; a computer-graphics system specifically oriented to support circuit design development from schematic capture through simulation, timing analysis, testability analysis, and eventually test pattern generation. Some can handle layout, PG tape pattern generation. At the minimum, it will produce a net-list from the captured schematic.

*External pin*

A pin on the outside on the die used to interface the circuitry to the outside world.

*Extrinsic delay*

The delay due to metal (capacitance load) that is between one macro and another or the delay due to package pin capacitance and system load on a output macro.

*Fan-in*

The number of electrical loads presented by an input pin to the driving device, applies to macros within an array or to discrete devices.

*Fan-out*

The number of components to which a signal is connected; For the Q700 and Q1500 series, macros are available to drive 1, 6, 9 or 15 loads. For the Q3500 Series, macros are available to drive 1, 4, 9, 15, 18 or 25 loads.

*Fault, as in logical fault*

An error due to hard or soft failure such that the logical function implemented is not what is desired. (e.g., SA1, SA0, SAX)

*Fault coverage*

The inclusion in the test set of a test to cover each possible, observable fault at least once. A measure of this coverage expressed in per cent. Recommended coverage is 90% or higher.

*Fault grading*

The process of estimating the percentage of faults tested by the test vectors.

*FIS*

Fixed instruction set [microprocessor]

*Flat-pack*
A minimum volume package with leads or connectors distributed radially on all four sides and paralled with the die cavity. Flat packs are commonly used where a high pin-count, very light weight packaging system is needed. Used in military and space systems.

*FP*
Abbreviation for flat pack. Package type.

*FPGA*
Field programmable gate array.

*FPLA*
Field programmable logic array; "AND" array user- programmable, some pre-selected subset of the $2^n$ product terms is available from the n inputs (array-dependent), "OR" array user-programmable, any product term (of those available) and be ORed to the y outputs.

*FPLS*
Field programmable logic sequencer.

*Front-annotation*
The method used to predict the loading on a circuit by using the actual fan-out (electrical) load, the actual wire-OR (electrical) load and the statistically estimated metal (physical) load, where the estimate is the mean of the collected data of observations made on previous circuits. The estimate is a function of the fan-out and wire-OR loads, in terms of the physical pin connect and the array (die size).

*Function cell*
Internal logic cell capable of supporting one or more logic operations, depending on the cell size.

*Function macro*
Internal macro, operates at internal ECL levels (one-half volt ECL for AMCC bipolar arrays), placed on internal logic or buffer cell (optional placement).

*Functional elements*
See function macro.

*Functional simulation*
Simulation designed to examine the functional integrity of a circuit design.

*Functionality*
Degree of density of a design; also the logical integrety of a Boolean circuit, independent of detailed speed or parametric behavior.

*Gate array*
An array formed from elementary gates, usually 2-input NOR or 2-input NAND (CMOS) gates. A gate array is configured into a variety of logical circuits via customized interconnect.

*Gate delays*
The time it takes to propagate a signal through a gate.

*Gate equivalent circuit*
Unit of measure; equivalent gates refers to the number of gates of a given complexity (2-input NOR, 2-input NAND) that would be required to perform the same function.

*Generic*
Non-specific; applies to more than one of a kind (workstation technology)

*Heatsink*
A device which enhances thermal conductivity, usually metal.

*Heatsink attachment*
The technique and conditions associated with adhering heatsink to the package. This is usually performed on cavity down PGAs.

*Heatsink drawing*
Outline drawing describing dimensions and tolerances of customer heatsink.

*Hertz, HZ*
Cycles/second.

*Hierarchical structuring*
Generally a tree-like structure for top-down design from block diagram to detailed circuit. Depending on the EWS, this can involve nesting, blocks, cells (on-page-nest) and multiple directory levels.

*High performance*
High-speed, high density.

*High speed macro option*
This version of the macro is designed for high speed applications with associated greater power dissipation.

*High speed option*
The macro has another version which is designed for high speed, generally at the cost of increased power.

*I cell*
Accommodates macros for input type functions only. CMOS refers to these as dedicated input cells.

*IC*
Integrated circuit

*$I^2L$*
Integrated injection logic.

*I/O cell*
Stands for Input/Output Cell. An interface cell that accommodates macros for input, output and bidirectional functions as well as 3-state enable drivers; where interface functions are performed.

*Interconnect verification*
Validation of the interconnections between macros used to form a circuit.

*Interface*
Taken to be the transition between external and internal levels of a device.

*Interface macro*
A macro whose function is to perform the translation between external and internal device levels.

*Internal logic cell*
Cells designed for logical functions and not for I/O; can accommodate certain buffers.

*Internal logic macro library*
A set of macros which may be placed on the internal logic cells; they may not be restricted to those cells.

*Internal macro*
Internal Logic Macro; A functional macro.

*Internal pin*
A pin on a macro that is used to connect it to the other macros on the array (in the circuit). Internal pin count is a measure of routability.

*Intrinsic delay*
The delay within a macro, referred to as $T_{pd}$ delay; the propagation path delay from a macro input pin to an output pin.

*Junction-isolated*
Conventional bipolar technology. Used for the Q700 and Q1500 Series Logic Arrays.

*Junction temperature*
See $T_J$.

*L cell*
See logic cell.

*LLCC*
Abbreviation for leadless chip carrier. Package type.

*LDCC*
Abbreviation for leaded chip carrier. Package type.

*Leaded chip carrier*
See LCC.

*Leadless chip carrier*
See LDCC.

*LED*
Light-emitting diode.

*Load delays*
The amount of time delay caused by loading on the macro due to electrical effects of fan-out loading, wire-OR loading and the physical metal etch.

*Logic array*
An array of predefined base-wafer transistor, diode and resistor components that can be configured into a variety of logical circuits via two-level metal interconnect.

*Logic cell*
Internal cell, function cell. Cells designed for logical functions and not for I/O; can accommodate certain buffers.

*Logic functions*
See functionality.

*Low-power macro*
A macro option designed to use less power than the standard option at the the cost of slower propagation delays.

*Low-power option*
Same as low-power macro; macro options.

*LSI*
Large Scale Integration, from 200 to 1000+ equivalent gates on a chip.

*LSTTL*
Low power Schottky TTL.

*Macro*
Pre-designed logical function with a name; may be multiple cells.

*Macro*
Functions

*Macro library*
The collected set of macros that are valid for use in a given array or array series.

*Macro library element*
A macro, either simple (0.5 cell to 1 cell) or MSI (multiple-cell).

*MACROMATRIX™*
An integrated set of software tools for logic array design.

*Macro options*
Variations on the basis macro specification such as low-power, high-power, high-speed. The propagation time and current specifications of the options will vary from the standard while the function performed does not. Drivers do not have options. Different ECL types and power supply configurations are handled by macro versions.

*Macro oriented*
An array arranged as repeated groups of configurable components in contrast to a "sea of primitives gates" structure.

*Macro version*
A macro meant for another ECL type (ECL 10K vs. ECL 100K) or power supply (+5V REF ECL vs. STD REF ECL). The parameters are identical.

*Marking instructions*
Device labelling (lid, topside) outlined in customer design submission documentation and/or device specification.

*Mask*
Photo process negation; etch pattern master.

*Metal*
Interconnect used for intra-macro definition and inter-macro connection.

*Metalization*
The process steps used to deposit metal on the array.

*Meta-assembler*
Used for microprogram development. It allows a definition of the source language in which the micro code will be written; useful for vector documentation as (see DEC's MICRO2).

*Microprogrammable architecture*
The architecture may be altered by programming different control bits; an architecture that is bit-slice organized.

*Monostable*
A circuit with one stable state and one quasi-stable state. Also called a one-shot, a delay circuit, a single-cycle circuit, a gating circuit.

*MOS*

Metal-oxide semiconductor; developed for denser, lower performance circuits. Simpler processing and fewer mask layers allow larger circuits to be produced.

*MSI*

Medium Scale Integration; 20-100+ equivalent gates on a chip.

*MSI functions*

Functions of size/complexity appropriate to MSI devices; Medium scale functions; MUX, decoder, register. See above.

*MSI LIBRARY*

The collection of large, multiple cell, macros

*MSI LOGIC MACROS*

Large, multiple cell macros

*MUX*

Multiplexor; also spelled multiplexer; a select one of n device where n input lines are reduced to one output, the nth line active is selected by one or more selection control inputs.

*Net*

The etch required to connect one output pin to all of its destination pins plus any etch required to connect any other sources wire-ORed to that pin. Also described as "photolithographically determined interconnect metalization". A wire-net refers to the representation of a net on a circuit schematic.

*Netlist*

A listing of all of the interconnects within a circuit.

*NRE*

Non-recurring engineering charge ($)

*ns*

nanosecond, $10^{-9}$sec.

*Output cell*

A cell that accommodates output-only functions.

*Output macro*

Macro that performs the translation from internal levels to external levels for a device. Depending on the cell complexity, it may require the use of a buffer or may provide its own.

*Oxide-isolated*

Another bipolar technology; used for the Q3500 Series Logic Arrays.

*Package outline drawing*

Diagram which defines the outside dimensions and tolerances of a selected package.

*PAL*

Programmable Array Logic; an optimized variant of a PLA (more inputs, more outputs or more functionality by reducing the width of the OR portion of the array). "AND" array user-programmable, "OR" array pre-programmed, groups of product terms are ORed to the y outputs according to the pre-arranged, pre- programmed pattern.

*PAR*

Pre-Approval Request required to be submitted to establish feasibility or initiate development of custom macros or to obtain specification or ERC/VRC waiver.

*Parametric test*

ATE measurements made to verify interface thresholds and currents as well as static device power. Measurement of $V_{IH}$ - $V_{IL}$

*Parametric vectors*

Vectors developed for use on a tester to provide $V_{IH}$-$V_{IL}$ measurements and characterization.

*PC, PCB*

A printed circuit board has interconnections between points printed in metal on the board.

*PGA*

Pin grid array; a package type suitable for high pin-count requirements, it has pins .100 inch apart on 10x10 through 17x17 matrices brazed perpendicular to the die cavity.

*Piece-price*

Cost of an individual device ususally referred with the respect to production volume.

*Pin Matrix*

Matrix describing the relationship between bonding post and output pin in PGA package.

*PLA*

Programmable Logic Array; either AND-OR or NOR-NOR structure.

*PLD*

Programmable logic device (any)

*Power/density*

Ratio of the density (number of gates) to the power (current and therefore heat) possible in a given technology.

*Power I/R drop*

A voltage drop along the power bus created by distance from the power source.

*Power option*

Macro option that provides extra current to drive additional fan-out loads without altering the function or the propagation delay.

*PROM*

Programmable read-only memory; "AND" array, pre-programmed (at the factory), n inputs, $2^n$ product terms; "OR" array, user-programmable, any of the product terms can be ORed to the y outputs.

*Propagation delay*

The time it takes a signal to pass through a macro from input to output, specified in typical time in the macro listing in the AMCC design guides. Note: AMCC uses Tpd as opposed to $t_{PD}$ for this value.

*Pseudo-ECL*

ECL operating in the TTL voltage range, using +5V and GND. More properly called +5V Ref ECL.

*Q*

True output of a F/F or latch.

*QN*

Complementary output of a F/F or latch.

*R*
Reset Q output to FALSE, usually = 0. (S set Q output to TRUE, usually = 1.)

*Radiation Hardness*
Degree of resistance from radiation effects.

*Prototype*
Initial devices shipped as part of NRE activity; processed to AMCC's standard prototype grade flow.

*RAM*
Random Access Memory, used to refer to Readable-writable Memory.

*Re-spin*
An iteration of the same or similar design.

*ROM*
Read Only Memory

*Routing channels*
Paths which can be used during layout to complete circuit interconnections.

*Scan-set*
A test methodology which allows loading of all combinatorial logic into register files.

*SCD*
Specification Control Drawing.

*Schematic*
Logic symbol design; macro symbol representation of the design.

*Schematic capture*
The process of entering macros and their interconnections into an EWS prior to error analysis and simulation.

*Sea-of-cells*
Gate array architecture which butts macro cells together, typically routes on 2nd and 3rd layer metal, eliminating routing channels between cells.

*Sea-of-gates*
Gate array architecture which has rows of transistors with no predefined routing channels. Typically routes on 1st layer metal over unused components.

*Semicustom array*
An array which is pre-designed in all base levels, leaving the top two levels for user-defined connections.

*Series*
As in logic array series; devices which are basically similar, differing in size. Q700, Q710, Q720 is one such series; a related set of products.

*Series gating*
Transistor chaining.

*Shell*
Software routine designed to screen the user from direct routine execution and calls; user interface for execution.

*Signal I/O placement*
Placement of an I/O macro onto an I/O cell.

*Simulation vector*
A bit-pattern used to evaluate functionality or timing performance of a circuit or array.

*Single-ended input*
Single rail, one polarity (as opposed to differential input).

*Skew*
The amount of variation in propagation delay between two logical gates. A function of placement, switching, whether the two gate functions are on the same macro, etc. A worst-case processing variation skew for AMCC bipolar arrays is 20% for like-edge, identical macro.

*Speed/power ratio*
Term used to indicate the trade-off of higher speed for higher current and therefore power dissipation.

*Standard cell*
A semicustom methodology, which yields variable die size and effects all silicon layers.

*SSI*
Small Scale Integration; 2-20 equivalent gates on a chip; AND, OR, NOT level gates.

*SSO*
Simultaneously switching output.

*Stabilization time*
Time required for a circuit to reach a stable, known state.

*Standard macro*
The basic parametric configuration for a macro. All macros have an S-option although drivers have only one option.

*Testability Analysis*
Evaluation of the controllability and observability of a circuit. Controllability is the measure of how easy it is to toggle a node. Observability is the measure of whether or not the toggling of a node can be seen at an output easily, with difficulty, or not at all.

*Three-level gating*
Three-stage transistor staging; proprietary technique used in the Q3500 Series Bipolar Logic Arrays.

*TTL*
Transistor-Transistor logic; aka $T^2L$.

*TTL output drive*
See $I_{OL}$

*Turbo*
An AMCC design technique used to give dynamic current to the output emitter follower.

*Uncommitted logic*
Logic whose use or application is not predetermined by the manufacturer.

*VHSLSI*
Very high-speed large scale integration. See VHSIC.

*VHSIC*
Very high-speed integrated circuits, from the American military program.

*VLSI*

Very large scale integration, over 1000 equivalent gates, (1000-10000 gates on a chip).

*Wafer*

The silicon slice (various diameter circles) upon which multiple layers of doped materials have been placed to form a number of usable component chips known as dice. Yield is usualy referred to the number of usable die per wafer.

*Waiver*

Agreed-upon deviation from standard design submission flow, error-free ERC/VRC, or device specifications.

*Worst-case COMMERCIAL*

Refers to the multiplication factors used to compute worst-case power and worst-case path propagation delay when the circuit is for COMMERCIAL application.

*Worst-case MILITARY*

Refers to the multiplication factors used to compute worst-case power and worst-case path propagation delay when the circuit is for MILITARY application.

## SYMBOLS

$F_T$
The unity-gain frequency of a transistor.

$V_{IH}$
High-level input voltage. The minimum voltage that should be applied to the input of a device for a logical 1 voltage level. A maximum may be specified; the input current will become very large if this maximum is exceeded. For AMCC bipolar logic arrays this is 2V.

$V_{OH}$
High-level output voltage.

$V_{IL}$
Low-level input voltage. The maximum voltage that should be applied to the input of the device for a logical 0 voltage level. For AMCC bipolar Logic Arrays this is 0.8V.

$V_{OL}$
Low-level output voltage.

$V_{IK}$
Input clamp diode voltage, limits input swing.

$T_{pd}+-, T_{PLH}$
Propagation delay time, LOW-to-HIGH-level output.

$T_{pd}+-, T_{PHL}$
Propagation delay time, HIGH-to-LOW-level output.

$T_{pd}++$
Propagation delay time, HIGH-to-HIGH-level output.

$T_{pd}--$
Propagation delay time, LOW-to-LOW-level output.

$T_{PLZ}$
Output disable time, LOW-to-high-impedance (off) output.

$T_{PZL}$
Output enable time, high-impedance (off) to LOW output.

## SYMBOLS

*$T_{PHZ}$*

Output disable time, HIGH-to-high-impedance (off) output.

*$T_{PZH}$*

Output enable time, high-impedance (off) to HIGH output.

*Tsu*

Set-up time; the minimum time between the application of a data signal and the active edge of the clock. A negative set-up time implies that the data must remain "set-up" after the active edge of the clock. AMCC specifies Tsu as worst-case (the minimum for which operation is guaranteed).

*Th*

Hold time; the minimum time between the application of a clock signal and the removal of the data signal being clocked. A negative hold time imples that the data may be removed prior to the arrival of the active edge of the clocking signal. AMCC specifies Th as worst-case (the minimum for which operation is guaranteed).

*Trec*

Recovery time; the minimum time required between the removal of a set or reset and the next active edge of the clock for the correct operation of the device to be guaranteed.

*$f_{max}$*

Maximum clock frequency; highest rate at which a clock input can be driven and still maintain stable transitions.

*PW*

Pulse width. The minimum time required between edges of the driving signal. AMCC specifies PW as the wort-case (the minimum for which operation is guaranteed).

*$I_{CC}$*

The current dissipated by the macro, into the Vcc supply of the circuit. For individual macros, the current dissipated by that macro (TYPICAL). When computing the supply current for an array, it will be a function of the macros used in the array plus the overhead current for the I/O mode. It may also be a function of the number of TTL input macros.

## SYMBOLS

*$I_{CC}$ HIGH*
The current dissipated by the macro when the output is logical HIGH.

*$I_{CC}$ LOW*
The current dissipated by the macro when the output is logical LOW.

*$I_{CC}$ HIGH-Z*
The current dissipated by the macro when the output of high-impedance OFF.

*$I_{EE}$*
The current dissipated by the macro, into the $V_{EE}$ supply of the circuit. For individual macros, the current dissipated by that macro (TYPICAL). When computing the supply current for an array, it will be a function of the macros used in the array plus the overhead current for the I/O mode. It may also be a function of the number of TTL input macros (unless 100 ECL or a Q3500 design).

*$I_{OL}$*
TTL output drive when the output logic level is LOW. The current dissipated by the macro then sink capability of an output. For AMCC bipolar Logic Arrays this is 20mA.

*$I_{OH}$*
TTL output drive when the output logic level is HIGH.

*$I_{IL}$*
TTL input source when the input logic level is LOW. The current sink capability of an output. For AMCC bipolar Logic Arrays this is 20mA. Some individual macros specifications carry the IIL for the individual macro. This is not used in power computations (used in the test process only).

*$I_{IH}$*
TTL input source when the input logic level is HIGH.

*$I_I$*
Input HIGH current at maximum $V_{in}$.

*$I_{OS}$*
Output short circuit current.

## SYMBOLS

$T_J$

Junction temperature of a device; specified as the maximum for which operation can be guaranteed. For MILITARY circuits, $T_J$ = 150°C. For COMMERCIAL circuits, $T_J$ = 130°C.

- Avoid floating nodes on internal 3-state busses or external bidirectional busses.
- Use Johnson (a.k.a. Mobius, Ring or Twisted-tail) counters or separate flip/flops to decode terminal counts. The loading on the Q outputs is identical, eliminating the loading skew (not the metal skew), and the outputs are a Gray code - only one output changes state per clock cycle. (Binary counter decoding can cause glitches.)
- Compensate for rising and falling edge loading skews and the reversed TTL input translator rising and falling edge skews by inversion as needed to reduce pulse stretch and pulse shrink phenomena.