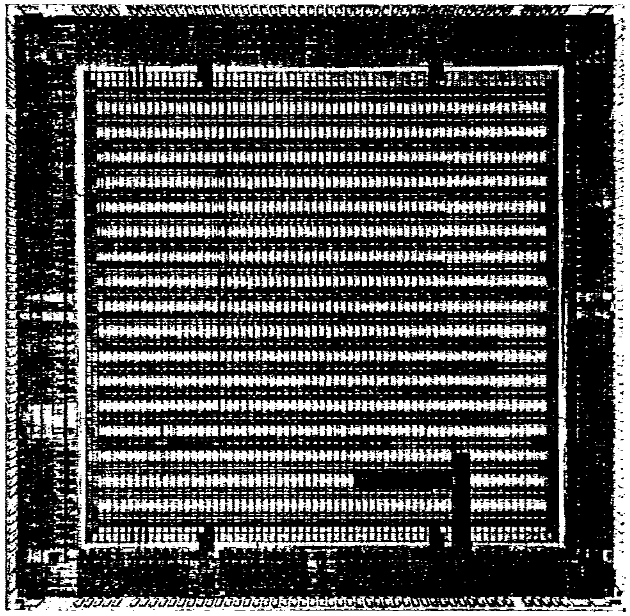
AMCC®

DEVICE SPECIFICATION

Q14000 SERIES BiCMOS LOGIC ARRAYS

T-42-11-15

DESCRIPTION



The AMCC Q14000 Series of BiCMOS logic arrays is comprised of five products with densities of 2160, 5760, 9072, 13,440 and 27,520 equivalent gates. The series is optimized to provide CMOS densities with bipolar performance for today's sophisticated semicustom applications.

The Q14000 Series combines 1.5-micron CMOS features with an advanced 1.5-micron oxide-isolated bipolar process on a single silicon chip. AMCC's BiCMOS is especially optimized for high speed utilizing BiCMOS core with primarily bipolar devices in the I/O. The BiCMOS process uses an N-type epitaxial layer as the foundation for both the NPN bipolar and CMOS devices. The CMOS transistors are used for logic implementation only while bipolar devices are utilized for drive capability necessary for large intermacro connections. For high performance systems, such capability is necessary to drive high fanout and large metal interconnect.

In addition, the Q14000 Series is highly flexible providing interface to ECL 10K, ECL 100K, TTL, CMOS or mixed CMOS/ECL/TTL systems.

An extensive library of SSI and MSI logic macros is available in conjunction with AMCC's MacroMatrix® design kit. MacroMatrix is available for use with Dazix, Mentor, Valid and Verilog as well as Lasar 6.

PERFORMANCE SUMMARY	
PARAMETER	VALUE
Typical internal gate delay	
1 load, no metal	.43 ns
2 loads, 2 mm of metal	.52 ns
Typ. internal F/F toggle frequency	240MHz
Typ. input delay	
ECL-	1.3 ns
TTL-	3.0 ns
Typ. output delay	
ECL-	.6 ns
TTL-	2.2 ns
ECL compatible output drive	25 Ω, 50 Ω
TTL compatible output drive	8, 20, 48 mA
Cell utilization	up to 100%

Table 1

FEATURES

- Mixed 1.5 Micron CMOS/1.5 Micron Bipolar Technology
- Equivalent Speeds of First-generation ECL - .5nS Gate Delays
- Extremely Low Power
- High Density - Up to 27,520 Usable Gates
- Low Interconnect Delay Penalty - 25 pS/fanout
- Speed/Power Programmable I/O Macros
- 10K ECL, 100K ECL, CMOS, TTL or Mixed CMOS/ECL/TTL
- Operation from -55°C Ambient to +125°C Case
- Performance Specified to T_J = 130°C Commercial, 150°C Military
- High Output Drive Capability - 48 mA

PRODUCT SUMMARY					
DESCRIPTION	Q2100B	Q6000B	Q9100B	Q14000B	Q28000B
Equivalent gates	2160	5760	9072	13440	27520
Internal logic cells	540	1440	2268	3360	6880
I/O pads	80	132	160	226	256
Fixed power/ground pads	28	50	56	56	112
Total pads	108	182	216	282	368
Typical power[1]	1-2W	1-2.8W	2-4W	1.4-4.4W	2.8 - 9W
Available	NOW	NOW	NOW	NOW	NOW

1 4.5Volts supply @ 25°C, 50% inputs/50% outputs; 40MHz with 20% of internal gate switching.

9000-0456

Table 2

Q14000 SERIES BICMOS LOGIC ARRAYS

T-42-11-15

Process Cross Section

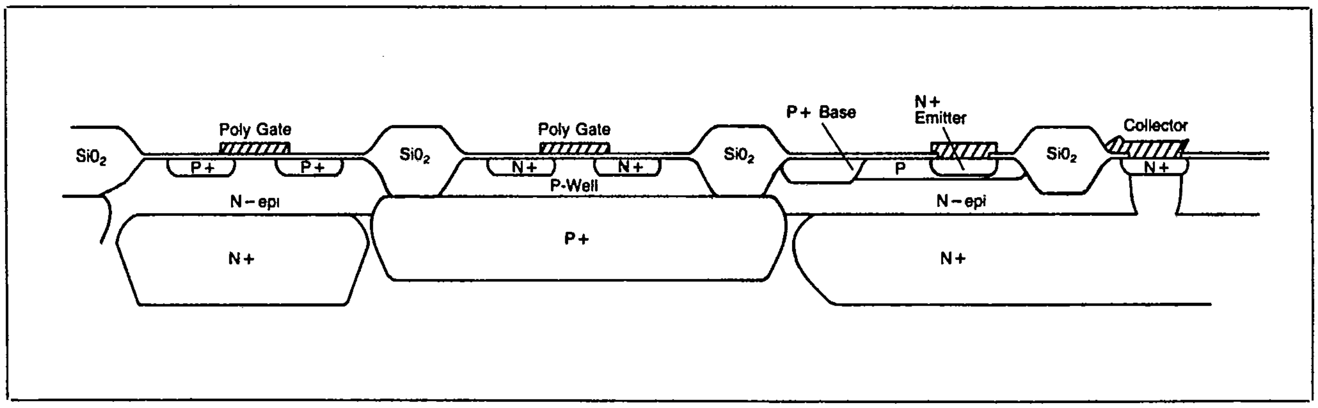


Figure 1

ARRAY ARCHITECTURE

The Q14000 Series logic arrays are comprised of both channelled and channelless architectures. While the Q2100B and Q9100B are channelled arrays, the Q6000B, Q14000B and Q28000B utilize AMCC's innovative Sea-of-Cells channelless architecture. The Sea-of- Cells organization eliminates the dedicated routing channels between cells, used in channelled array architectures, thereby increasing the core density. 100% routing capability is maintained up to 100% utilization with three levels of metal interconnect. First level metal is used primarily for macro definition while second and third level metal handle inter-macro routing.

The Q14000 Series is a true BiCMOS array. Each core cell has BiCMOS components, while the I/O is comprised primarily of bipolar construction. BiCMOS performance is not limited by I/O switching speeds. Core macros employ a bipolar totem pole configuration used to drive the next function for all macros. The I/O's are highly flexible and can be configured as an input or an output.

Both channelled and channelless arrays utilize the same logic cell. The internal logic library is common to both array architectures. However, the I/O cells between the channelled and the channelless arrays are constructed differently.

The channelled arrays have two types of I/O cells. On three sides of the array, the I/O cells can be used to implement unidirectional input or output. The remaining side of the array can implement single-cell bidirectional or unidirectional I/O functions. However, this does not restrict the number of bidirectional I/Os in the channelled arrays. Bidirectional functions can also be implemented by tying two unidirectional I/Os together. In addition, all I/O cells can implement ECL 10K, ECL 100K, TTL, CMOS or a mixture of all these technology interfaces on one chip.

The channelless arrays have only one type of I/O cell. All I/O cells implement unidirectional input or output. Bidirectional I/Os are created by tying two unidirectional I/Os together. In addition, all I/O cells can implement ECL 10K, ECL 100K, CMOS, TTL or a mixture of these technology interfaces on one chip.

Q14000B ARRAY LAYOUT
Sea-of-Cells Architecture

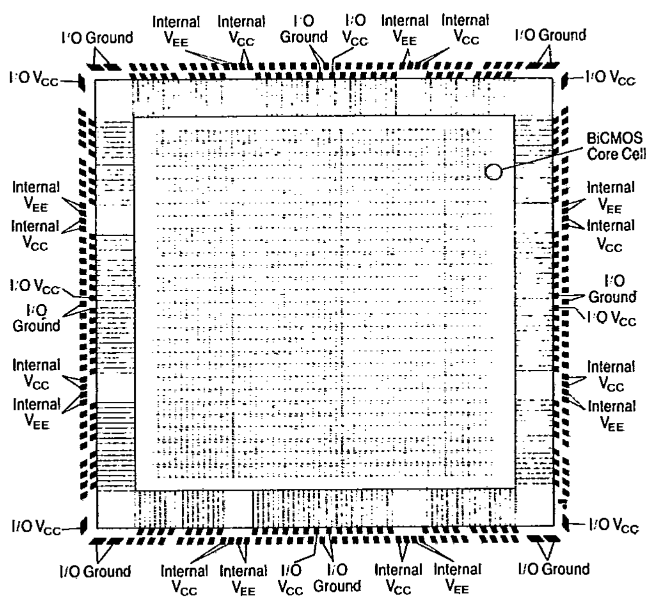


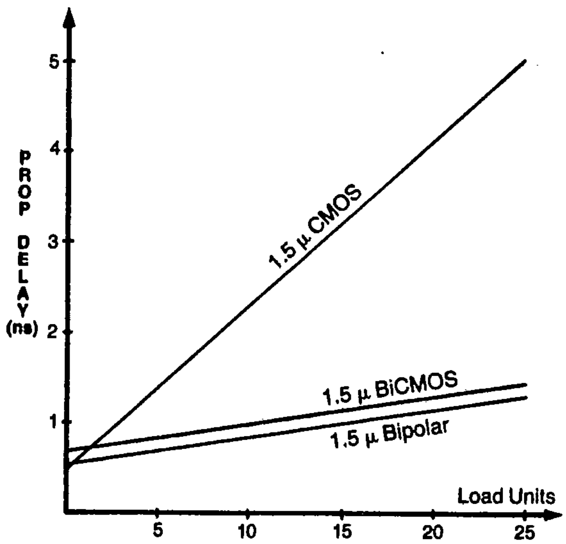
Figure 2

LOW INTERCONNECT DELAY

When considering the performance of a design, the interconnect can contribute a significant proportion of the overall delay. The performance of an internal macro is directly related to the drive, or k-factor, associated with the macro. Typical CMOS drive factors can range from 150 to 250 pS per fanout. However, each internal macro of AMCC's BiCMOS typically has loading delay penalties of 25 pS per fanout, a 6X to 10X improvement. Since the bipolar transistors used in the Q14000 Series basic cell yield drive factors 6 to 10 times lower than those of comparable CMOS transistors, BiCMOS macros experience little performance degradation as fanout loads are increased.

Another benefit to AMCC's BiCMOS is the symmetrical k-factors. Loading delays of 25 pS per fan-out applies to both rise and fall delay penalties. Typically for CMOS devices, p-channel and n-channel devices have inherently different drive factors. This contributes to uneven k-factors for rising and falling edges, further pronouncing signal skews. Uneven skews contribute to pulse width degradation of system clocks, limiting maximum system performance. BiCMOS designs can improve high performance system speeds due to the minimal loading skews.

FANOUT DEGRADATION COMPARISON



Typical Delay of 2-input NOR Gate as Function of Loading

Figure 3

HIGH DRIVE CAPABILITY

TTL output drive strengths of 8 or 20 mA from a single I/O cell are available to optimize power versus drive strength. Thus, users will no longer sacrifice I/O cells for increased drive capability. In addition, two output buffers can be used in parallel to achieve 48 mA sink current capability. Such high drive strength will allow direct interface to common bus specifications.

TTL OUTPUTS	DRIVE STRENGTH (mA)		
	8	20	48
Power (mW)	5	9/13	26

Table 3

180 MHZ PERFORMANCE

Even though shrinking geometries have dramatically increased CMOS internal switching frequencies, the I/O has not reaped the same benefit. CMOS I/O frequencies continue to be less than 100 MHz due to limitations of the I/O switching. With AMCC's BiCMOS the maximum switching frequency is not limited by the I/O since the I/O is primarily bipolar. Instead BiCMOS benefits from the high nominal internal switching frequency, yielding a frequency of 180 MHz under worst case commercial conditions.

With this performance, applications such as high resolution graphics, telecommunications, high end personal computers, workstations, and military can capitalize on ECL type speeds with extremely low power.

BICMOS INTERNAL LOGIC CELL STRUCTURE

The Q14000 Series internal logic cell utilizes both CMOS and bipolar devices. Each cell has 4 resistors, 8 CMOS transistor pairs with four bipolar transistors in a totem pole configuration. The CMOS devices are used for logic implementation while the bipolar device pairs provide necessary drive capability. With this type of core cell design, each macro benefits from the additional drive of bipolar transistors. There is very little real estate penalty from the bipolar drivers since they occupy only 10% of the entire chip area. There is only one logic cell type, simplifying the gate array design process. With such a large cell, macro functions such as D latches, 6-input ORs or Exclusive ORs can be implemented in a single cell with minimum intramacro metal delay penalty.

2 INPUT NAND SCHEMATIC

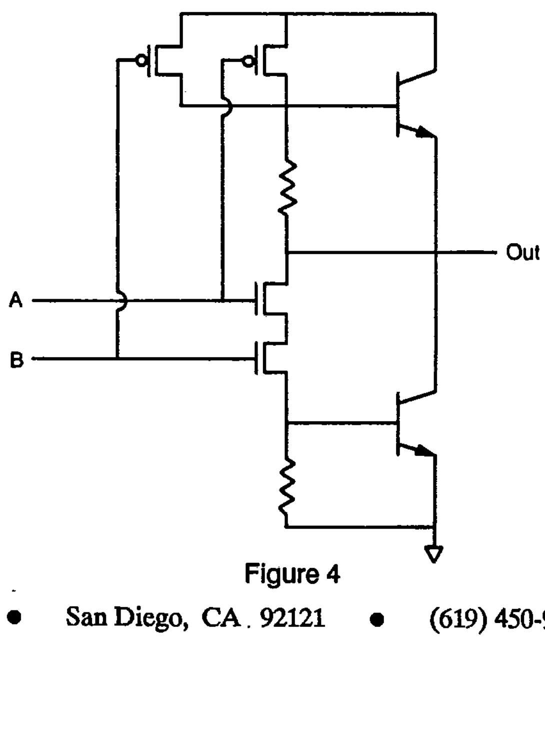


Figure 4

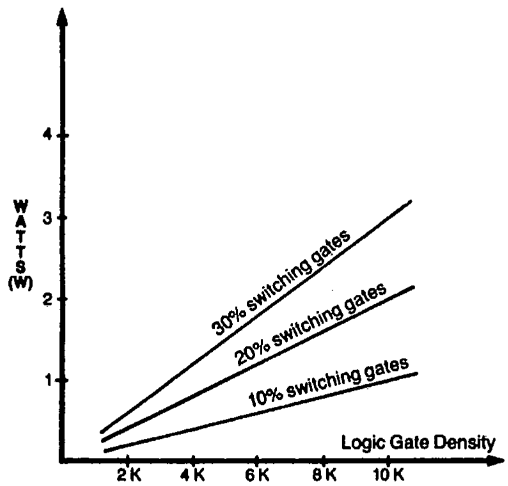
Q14000 SERIES BiCMOS LOGIC ARRAYS

POWER CONSIDERATIONS

AMCC's Q14000 Series arrays have been designed for high performance while maintaining low power dissipation. The power consumption of the internal core of a BiCMOS array is directly proportional to the number of gates switching simultaneously during a clock cycle and the operating frequency. Internal power consumption for Q14000 Series BiCMOS arrays is approximately 20μW/gate-MHz for active gates switching during the clock cycle. The core area consumes no DC power. Figure 5 plots internal power versus the percentage of simultaneously switching gates.

I/O cell power is determined by the interface mode selected and the particular macro selected. Power consumption for representative I/O macros is defined in the CMOS, ECL and TTL Interface sections of this data sheet.

TYPICAL CORE POWER DISSIPATION



Internal Power as Functions of Logic Gate Density and Percentage of Simultaneously Switching Gates (Clock Freq. = 50 MHz)

Figure 5

HIGH SPEED/LOW POWER MACROS

The Q14000 Series macro library offers maximum flexiblity in the optimization of circuit performance and power consumption. I/O macros are offered with low power, standard and high-speed options. The high speed options require somewhat more power than standard and low power but provide a significant improvement in performance.

Table 4 illustrates the effects of speed/power selections on maximum frequency versus power. As the table indicates the overall macro performance versus power consumption can be varied significantly depending upon the option selected.

The circuit designer can make the selection of speed/power options at the time of schematic capture on a supported engineering workstation. Through simulation, the designer can fine-tune the circuit to

	I/O TYPE	PARAMETER	SPEED/POWER OPTIONS[1] LOW POWER	STANDARD	HIGH SPEED
E[2]CL	INPUT	MAX FREQ (MHz)		160	180
		POWER (mw)		10	13
	OUTPUT	MAX FREQ (MHz)			180
		POWER (mw)			22
T[3]TL	INPUT	MAX FREQ (MHz)	35		65
		POWER (mw)	5		14
	OUTPUT (8mA)	MAX FREQ (MHz)	25		
		POWER (mw)	5		
	OUTPUT (20mA)	MAX FREQ (MHz)	50	65	
		POWER (mw)	8	12	

1 Maximum rating frequency under commercial conditions
2 ECL power determined at VEE = –4.5V
3 TTL outputs illustrated are used for mixed mode. 100% TTL mode macros will experience considerably lower power.

Table 4

provide the required mix of performance and power savings.

The interface macro sections of the data sheet provide additional information on speed/power trade-offs.

FLEXIBLE I/O STRUCTURE

The Q14000 Series I/O cells are configurable to provide a wide range of interface options.

The Q14000 Series arrays also offer the following special options to support various interface requirements such as high speed and +5V, single-supply ECL and TTL I/O (see Table 5). The mixed ECL/TTL capabilities allow the interface to both technologies on a single chip without the use of external translators.

FLEXIBLE I/O STRUCTURE		
INPUT	**BI-DIRECTIONAL**	**OUTPUT**
TTL	TTL transceiver	TTL totem pole
ECL 10K	ECL 10K transceiver	TTL 3-state
ECL 100K	ECL 100K transceiver	TTL open collector
CMOS	CMOS	ECL 10K
		ECL 100K
		CMOS

Table 5

PSEUDO ECL

+5V referenced ECL (PSEUDO ECL) has a number of advantages that can improve system cost and performance. First, +5V referenced ECL mixed with TTL allows a single power supply to be utilized in the system. Second, the ECL I/O can provide fast on and off chip delays. Paired ECL I/O delay can be as a fast as 2.0 nS, a 60% improvement over TTL I/O delays. Pseudo ECL is also ideal for clock lines, providing minimal skew for clock distribution trees or the capability for differentially driven inputs or differential outputs. Differential signals provide higher noise immunity. Last of all, mixed +5V ECL/TTL, systems can break the 100 MHz frequency barrier, and still maintain TTL system compatibility.

ECL INTERFACE

The Q14000 Series BiCMOS arrays can interface to standard ECL 10K and ECL 100K levels. In fact, 10K and 100K output cells can be combined in one array.

ECL outputs can leave the arrays from any I/O cell and provide 50 ohm or 25 ohm output drive. Some 50 ohm output macros incorporate simple logic functions within the I/O cell effectively providing added density.

On the channeled arrays, single cell bidirectional ECL operation is available using one-quarter of the available I/O cells. 20 and 45 ECL transceiver macros are located along one side of the Q2100B and Q9100B arrays, respectively. For the channelless arrays, bidirectional ECL is achieved by tying two I/O cells together.

TTL INTERFACE

TTL signals can enter the Q14000 Series arrays from any I/O cell. Once on-chip, TTL signals are automatically converted to internal operating levels for logic operations. TTL outputs are available in bi-state or 3-state configurations.

TTL and ECL I/O can be mixed on each array yielding three basic configurations: TTL-only, mixed ECL/TTL (dual supply) and mixed ECL/TTL (single supply). Power supply requirements for each mode of operation are shown in Table 6. Representative TTL and TTLMIX I/O configurations are summarized in Table 9.

One quarter of the I/O cells on each channelled array can be configured to allow single cell bidirectional TTL operation. All single-cell bidirectional I/O cells are located along a single side of each array. For the channelless arrays, bidirectional TTL is achieved by tying two I/O cells together.

CMOS INTERFACE

CMOS signals can enter the Q14000 Series from any I/O cell. For driving CMOS logic devices, AMCC has designed special macros which can maintain the high noise margins of CMOS but with improved drive capability of bipolar. With AMCC's BiCMOS, complete flexibility to mix CMOS, ECL and TTL can be integrated on a single chip. Translators are no longer necessary, reducing board space requirements.

I/O POWER SUPPLY CONFIGURATION		
I/O	V_{EE}	V_{CC}
ECL 100K	−4.2 to −4.8V	–
ECL 10K	−4.7 to −5.7V	–
ECL 100K/TTL	−4.2 to −4.8V	4.5 to 5.5V
ECL 10K/TTL	−4.7 to −5.7V	4.5 to 5.5V
TTL	–	4.5 to 5.5V
ECL/TTL Single Supply	4.5 to 5.5V	4.5 to 5.5V

Table 6

REPRESENTATIVE CMOS INTERFACE MACROS			
	CELLS	TYPICAL DELAY (ns)[3]	TYPICAL POWER (mW)[4]
INPUT Non-Inverting	1	6.8	7.5
OUTPUT 2 input OR	1	3.4	4.9

Table 7

REPRESENTATIVE ECL INTERFACE MACROS					
DESCRIPTION	CELLS	TYPICAL DELAY (ns)[1]		TYPICAL POWER (mW)[2]	
ECL 10K/100K		STANDARD	HIGH SPEED	STANDARD	HIGH SPEED
INPUTS Noninvert[3]	1	3.1	1.1	9.9	12.6
OUTPUTS					
2 Input OR	1	.6	–	21.8	–
25Ω Driver	2	.6	–	56.8	–
Bidirectional	1	.4	.4	32.2	34.6

Table 8

REPRESENTATIVE TTL INTERFACE MACROS								
	DESCRIPTION	CELLS	TYPICAL DELAY (ns)[3]			TYPICAL POWER (mW)[4]		
			LOW POWER	STANDARD	HIGH SPEED	LOW POWER	STANDARD	HIGH SPEED
SINGLE SUPPY	INPUTS Noninverting	1	2.1	–	–	1.0	–	–
	OUTPUTS 2 input OR	1		2.0	–	–	5.0	–
DUAL SUPPY	INPUTS Noninverting	1	3.5	–	1.3	5.5	–	13.7
	OUTPUTS 2 input OR	1		3.9	3.0	–	8.2	12.4
	3-state	1		4.1	3.2	–	14.5	18.6
	Bi-directional	1		4.4	–	–	44.5	–
	2 input OR (8mA)	1		6.6	–	–	4.6	–
	3-state (8mA)	1		7.3	–	–	7.7	–

NOTES:

1 Prop Delays are averaged, V_{EE} = −4.5V. under no load conditions.

2 At V_{EE} = −4.5V. Does not include I_{OEF}.

3 Prop Delays are averaged. V_{CC} = 5.0V, T_J = 25 °C.

4 At V_{CC} = 5.0V

Table 9

Q14000 SERIES BiCMOS LOGIC ARRAYS

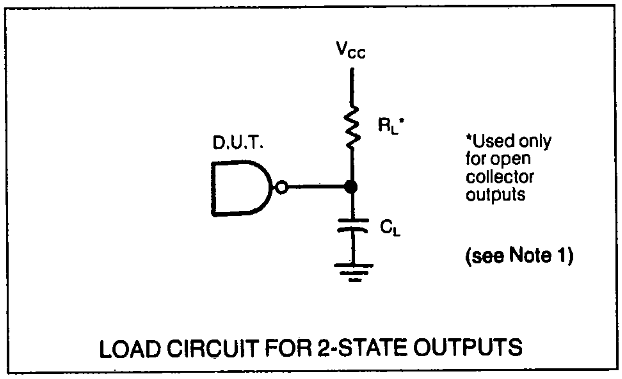


FIGURE 6

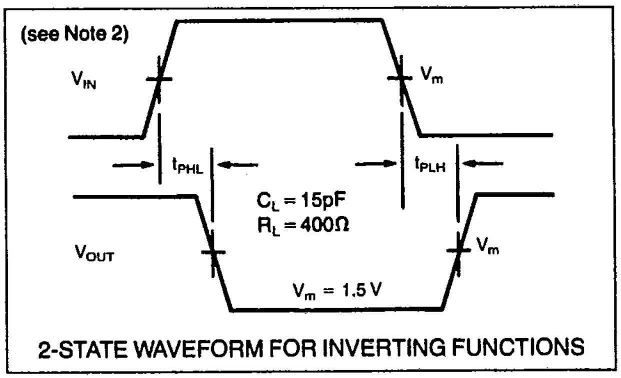


FIGURE 7

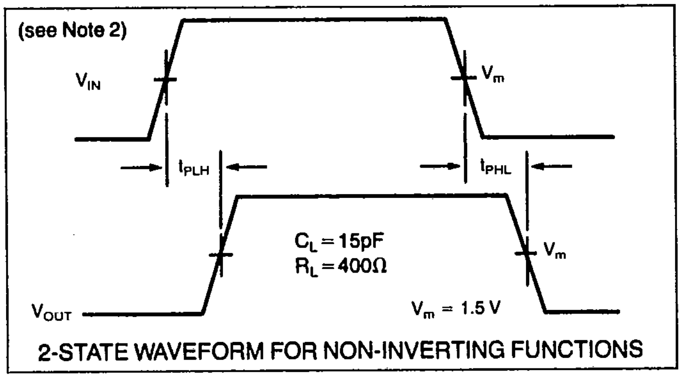


FIGURE 8

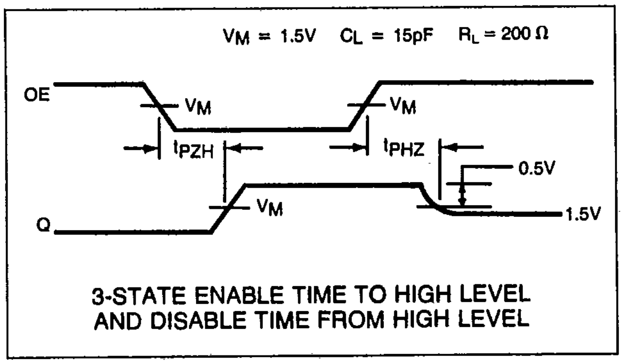


FIGURE 9

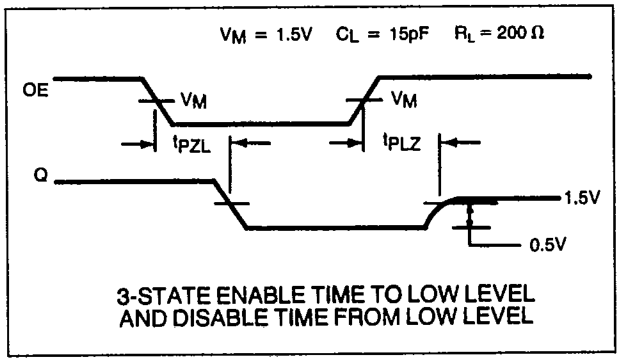


FIGURE 10

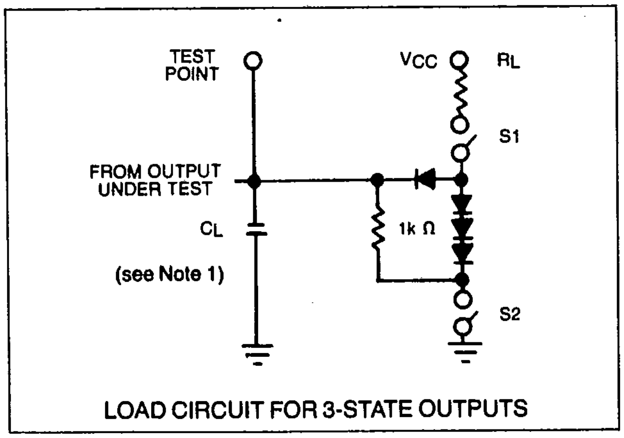


FIGURE 11

3-STATE TEST CIRCUIT SWITCH TABLE

TEST FUNCTIONS	S1	S2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

NOTES:

1 Standard TTL load circuit used for macro specification, see Figures 6 and 7. CL includes probe, jig and package.

2 V_{IN} = 0 to 3.0 volts.

Table 10

INTERNAL LOGIC CELL CAPABILITIES

The Q14000 Series internal logic cells are all identical in structure and are positioned in uniform columns across the arrays. Each cell contains 16 CMOS and 4 bipolar uncommitted transistors along with 4 resistors. The cells are individually configurable to provide a variety of logic functions through the use of the Q14000 Series macro library. The macro library provides SSI, MSI and some basic LSI functions. The higher level macros provide the advantages of higher speed, lower power and increased circuit density over a logically equivalent SSI macro implementation.

Table 11 lists parameters for a number of representative Q14000 Series internal macros.

REPRESENTATIVE INTERNAL MACROS						
DESCRIPTION	NUMBER OF CELLS	TYPICAL DELAY (ns)1		LOADED DELAY (ns)2		
		tpLH	tpHL	tpLH	tpHL
2-Input NAND (DUAL)	1	.63	.40	.87	.64
3-Input NAND	1	.77	.48	1.01	.72
4-Input NAND	1	.79	.61	1.03	.90
2-Input NOR (DUAL)	1	1.15	.36	1.44	.60
3-Input NOR	1	1.52	1.25	1.76	1.49
4-Input NOR	1	1.64	1.36	1.93	1.60
Exclusive OR	1	.90	.60	1.14	.84
Exclusive NOR	1	.88	.61	1.17	.85
Latch with Reset					
D →Q	1	1.51	1.58	1.75	1.79
D →$\overline{Q}$		.91	1.11	1.15	1.35
C →Q		2.81	2.78	3.05	3.02
C →$\overline{Q}$		2.31	2.21	2.55	2.45
D F/F with Reset					
C →Q	2	1.47	1.43	1.71	1.67
C →$\overline{Q}$		2.45	2.02	2.69	2.26
4 : 1 Mux					
Data →Y	2	1.85	2.25	2.14	2.49
Select →Y		1.92	1.63	2.21	1.87

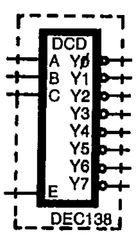
NOTES:
1 Driving no loads
2 Driving 4 loads plus 4mm of metal

Table 11

HARD MSI MACROS

In addition to basic macros, the Q14000 Series incorporates hard MSI macros for faster, more efficient designs. MSI macros can decrease design time by using large building-blocks rather than one-cell macros. Hard MSI macros are customized transistor level implementation of complex functions as opposed to "soft macros", which are gate-level implementation through logic equivalence. AMCC's hard macros have a distinct advantage over "soft macros" by 1) improving density in utilizing more transistors per cell 2) performance improvement due to optimized metal interconnect and 3) predictable delay characteristics from pre-determined layout constraints.

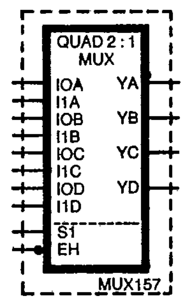
TYPICAL MSI MACROS



3 : 8 DECODER WITH ENABLE (6 CELLS)

DELAY PATH	TYPICAL DELAY (ns)1		LOADED DELAY (ns)2	
	tpLH	tpHL	tpLH	tpHL
A, B, C →Y	1.60	1.44	1.84	1.68
Enable →Y	1.76	1.41	2.00	1.65

NOTES:
1 Driving no loads
2 Driving 4 loads plus 4mm of metal



QUAD 2 : 1 MUX (4 CELLS)

DELAY PATH	TYPICAL DELAY (ns)1		LOADED DELAY (ns)2	
	tpLH	tpHL	tpLH	tpHL
I0, I1 →Y	1.34	1.61	1.58	1.85
S1 →Y	2.52	2.69	2.76	2.93

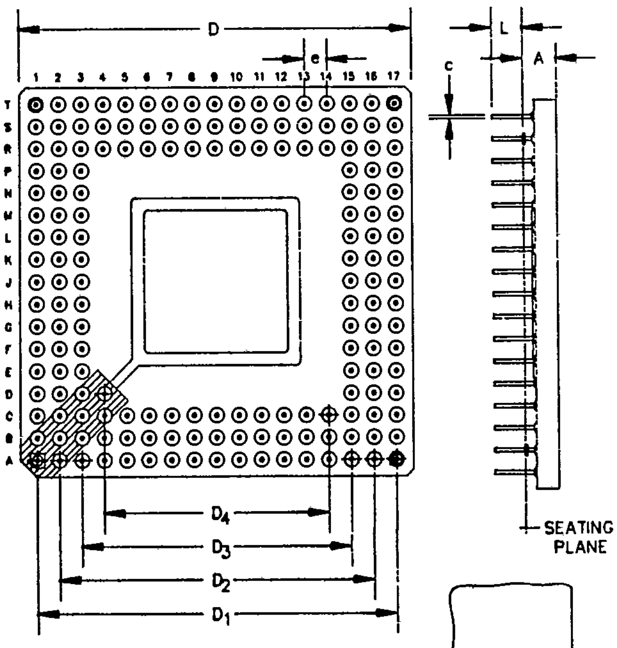
Q14000 SERIES BiCMOS LOGIC ARRAYS

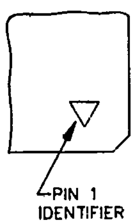
PACKAGING

The Q14000 Series logic arrays are available in a broad range of standard packages including surface mount chip carriers and pin grid arrays. Each package is custom designed by matching the bond finger layout to the power and ground locations of each AMCC BiCMOS array. Special attention has been paid to minimizing resistances and inductance on power and ground pins by using multi-layer construction for package power and ground planes. In addition, capacitance on signal pins has been minimized while consideration for low thermal resistance is designed into each BiCMOS package. For more details consult the AMCC Packaging Guide.

Sym.	Inches (mm)	
	Max.	Min.
A	.155 (3.94)	.145 (3.68)
c	.020 (0.51)	.016 (0.41)
D	1.768 (44.91)sq.	1.732 (43.99)sq.
D_1	1.605 (40.77)sq.	1.595 (40.51)sq.
D_2	1.405 (35.69)sq.	1.395 (35.43)sq.
D_3	1.205 (30.61)sq.	1.195 (30.35)sq.
D_4	1.005 (25.53)sq.	.995 (25.27)sq.
e	.105 (2.67)	.095 (2.41)
L	.145 (3.68)	.115 (2.92)
S	.085 (2.16)sq.	.065 (1.65)sq.

Table 12





169 PGA Cavity Down

PACKAGING TABLE

PACKAGE	REMARKS	Q2100B	Q6000B	Q9100B	Q14000B	Q28000B
Leaded Chip Carriers						
84 Flatpack	50 mil ctr	X				
100 LDCC	50 mil ctr	X				
132 LDCC	25 mil ctr			X	X	
172 LDCC	25 mil ctr		P			
196 LDCC	25 mil ctr			X	X	
340 LDCC	20 mil ctr					P
Pin Grid Arrays						
68 PGA	CD	X				
84 PGA	CD	X				
100 PGA	CD	X	X			
169 PGA*	CD		X	X	X	
225 PGA*	CD			X	X	
301 PGA*	CD				X	
364 PGA	CD					P

* Includes 1 orientation pin.
P Planned

Table 13

PAD TO PIN INTERCONNECTION LIST

PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN
1	B2	35	T2	69	P15	103	B15	VCC	C5	VSS	C8
2	B1	36	R4	70	R16	104	A15		C13		C10
3	D3	37	S3	71	R17	105	B14		E3		H3
4	C2	38	T3	72	P16	106	A14		E15		H15
5	C1	39	S4	73	P17	107	B13		N3		K3
6	D2	40	T4	74	N16	108	A13		N15		K15
7	D1	41	S5	75	N17	109	B12		R5		R8
8	E2	42	T5	76	M16	110	A12		R13		R10
9	E1	43	S6	77	M17	111	B11				
10	F2	44	T6	78	L16	112	A11	VDD	F3	VEE	C7
11	F1	45	S7	79	L17	113	B10		J3		C11
12	G2	46	T7	80	K16	114	A10		M3		G3
13	G1	47	S8	81	K17	115	B9		R6		G15
14	H2	48	T8	82	J16	116	A9		R9		L3
15	H1	49	S9	83	J17	117	B8		R12		L15
16	J2	50	T9	84	H16	118	A8		M15		R7
17	J1	51	S10	85	H17	119	A7		J15		R11
18	K2	52	T10	86	G17	120	B7		F15		
19	K1	53	T11	87	G16	121	B6		C12		
20	L1	54	S11	88	F16	122	A6		C9		
21	L2	55	S12	89	F17	123	A5		C6		
22	M2	56	T12	90	E17	124	B5				
23	M1	57	T13	91	E16	125	A4				
24	N1	58	S13	92	D17	126	B4				
25	N2	59	T14	93	D16	127	A3				
26	P1	60	S14	94	C17	128	C4				
27	P2	61	T15	95	C16	129	B3				
28	R1	62	R14	96	D15	130	A2				
29	R2	63	S15	97	B17	131	C3				
30	P3	64	T16	98	B16	132	A1				
31	S1	65	T17	99	C15						
32	S2	66	R15	100	A17						
33	R3	67	S16	101	A16						
34	T1	68	S17	102	C14						

DESIGN INTERFACE

AMCC has structured its circuit design interface to provide maximum flexibility without compromising design correctness. For implementations using an engineering workstation, AMCC provides MacroMatrix software. MacroMatrix works in conjunction with the most popular workstations to provide the following capabilities.

- Schematic Capture
- Logic Simulation
- Pre-Layout Delay Estimation
- Array and Technology-Specific Rules Checks
- Estimated Power Computation
- Preliminary Package Pinouts

Upon submission of the design database to AMCC, a comprehensive review of the circuit is performed making use of the same EWS and MacroMatrix tools used by the designer. No translation of the logic data is required so the chance of non design-related errors is virtually eliminated.

CUSTOM MACROS

To further enhance the functionality of the Q14000 Series macro library, AMCC has developed MDS. Macro Development System (MDS) uses a "correct by construction" approach to develop macros that meet all the pertinent design rules. As individual circuit applications warrant, macros with unique characteristics can be developed rapidly and used to optimize the array design.

BICMOS EVALUATION KIT

AMCC has developed the BICMOS Evaluation Kit to facilitate reliable assessment of the Q14000 Series BICMOS Logic Arrays. The Evaluation Kit consists of a Q2100B Design Verification Chip, multi-layer high performance board, miniature coax cables and 50-ohm input terminators. The user need not develop a test board or special hardware to use the Evaluation Kit. Evaluation features include:

- ECL I/O Pair Delay
- TTL I/O Pair Delay
- D Flip-Flop Toggle Frequency
- D Flip-Flop Set-Up and Hold Time
- Ring Oscillators for Internal Macro Delays
- Fanout Delay Loading Penalty
- Metal Delay Loading Penalty
- Simultaneous Switching Outputs

Evaluation Kits are available through AMCC's Regional Sales Manager.

AMCC DESIGN SERVICES

In addition to supporting design work at the designer's location, AMCC also offers customers the option of working at the San Diego Design Center. At the Design Center, engineers have access to the same sophisticated CAE/CAD tools supported for customer site designs plus direct contact with a dedicated applications engineer to assist with the array implementation.

AMCC also provides a number of additional support services including:

- Full Design Implementation Service
- Local and Factory Applications Engineering Support
- Comprehensive Training Courses
- Complete Design Documentation

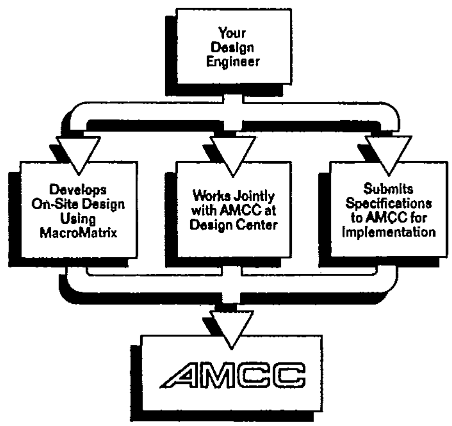


FIGURE 12

RELIABILITY

Reliability is created through stringent design reviews followed by vigorous characterization and qualification testing of new products and processes. Prior to building first customer designs, AMCC institutes high temperature operating life testing to achieve a high equivalent number of device hours. During production, life testing and thermal stress testing are run on production released designs to ensure that reliability of the proven design is maintained. The ongoing Rel Program monitors the quality and reliability of production released products manufactured by AMCC. Samples are chosen from normal military and commercial hi-rel production device runs. From the accumulated data, device family reliability data can be estimated by using the Arrhenius equation model. Specific information about test conditions and activation energy assumptions are available from AMCC's reliability brochure.

Q14000 SERIES BiCMOS LOGIC ARRAYS

RECOMMENDED OPERATING CONDITIONS - COMMERCIAL				
PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE}) $V_{CC}=0$				
10K, 10KH Mode	−4.94	−5.2	−5.45	V
100K Mode	−4.2	−4.5	−4.8*	V
ECL Input Signal Rise/Fall Time	–	1.5	5.0	ns
TTL Supply Voltage (V_{CC})	4.75	5.0	5.25	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	0 (ambient)		70 (ambient)	°C
Junction Temperature			130	°C

RECOMMENDED OPERATING CONDITIONS - MILITARY				
PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE}) $V_{CC}=0$				
10K, 10KH Mode	−4.7	−5.2	−5.7	V
100K Mode	−4.2	−4.5	−4.8*	V
ECL Input Signal Rise/Fall Time	–	1.5	5.0	ns
TTL Supply Voltage (V_{CC})	4.5	5.0	5.5	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	−55 (ambient)		125 (case)	°C
Junction Temperature			150	°C

* −5.7V is possible. Consult AMCC for ECL 100K DC parametrics oprating at this voltage.

ABSOLUTE MAXIMUM RATINGS	
ECL Supply Voltage V_{EE} (V_{CC} = 0)	−8.0 VDC
ECL Input Voltage (V_{CC} = 0)	GND to V_{EE}
ECL Ouput Source Current (continuous)	−50mA DC
TTL Supply Voltage V_{CC} (V_{EE} = 0)	7.0 V
TTL Input Voltage (V_{EE} = 0)	5.5 V
Operating Temperature	−55°C (ambient) to +125°C (case)
Operating Junction Temperature T_J	+150°C
Storage Temperature	−65°C to +150°C

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	COM 0°/+70°C MIN	TYP	MAX	MIL −55°/+125°C MIN	TYP	MAX	UNIT
t_{IPD}-ECL	ECL Input Propagation Delay Including Buffer	Standard	3 loads		3.2	4.3		3.2	4.6	ns
		High Speed	3 loads		1.2	1.6		1.2	1.7	ns
t_{IPD}-TTL	TTL Input Propagation Delay Including Buffer (Std.)	Low Power	3 loads		3.5	4.7		3.5	5.1	ns
		High Speed	3 loads		1.3	1.8		1.3	1.9	ns
t_{OPD}-ECL	ECL Output Propagation Delay				0.6	0.8		0.6	0.9	ns
t_{OPD}-TTL	TTL Output Propagation Delay	Standard	15 pf		4.7	6.3		4.7	6.8	ns
		High Speed	15 pf		3.8	5.2		3.8	5.5	ns
t_{FPD}	Internal Gate Delay		2 loads +2mm of metal		0.52	0.81		0.52	1.01	ns
F_{maxt}	Maximum Internal Flip/Flop Toggle Frequency				240	180		240	165	MHz
F_{in}-ECL	ECL Input Frequency at Package Pin	Standard	3 loads		220	160		220	135	MHz
		High Speed	3 loads		240	180		240	165	MHz
F_{out}-ECL	ECL Output Frequency at Package Pin		50Ω		240	180		240	165	MHz
F_{in}-TTL	TTL Input Frequency at Package Pin	Low Power	3 loads		55	35		55	30	MHz
		Standard	3 loads		90	65		90	60	MHz
F_{out}-TTL	TTL Output Frequency at Package Pin	Low Power	15 pf		70	50		70	45	MHz
		Standard	15 pf		90	65		90	60	MHz
t_{PZH}	Enable time to high level		Fig. 9		9	12.3		9	13.0	ns
t_{PZL}	Enable time to low level		Fig. 10		9	12.3		9	13.0	ns
t_{PHZ}	Disable time from high level		Fig. 9		9	12.3		9	13.0	ns
t_{PLZ}	Disable time from low level		Fig. 10		9	12.3		9	13.0	ns

All AC characteristics are for channelled arrays. The channelless arrays may vary slightly.

Q14000 SERIES BICMOS LOGIC ARRAYS

T-42-11-15

ECL 10K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -5.2V$[1]

	$T_{ambient}$				T_{case}	
	−55°C	0°C	25°C	75°C	125°C	UNIT
V_{OHmax}	V_{cc}−850	V_{cc}−770	V_{cc}−730	V_{cc}−650	V_{cc}−575	mV
V_{IHmax}[5]	V_{cc}−800	V_{cc}−720	V_{cc}−680	V_{cc}−600	V_{cc}−525	mV
V_{OHmin}	V_{cc}−1080	V_{cc}−1000	V_{cc}−980	V_{cc}−920	V_{cc}−850	mV
V_{IHmin}[5]	V_{cc}−1255	V_{cc}−1145	V_{cc}−1105	V_{cc}−1045	V_{cc}−1000	mV
V_{ILmax}[5]	V_{cc}−1510	V_{cc}−1490	V_{cc}−1475	V_{cc}−1450	V_{cc}−1400	mV
V_{OLmax}	V_{cc}−1655	V_{cc}−1625	V_{cc}−1620	V_{cc}−1585	V_{cc}−1545	mV
V_{OLmin}	V_{cc}−1980	V_{cc}−1980	V_{cc}−1980	V_{cc}−1980	V_{cc}−1980	mV
V_{ILmin}[5]	V_{cc}−2000	V_{cc}−2000	V_{cc}−2000	V_{cc}−2000	V_{cc}−2000	mV
I_{IH}[2]MAX	30	30	30	30	30	µA
I_{IL}[2]MAX	−.5	−.5	−.5	−.5	−.5	µA

ECL 100K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -4.5V$[3]

SYMBOL	PARAMETER	TEST DC CONDITIONS	COMM 0°/+70°C			MIL −55°/+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	Output Voltage HIGH	Loading is 50 Ohms to −2V	V_{CC}−1035		V_{CC}−850	V_{CC}−1080		V_{CC}−835	mV
V_{OL}	Output Voltage LOW	Loading is 50 Ohms to −2V	V_{CC}−1830		V_{CC}−1605	V_{CC}−1880		V_{CC}−1595	mV
V_{IH}	Input Voltage HIGH	Maximum input voltage HIGH	V_{CC}−1145		V_{CC}−800	V_{CC}−1145		V_{CC}−800	mV
V_{IL}	Input Voltage LOW	Maximum input voltage LOW	V_{CC}−1950		V_{CC}−1475	V_{CC}−1950		V_{CC}−1475	mV
I_{INL}[2]	Input Current LOW	$V_{IN} = V_{ILmin}$			−0.5			−0.5	µA
I_{IH}[2]	Input Current HIGH	$V_{IN} = V_{IHmax}$			30			30	µA

TTL INPUT/OUTPUT DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST DC CONDITIONS		COMM 0°/+70°C			MIL −55°/+125°C			UNIT
				MIN	TYP[4]	MAX	MIN	TYP[4]	MAX	
V_{IH}[5]	Input voltage HIGH	Guaranteed input HIGH voltage for all inputs		2.0			2.0			V
V_{IL}[5]	Input voltage LOW	Guaranteed input LOW voltage for all inputs				0.8			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = −18mA			−.8	−1.2		−.8	−1.2	V
V_{OH}	Output voltage HIGH	V_{CC} = Min, I_{OH} = −1mA		2.7	3.4		2.4	3.4		V
V_{OL}	Output voltage LOW	V_{CC} = Min	I_{OL} = 8mA			0.5			0.5	V
			I_{OL} = 20mA			0.5			0.5	V
						0.6			0.6	V
I_{OZH}	Output "off" current HIGH (3-state)	V_{CC} = Max, V_{OUT} = 2.4V		−50		50	−50		50	µA
I_{OZL}	Output "off" current LOW (3-state)	V_{CC} = Max, V_{OUT} = 0.4V		−50		50	−50		50	µA
I_{IH}	Input current HIGH	V_{CC} = Max, V_{IN} = 2.7V				50			50	µA
I_I	Input current HIGH at Max	V_{CC} = Max, V_{IN} = 5.5V				1.0			1.0	mA
I_{IL}[6]	Input current LOW	V_{CC} = Max, V_{IN} = 0.5V				50			50	µA
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} = 0.5V		−25		−100	−25		−100	mA

1 Data measured with V_{EE} = −5.2 ± .1V (or V_{CC} = 5.0 ± .1V for +5V ref. ECL 10K) assuming a +50°C rise between ambient (T_a) and junction temperature (T_J) for −55°C, 0°C, +25°C, and +70°C, and a +25°C rise for +125°C. Specifications will vary based upon T_J. See AMCC Packaging and Design Guides concerning V_{OH} and V_{OL} adjustments associated with T_J for packages and operating conditions.

2 Per fan-in.

3 Data measured at thermal equilibrium, with maximum T_J not to exceed recommended limits. See AMCC Packaging Guide to compute T_J for specific package and operating conditions. For +5V ref. ECL 100K, V_{OH} and V_{OL} specifications will vary based upon power supply. See AMCC Design Guide for adjustment factors.

4 Typical limits are at 25°C, V_{CC} = 5.0V.

5a These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

5b Use extreme care in defining input levels for dynamic testing. Many outputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for dynamic TTL testing and V_{ILMIN} and V_{IHMAX} for ECL testing.

6 For standard speed options only.