AMCC
APPLIED MICRO CIRCUITS CORPORATION

Q14000 RAPID REFERENCE

(803)

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Q14000 RAPID REFERENCE

This document is not intended as a replacement for the Q14000 Series Design Manual, class note set or the design guide. It is intended to provide the designer with a compact easy cross-reference to the tables for all BiCMOS arrays in the series to allow design decisions affecting the selection of an array within the series. These decisions include operating speed, sizing, population, macro options, power, maximum current, loading and fan-out limits.

The assumption is that the designer has previously reviewed:

- The Design Manual for the Q14000
- The Design Submission Document for the EWS or for AMCC Implemented Design Submission
  Design Manual Vol II, Sec 6.
- AMCC EWS Schematic Rules and Conventions
  Design Manual Vol II, Sec 3 and Sec 7.
- AMCC Vector Submission Rules and Guidelines
- BiCMOS Design Validation
  Design Manual Vol II, Sec 4.

EQUIVALENT GATES

An equivalent gate is defined as a 2-input NAND gate for the BiCMOS arrays. A measure of design density is the number of these gates that would be required to construct the design in SSI logic. The number of equivalent gates is also a sizing measure for the AMCC logic arrays.

SIZES OF THE AMCC BiCMOS ARRAYS

ARRAY NAME	EQUIVALENT GATES
Q9100B	9072
Q2100B	2160

The actual circuit density obtained is a function of the design objectives, design approach and macros selected.

A denser design is possible if the more complex macros are used first - MSI level and other cell-efficient, dense macros - keeping the use of SSI-level AND, OR, NOR, NAND gates to a minimum. Balanced delay paths use more cells than a minimized design; high-speed designs may use more cells if heavily loaded paths are to be broken up into parallel structures.

MAXIMUM OPERATING FREQUENCY

The maximum operating frequency is specified as the maximum I/O switching rate for an I/O macro or the maximum internal toggle rate for an internal macro. The actual speed at which a circuit may operate must be computed from a worst-case critical-path timing analysis and must include the intrinsic macros delays (specified as "Tpd" in the macro documentation) and the extrinsic loading delays as computed using Back-Annotation.

MAXIMUM OPERATING FREQUENCY

TYPE OF I/O:	OPTION:	COM MAX LIMIT MHz	MIL MAX LIMIT MHz	PLACE f ON I/O LIST WHEN f > MHz
TTL INPUT	S	65	60	60
TTL INPUT	H	90	85	60
TTL OUTPUT	S	50	45	35
TTL OUTPUT	H	65	60	35
ECL INPUT	S	110	100	100
ECL INPUT	H	180	165	120
ECL OUTPUT	S	110	100	100
	H	180	165	120
INTERNAL MACRO	S	180	165	

For the hierarchical macros, refer to the individual maximum frequency of operation specification within the macro library documentation.

For I/O macros, the toggle frequency should be added to the I/O list in the appropriate column only when the frequency exceeds that listed in the right column. This will allow proper high-speed design validation to be performed by AMCC. The I/O list is generated as AMCCIO.LST by the MacroMatrix software.

INTERNAL RESOURCES

In selecting an array, one of the first sizing considerations is the number and type of internal cells and interface cells available.

The internal matrix area of the BiCMOS arrays is restricted to basic (B) cells.

ARRAY CELL RESOURCE SUMMARY

array	cells	I/O	External PINS	Bidirec. I/O **	% util.	die size
Q9100B	2268	160	216	40	95%	415 x 410
Q2100B	540	80	108	20	95%	255 x 245

** Bidirectional I/O macros are limited to the number shown and MUST ALL be placed on the LEFT side of the array. The total I/O count includes the bidirectional limit. The external pin count includes the I/O pins and the fixed power and ground pins.

Internal cell usage is reported by the population ERC.

I/O RESOURCES - IN GENERAL

The flexible I/O of the AMCC Logic Arrays allow a broad selection of interfaces. TTL, ECL, TTL/ECL, +5V REF ECL, +5V REF ECL/TTL with either ECL 10K or ECL 100K are among the modes supported (consult the individual library for specific limitations). TTL totem pole, open-collector and three-stated outputs are also supported as are ECL terminations of 50ohms.

The number of fixed power and ground pins for a given I/O mode and a given array is displayed on the chip macro for that array and I/O mode.

Cell and pin usage is reported by the population ERC.

ECLCOREVCC, ECLIOVCC and VDD are 0V for standard reference ECL 10K or ECL 100K. They are +5V for +5V REF ECL 10K or 100K. ECLCOREVEE and VSS are -4.5V for ECL 100K, -5.2V for ECL 10K or 0V for +5V REF ECL 10K or 100K.

Q14000 SERIES CELL RESOURCES

Cells and Pins:	Q9100B	Q2100B	
EXTERNAL PINS:	216	108	
Bidirectional I/Os:	40	20	
I/O Cells	160	80	(includes Bidi)
Logic Cells	2268	540	

Q14000 SERIES POWER AND GROUND RESOURCES

MODE	DESCRIPTION	Q9100B	Q2100B
TTL	I/O Cells	160	80
SYSTEM	V_{CC} (+5V)	32	16
	GROUND	24	12
ECL	I/O Cells	160	80
SYSTEM	V_{CC} **	40	20
any	V_{EE} *	16	8
MIXED	I/O Cells	160	80
TTLMIX	V_{CC} (+$5V_{DC}$ NOM)	8	4
and ECL	V_{EE} *	16	8
SYSTEM	TTL GROUND	8	4
	ECL V_{CC} **	24	12
MIXED			
+5V	I/O cells	160	80
SYSTEM	V_{CC} (+$5V_{DC}$ NOM)	32	16
	GROUND	24	12

* V_{EE} is -5.2V FOR STD-REF ECL 10K
-4.5V FOR STD-REF ECL 100K
0V FOR +5V REF ECL 10K OR ECL 100K

** V_{CC} is 0V FOR STD-REF ECL 10K
0V FOR STD-REF ECL 100K
+5V FOR +5V REF ECL 10K OR ECL 100K

ADDING EXTRA POWER AND GROUND

The Q14000 Series Logic Arrays require that extra power and ground be added when the number of simultaneously switching TTL or ECL outputs exceeds eight (8) for any QUADRANT of the array. Add an ITPWR - ITGND pair for each group of eight TTL simultaneously switching outputs after the first eight in the quadrant. Add an IEVCC for each group of eight simultaneously switching ECL outputs after the first eight in the quadrant. Refer to the table below.

The simultaneously switching ERC check evaluates added power and ground requirements due to simultaneously switching outputs. The design must use the /SWGROUP parameter.

Q14000 SERIES;
ADDITIONAL POWER/GROUND

# OF SIMULTANEOUSLY SWITCHING TTL PER QUADRANT		ADD TTL V_{CC} - TTL GROUND PAIRS (2 pads)
TTL in any system; 100% TTL or mixed mode	0 - 8	0
	9 - 16	1
	17 - 24	2
	25 - 32*	3

# OF SIMULTANEOUSLY SWITCHING ECL PER QUADRANT		ADD ECL VCC:
ECL in any system; 100% ECL or mixed mode	0 - 8	0
	9 - 16	1
	17 - 24	2
	25 - 32	3
	33 - 40*	4

* There is a MAXIMUM of 40 I/O cells per quadrant that may be used for outputs in the largest array (the Q9100B).

EXTRA POWER AND GROUND MACROS

Place on the schematics according to the EWS Schematics Rules and Conventions:

SERIES:	TTL V_{CC}	TTL GND	ECL VCC
Q14000 Series	ITPWR	ITGND	IEVCC

The population ERC reports on added power and ground usage. The AMCCIO.LST report contains a summary of simultaneously switching outputs, provided that the macro parameter /SWGROUP is used for all groups of simultaneously switching output macros and all added power and ground macros added to accomodate those groups.

MAXIMUM INTERNAL CELL UTILIZATION

Internal cell utilization is one means of estimating the feasibility of a design on a given array. The specified cell utilization limit is designed as a sizing guideline. Designs meeting the restrictions are felt to be routable designs, provided they also satisfy internal pin count limits. The cell utilization refers to the internal array matrix only and should not be considered to be the only population check.

INTERNAL CELL UTILIZATION LIMITS

Array	%
Q9100B	95
Q2100B	95

Cell utilization is reported by the population ERC.

INTERNAL PIN COUNT LIMIT

The internal cell utilization limit is a guideline for the routability of an array. A more specific check on routability is the internal pin count.

- An array is routable if the number of internal pins that must be routed does not exceed the maximum pin count limit.
- It is considered to be a RISKY design if the number of pins is up to +10% over the maximum pin count limit.
- It is considered to be an EXTREMELY RISKY design if the number of pins is from +11% to +18% over the maximum pin count limit.
- A design is UNACCEPTABLE if the number of pins is ≥+18% over the maximum allowed pin count.

MAXIMUM INTERNAL PIN-COUNT

Array	Actual Limit	Estimated Limit
Q9100B	8000	7300
Q2100B	2200	2160

The AMCC MacroMatrix internal pin count ERC reports the internal pin count.

ESTIMATING INTERNAL PIN-COUNT

If the number of internal pins that must be routed (pin-count) is not available for a design in its early stages (prior to capture), estimate it by the following guidelines.

SERIES	MACRO	PINS
Q14000	Internal	8
	I/O	1.5

Do not count external pins or pins connected to pads

Q14000 Series hierarchical macros state their pin count (refer to the macro summary, Design Manual Volume I, Section 6).

FAN-OUT RESTRICTIONS

The individual macro electrical fan-out load limits are specified in the Design Manual, Volume I, Section 6. The fan-out ERC checks for excessive fan-out loading.

Derating breakpoint: 100 MHz. Derate all clock lines and distortion sensitive paths by 20% for speeds below the breakpoint and by 40% for speeds at or above the breakpoint. Derating requirements are discussed in Volume I, Section 2.

The fan-out ERC will check for a derated fan-out load limit if the FOD net parameter has been used.

HIGH-CAPACITIVE LOADING ON OUTPUT MACROS - ALL ARRAYS

ECL and TTL output macros are specified with NO CAPACITIVE loading on the macros. All capacitive loads must be computed for the delay calculations.

CAPACITIVE LOAD DELAY (TYPICAL)	
ECL	45ps/pf
TTL	55ps/pf

The capacitive load delay should be added to the path delay and the total sum multiplied by the appropriate worst-case timing multiplier to find the worst-case delay.

A future MacroMatrix release will include k-factors for the output macros and load-delay macros that can be incorporated into the schematic to allow automatic delay computation.

PROPAGATION DELAY MULTIPLICATION FACTORS

All of the tables shown in this reference (Front-Annotation L_{net}, k-factors, external capacitive load delays) and all of the macro propagation delay specifications given in the design guides and design manuals provide typical propagation delays. To perform worst-case timing analysis, the following worst-case multipliers must be used.

WORST-CASE MULTIPLICATION FACTORS

Circuit Classification:	Multiplication Factor (M.F.)	MACRO TYPE:
Nominal	1.00	ANY
Commercial *	1.55	internal
Commercial *	1.35	interface (I/O)
Military **	1.95	internal
Military **	1.45	interface (I/O)
Minimum ***	0.70*	ANY

* $T_j \leq 130^{o}C$

** $T_j \leq 150^{o}$ C

*** Guideline only; not guaranteed; user must state requirements.

WORST-CASE MULTIPLIERS FOR FRONT- AND BACK-ANNOTATION FOR INTRINSIC AND EXTRINSIC PROPAGATION DELAYS

Array Series:		Q14000 internal	I/O
MINIMUM	minimum	0.70	0.70
	typical	0.78	0.78
	maximum	0.86	0.86
NOMINAL	minimum	0.90	0.90
	typical	1.00	1.00
	maximum	1.10	1.10
COMMERCIAL	minimum	1.27	1.11
	typical	1.41	1.23
	maximum	1.55	1.35
MILITARY	minimum	1.59	1.19
	typical	1.77	1.32
	maximum	1.95	1.45

- The internal multipliers apply to the intrinsic and extrinsic internal macro delays (to the k drive factors). All internal net delays use the internal logic worst-case multipliers. The interface macro multipliers apply to the interface macro delays and to external capacitive load delays.

- maximum = 1.1 * typical; minimum = 0.9 * typical for all operating conditions.

WORST-CASE MULTIPLICATION FACTORS

The worst-case multipliers for annotated simulations take into account the following:

- Process variations;
- Temperature variations;
- Voltage variations;

and apply to both the intrinsic macro delays (t_{in} = Tpd) and the extrinsic loading delays (t_{ex}).

- For each net, the AMCC MacroMatrix Front-Annotation software computes an ESTIMATED metal delay based on the size of the net and combines this with the actual delay due to fan-out loading and any wire-OR present in the net.

- For each net, the Back-Annotation software uses the post-layout file to insert the ACTUAL metal delay and combines this with the actual delay due to fan-out loading and any wire-OR present in the net.

COMMERCIAL SPECIFICATION

Commercial worst-case multipliers are for 0°C ambient to 70°C ambient with ±5% power supply variation and a junction temperature ≤130°C. Violation of any of these parameters requires the use of the MILITARY timing multipliers.

MILITARY SPECIFICATION

Military worst-case multipliers are for -55°C ambient to +125°C case with ±10% power supply variation and a junction temperature ≤150°C. MIL-STD-883C Class B screening is used.

FRONT-ANNOTATION STATISTICAL WIRE LOADS

L_{net}

NET -1	Q2100B	Q9100B	NET -1	Q2100B	Q9100B
1	1.00	1.18	31	9.64	25.95
2	1.58	2.20	32	9.85	26.70
3	2.06	3.17	33	10.05	27.45
4	2.50	4.11	34	10.25	28.20
5	2.89	5.02	35	10.45	28.94
6	3.26	5.92	36	10.65	29.69
7	3.61	6.80	37	10.84	30.43
8	3.94	7.67	38	11.03	31.17
9	4.26	8.53	39	11.22	31.90
10	4.57	9.37	40	11.41	32.64
11	4.87	10.21	41	11.60	33.37
12	5.16	11.04	42	11.79	34.10
13	5.44	11.87	43	11.97	34.83
14	5.71	12.69	44	12.15	35.56
15	5.97	13.50	45	12.33	36.29
16	6.23	14.31	46	12.51	37.01
17	6.49	15.11	47	12.69	37.74
18	6.74	15.91	48	12.87	38.46
19	6.98	16.70	49	13.05	39.18
20	7.22	17.49	50	13.22	39.90
21	7.46	18.28	51	13.40	40.62
22	7.69	19.06	52	13.57	41.33
23	7.92	19.84	53	13.74	42.05
24	8.15	20.61	54	13.91	42.76
25	8.37	21.38	55	14.08	43.47
26	8.59	22.15	56	14.25	44.18
27	8.80	22.91	57	14.42	44.89
28	9.02	23.68	58	14.58	45.60
29	9.23	24.44	59	14.75	46.31
30	9.44	25.19	60	14.91	47.01

Where NET-1 is the internal net physical pin count minus 1. Fan-outs count as one pin each, regardless of electrical fan-in represented by the load. Electrical fan-out loading is taken care of in the L_{fo} term.

FRONT AND BACK ANNOTATION MODEL PARAMETERS
TYPICAL k-FACTORS

Parameter/Family	Q14000 NS/LU
Standard Option-INTERNAL	
Drive Factor, k,up,mas	0.025-0.045
Drive Factor, k,dn,mas	0.025-0.045
High Speed Option - I/O	
Drive Factor, k,up,mas	0.025ns/LU
Drive Factor, k,dn,mas	0.030ns/LU
Standard Option - I/O	
Drive Factor, k,up,mas	0.025ns/LU
Drive Factor, k,dn,mas	0.030ns/LU
Specific wire load	
(metal 1) q,wire1	1.20 LU/mm
(metal 2) q,wire2	3.00 LU/mm

WORST-CASE MAXIMUM CURRENT MULTIPLICATION FACTOR

Product Grade	Worst-case Current Multiplier WCCM
MIL	1.54
COM	1.35

AMCC Q14000 ARRAYS TYPICAL OVERHEAD CURRENT DRAIN (mA)

CHIP	TTL MODE I_{CC},mA	ECL MODE I_{EE},mA	MIXED MODE I_{EE}/I_{CC},mA	+5V REF I_{CC},mA	ECL/TTL
Q2100	101	87	90/22	109	ECL 10K
Q2100	101	87	91/22	109	ECL 100K
Q9100	132	117	121/22	140	ECL 10K
Q9100	132	121	125/22	143	ECL 100K

The macro occurrence ERC includes overhead current in the power dissipation computation for the interface macros. The ERC also provides a table of internal macro usage to allow the designer to complete the power computation.

Equation used to compute internal cell power dissipation:

Pinwc = F * 0.2 * G * 20 microwatt/gate-MHz
F = operating frequency
G = Total gate count
(internal gate count =
4 * internal Cell count)
assumes 20% of gates switching.

ECL TERMINATION CURRENT

The ECL termination current is a function of the actual load. When a macro is selected it should be capable of driving a resistive load equal to or greater than its rating. The ERCs will assume the load to be equal to the rated load:

ECL TERMINATION CURRENT

TERMINATION	CURRENT
25ohm	28.0mA
50ohm	14.0mA
100ohm	7.0mA
200ohm	3.5mA

where the currents shown are the average current (average of I_{OH} and I_{OL}) for 50% terminations active. If other ECL output load values are used, the actual current values must be computed for use in the equation.

Since the macro occurrence ERC for the Q14000 uses a 50 ohm termination, for other terminations, an adjustment on the power dissipation computation must be made by the designer.

I_{EE} VS. TEMPERATURE

I_{EE} varies with temperature as follows:

$-0.04\ \% /^{o}C$

EXTERNAL PIN COUNT

The external pin count is the sum of all input, all output and all bidirectional signals plus the fixed power and ground pins and any added power and ground pins required due to simultaneously switching outputs, 3-state drivers, etc. The external pin count of a design may not exceed the external pin count limit for the array.

EXTERNAL PIN COUNT LIMIT

ARRAY NAME	REQUIRED POWER-GROUND PINS	CIRCUIT I/O PIN LIMIT	TOTAL EXTERNAL PINS
Q9100B	56	160	216
Q2100B	28	80	108

External pin count is reported by the population ERC.

Some packages provide for additional grounds beyond the external pin count limit for the array. These grounds do not appear on the EWS schematic nor do they appear in the ERC reports.

PACKAGE SELECTION

Package selection requires that the designer have two computations completed: 1) the total maximum worst-case power dissipation; and 2) the total number of external pins required. The external pins required is provided by the AMCC MacroMatrix ERC software Population Check Report as shown on the next page and is the sum of all signals, all power (fixed and added) and all ground (fixed and added) pins as indicated on the schematics.

The designer also needs the current AMCC Packaging Brochure Table 1a, which lists the package options for the bipolar arrays as well as the tables providing the Θ_{jc} and Θ_{ja} and the reductions possible with forced air and heatsinks.