AMCC
APPLIED MICRO CIRCUITS CORPORATION

Q5000 RAPID REFERENCE

(804)

INTRODUCTION
Q5000 RAPID REFERENCE

This document is not intended as a replacement for the Q5000 Series Design Manual, class note set or the design guide. It is intended to provide the designer with a compact easy cross-reference to the tables for all bipolar arrays in the series to allow design decisions affecting the selection of an array within the series. These decisions include operating speed, sizing, population, macro options, power, maximum current, loading and fan-out limits.

The assumption is that the designer has previously reviewed:

- The Design Manual for the Q5000
- The Design Submission Document for the EWS or for AMCC Implemented Design Submission Design Manual Vol II, Sec 6.
- AMCC EWS Schematic Rules and Conventions Design Manual Vol II, Sec 3 and Sec 7.
- AMCC Vector Submission Rules and Guidelines Design Manual Vol II, Sec 4
- Bipolar/BiCMOS Design Validation Design Manual Vol II, Sec 5.

EQUIVALENT GATES

An equivalent gate is defined as a 2-input NOR gate for the bipolar arrays. A measure of design density is the number of these gates that would be required to construct the design in SSI logic. The number of equivalent gates is also a sizing measure for the AMCC logic arrays.

SIZES OF THE AMCC BIPOLAR ARRAYS

ARRAY NAME	PRODUCT FAMILY	EQUIVALENT GATES
Q5000T	Q5000	5000
Q3500T	Q5000	3500
QM1600T	Q5000	1600 + 1280 bits of RAM
Q1300T	Q5000	1300

The actual circuit density obtained is a function of the design objectives, design approach and macros selected.

A denser design is possible if the more complex macros are used first - MSI level and then other cell-efficient, dense macros - keeping the use of SSI-level AND, OR, NOR, NAND gates to a minimum. Balanced delay paths use more cells than a minimized design; high-speed designs may use more cells if heavily loaded paths are to be broken up into parallel structures.

MAXIMUM OPERATING FREQUENCY

The maximum operating frequency is specified as the maximum I/O switching rate for an I/O macro or the maximum internal toggle rate for an internal macro. The actual speed at which a circuit may operate must be computed from a worst-case critical-path timing analysis and must include the intrinsic macros delays (specified as "Tpd" in the macro documentation) and the extrinsic loading delays as computed using Front-Annotation.

MAXIMUM OPERATING FREQUENCY

TYPE OF I/O:	OPTION:	MAX LIMIT MHz	PW ns	Indicate f on I/O list when f > MHz
TTL INPUT	S	120	4.16	120
	H,D	160	3.12	120
TTL OUTPUT	S	65	7.69	50
	H	90	5.55	50
	L	30	16.66	30
ECL INPUT	S,D	240	2.08	125 *
	S,D	360	1.38	125 **
COMMERCIAL	V MACRO	600	0.83	always
MILITARY	V MACRO	450	1.11	always
ECL OUTPUT	S	180	2.77	100 *
	S	360	1.38	100 **
COMMERCIAL	V MACRO	600	0.83	always
MILITARY	V MACRO	450	1.11	always
INTERNAL SWITCHING FREQUENCY				
INTERNAL	S	210	2.38	
	H,D	360	1.38	
	L	150	3.33	
COMMERCIAL	V MACRO	600	0.83	
MILITARY	V MACRO	450	1.11	

* SINGLE-ENDED
** DIFFERENTIAL

For hierarchical macros, refer to the individual maximum frequency of operation specification within the macro library documentation.

For I/O macros, the toggle frequency should be added to the I/O list in the appropriate column only when the frequency exceeds that listed in the right column. This will allow proper high-speed design validation to be performed by AMCC. The I/O list is generated as AMCCIO.LST by the MacroMatrix software.

INTERNAL RESOURCES

In selecting an array, one of the first sizing considerations is the number and type of internal cells and interface cells available. The internal matrix area of the Q5000 Series bipolar arrays is composed of logic (L) cells.

INTERNAL ARRAY CELL RESOURCE SUMMARY

Array Series	Array Name	Total Cells	
Q5000	Q5000T	352	
	Q3500T	242	
	QM1600T	114	+ RAM
	Q1300T	84	

The Q5000T Array has a two-layer metalization interconnect plus a third layer of metalization for power bus distribution. All other arrays in the series have a two-layer metalization for both interconnect and power bus distribution.

Internal cell usage is reported by the population ERC.

I/O RESOURCES - IN GENERAL

The flexible I/O of the AMCC Logic Arrays allow a broad selection of interfaces. TTL, ECL, TTL/ECL, +5V REF ECL, +5V REF ECL/TTL with either ECL 10K or ECL 100K are among the modes supported (consult the individual library for specific limitations). TTL totem pole, open-collector and three-stated outputs are also supported as are ECL terminations of 50ohms and 25ohms.

There is limit on the number of output macros that may be used on the Q5000T array. The limit is 30 per quadrant and 30 per side.

The AMCC MacroMatrix ERC population report will show an error if more than 120 output macros are used for the Q5000T. A bidirectional counts as an output macro.

The number of fixed power and ground pads for a given I/O mode and a given array is displayed on the chip macro for that array and I/O mode.

There are placement restrictions when both ECL 10K and ECL 100K appear on the same circuit.

Cell and pad usage is reported by the population ERC.

Q5000 SERIES I/O AND POWER-GROUND RESOURCES

MODE	DESCRIPTION	Q5000T	Q3500T	Q1300T	QM1600T
INTERNAL CELLS		352	242	84	114
100%	I/O Cells	160	120	76	106
TTL	CORE V+ (+5V)	4	6	4	6
	CORE GND (0V)	4	6	4	6
	I/O V+ (+5V)	4	4	4	4
	I/O GND (0V)	12	12	4	12
100%	I/O Cells	160	120	76	106
ECL	CORE GND (0V)	4	6	4	6
-5.2V	CORE V- (**)	4	6	4	6
or	I/O GND (0V)	16	16	8	16
-4.5V					
100%	I/O Cells	160	120	76	106
ECL	CORE V+ (+5V)	4	6	4	6
	CORE GND (0V)	4	6	4	6
+5VREF	I/O V+ (+5V)	16	16	8	16
MIXED	I/O Cells	160	120	76	106
ECL/TTL	CORE GND (0V)	4	6	4	6
-5.2V	CORE V- (**)	4	6	4	6
or	I/O V+ (+5V)	4	4	4	4
-4.5V	I/O GND (0V)	12	12	4	12
MIXED	I/O cells	160	120	76	106
ECL/TTL	CORE V+ (+5V)	4	6	4	6
	CORE GND (0V)	4	6	4	6
+5VREF	I/O V+ (+5V)	8	8	4	8
	I/O GND (0V)	8	8	4	8

** CORE V-: -5.2V FOR STD-REF ECL 10K
-4.5V FOR STD-REF ECL 100K

ADDING EXTRA POWER AND GROUND

The Q5000 Series Logic Arrays require that extra power and grounds be added when the number of simultaneously switching TTL or ECL outputs exceeds eight (8) for any QUADRANT of the array. Add an ITPWR - ITGND pair for each group of eight TTL simultaneously switching outputs after the first eight. Add an IEVCC for each group of eight simultaneously switching ECL outputs after the first eight.

As a general rule and specifically for the Q5000T, additional power and grounds should be placed on pads that can connect to the internal package power and ground planes. Consult AMCC for placement restrictions if you are doing preplacement.

The simultaneously switching ERC check evaluates added power and ground requirements due to simultaneously switching outputs. The designer must use the SWGROUP parameter on all simultaneously switching output macros and on the power and ground macros added for them if the check is to be performed.

Q5000 SERIES;
ADDITIONAL POWER/GROUND

# OF SIMULTANEOUSLY SWITCHING TTL PER QUADRANT		ADD TTL VCC - TTL GROUND PAIRS (2 pads)
TTL in any system; 100% TTL or mixed mode	0 - 8	0
	9 - 16	1
	17 - 24	2
	25 - 30*	3

# OF SIMULTANEOUSLY SWITCHING ECL PER QUADRANT		ADD ECL VCC:
ECL in any system; 100% ECL or mixed mode	0 - 8	0
	9 - 16	1
	17 - 24	2
	25 - 30*	3

* There is a MAXIMUM of 30 I/O cells per quadrant that may be used for outputs on the Q5000T array. The 10 additional I/O cells per quadrant are for input-only macros. No other array in the series limits the number of outputs that can be usd.

EXTRA POWER AND GROUND MACROS

Place on the schematics according to the EWS Schematics Rules and Conventions:

SERIES:	TTL V_{CC}	TTL GND	ECL VCC
Q5000	ITPWR	ITGND	IEVCC

The population ERC reports on added power and ground usage. The AMCCIO.LST report contains a summary of simultaneously switching outputs, provided that the macro parameter SWGROUP is used for all groups of simultaneously switching output macros and all added power and ground macros added to accommodate those groups.

MAXIMUM INTERNAL CELL UTILIZATION

Internal cell utilization is one means of estimating the feasibility of a design on a given array. The specified cell utilization limit is designed as a sizing guideline. Designs meeting the restrictions are expected to be routable designs, provided they also satisfy internal pin count limits. The cell utilization refers to the internal array matrix (L cells) only and should not be considered to be the only population check.

INTERNAL L CELL UTILIZATION LIMITS

Array	%
Q5000T	95
Q3500T	95
Q1300T	95
QM1600T	95

Cell utilization is reported by the population ERC.

INTERNAL PIN COUNT LIMIT

The internal cell utilization limit is a guideline for the routability of an array. A more specific check on routability is the internal pin count.

- An array is routable if the number of internal pins that must be routed does not exceed the maximum pin count limit.
- It is considered to be a RISKY design if the number of pins is up to +10% over the maximum pin count limit.
- It is considered to be an EXTREMELY RISKY design if the number of pins is from +11% to +18% over the maximum pin count limit.
- A design is UNACCEPTABLE if the number of pins is ≥+18% over the maximum allowed pin count.

MAXIMUM INTERNAL PIN-COUNT

Array	Actual Limit	Estimated Limit
Q5000T	3572	3393
Q3500T	2470	2346
QM1600T	1200	1140
Q1300T	906	860

The AMCC MacroMatrix internal pin count ERC reports the internal pin count.

ESTIMATING INTERNAL PIN-COUNT

If the number of internal pins that must be routed (pin-count) is not available for a design in its early stages (prior to capture), estimate it by the following guidelines.

SERIES	MACRO	PINS
Q5000	Internal	8.0
	I/O	1.5
	MSI	as specified

Do not count external pins or pin connected to pads

Q5000 Series hierarchical macros state their pin count (refer to the macro summary, Design Manual Volume I, Section 6).

MAXIMUM LIMIT ON HIGH-CURRENT INTERNAL MACROS
MAXIMUM INTERNAL CURRENT SPECIFICATION

The Q5000 L-option macros can be used to counter-balance the use of H-option, high-fan-out drivers and other high current macros providing speed-power programmability.

MAXIMUM INTERNAL CURRENT SPECIFICATION

Array:	Maximum Internal Current (mA)	Guideline (% H, D macros)	Row Limit mA/row
Q5000T	1383	100%	54
Q3500T	843	50%	39
QM1600T	427	100%	23
Q1300T	405	100%	34

• QM1600T: 160mA TYPICAL for 0.5 of RAM
% H, D macros = % of H-option and high-fan-out drivers

• During design, the maximum internal current specification should be used to determine limits for the circuit. (The sum of all current dissipated by macros placed on L cells times the worst-case current multiplier should be compared to the above table.) A computed internal current of 80% of the above limit or higher indicates that an array may have problems during layout.

• During layout, the maximum row current limits restrict the placement of H option or other high-current macros. Note that any one row may exceed the core limit divided by the number of rows.

The macro occurrence report ERC checks maximum core current utilization. Recommendation: design with S-option macros and change to H-option or drivers where necessary and to L-option macros where acceptable.

FAN-OUT RESTRICTIONS

The individual macro fan-out load limits are specified in the Design Manual, Volume I, Section 6. Derating requirements are discussed in Volume I, Section 2.

(STANDARD/20% DERATED/40% DERATED)
Derating breakpoint: 160MHz.

Q5000 Series	S	L	H
Unbuffered input macros:			
TTL	1/1/1	-	-
ECL	8	-	-
Input buffers	9/7/5	4/3/2	9/7/5
Logic macros	9/7/5	4/3/2	9/7/5
Output macros	REFER TO DATA SHEET		
3-state enable drivers	8	8	8
High-fan-out drivers (interface orinternal)	15/12/9	-	-
Super drivers (interface or internal)	25	25	25
V macros (very fast macros)	9	9	9

- High fan-out drivers with fan-out load limit = 25 are not derated.
- 3-State Enable-Drivers are not derated.
- Very-fast V-macros are not derated.
- Macros with a k factor = 0 are not derated.
- Derate all clock lines and distortion-sensitive paths by 20% for speeds below the breakpoint and by 40% for speeds at or above the breakpoint.

The fan-out ERC checks for excessive loading. It will check for a derated load limit only if the FOD net parameter has been used.

HIGH-CAPACITIVE LOADING ON OUTPUT MACROS - ALL ARRAYS

ECL and TTL output macros are specified with NO CAPACITIVE loading on the macros. All capacitive loads must be computed for the delay calculations.

TYPICAL
OUTPUT CAPACITIVE LOAD DELAY
CONVERSION FACTORS

ECL	.045ns/pf	rising edge
	.037ns/pf	falling edge
TTL	.072ns/pf	rising edge
	.072ns/pf	falling edge

The capacitive load delay should be added to the total typical path delay and the sum multiplied by the appropriate worst-case timing multiplier to find the maximum worst-case delay.

Capacitive load is the sum of the package pin capacitance for the output pin and the system load seen by that pin.

- A default system load is 5pf, ECL, and 15pf, TTL.

- Package pin capacitance varies by package and by specific pin. 3-16pf can be used as an estimation range.

The following table provides the typical time delay associated with a given capacitive load based on the k-factor of the macro and the I/O type and is for delay estimation use.

OUTPUT LOADING TYPICAL TIME DELAYS

load pf	ECL Rising ns	ECL Falling ns	TTL Rising ns	TTL Falling ns
0.0	0.0000	0.0000	0.0000	0.0000
5.0	0.2250	0.1850	0.3600	0.3600
10.0	0.4500	0.3700	0.7200	0.7200
15.0	0.6750	0.5550	1.0800	1.0800
20.0	0.9000	0.7400	1.4400	1.4400
25.0	1.1250	0.9250	1.8000	1.8000
30.0	1.3500	1.1100	2.1600	2.1600
35.0	1.5750	1.2950	2.5200	2.5200
40.0	1.8000	1.4800	2.8800	2.8800
45.0	2.0250	1.6650	3.2400	3.2400
50.0	2.2500	1.8500	3.6000	3.6000
55.0	2.4750	2.0350	3.9600	3.9600
60.0	2.7000	2.2200	4.3200	4.3200
65.0	2.9250	2.4050	4.6800	4.6800
70.0	3.1500	2.5900	5.0400	5.0400

Sum the package pin capacitance and the system capacitive load for a path. Determine if it is a rising edge or a falling edge output driving the load. Find the typical time delay in ns based on technology (ECL or TTL), the direction of the driving edge and the capacitive load. For loads above 70pf, factor by 70 and add the resulting delays together. For loads over 100pf, consult AMCC.

WORST-CASE PROPAGATION DELAY MULTIPLICATION FACTORS
WORST-CASE TIMING MULTIPLIERS

All of the tables shown and all of the macro propagation delay specifications given in the design guides and design manuals provide typical propagation delays. To perform worst-case analysis, the following worst-case multipliers must be used.

WORST-CASE TIMING MULTIPLIERS
FOR FRONT- AND BACK-ANNOTATION
FOR INTRINSIC AND EXTRINSIC PROPAGATION DELAYS

Array Series:		Q5000
MINIMUM	minimum	0.7
	typical	0.78
	maximum	0.86
NOMINAL	minimum	0.9
	typical	1.0
	maximum	1.1
COMMERCIAL	minimum	1.11
	typical	1.23
	maximum	1.35
MILITARY	minimum	1.19
	typical	1.32
	maximum	1.45

The worst-case delay multipliers for annotated simulations take into account the following:

- Process variations;
- Temperature variations;
- Voltage variations;
- Signal skew;

and apply to both the intrinsic macro delays (t_{in} = Tpd) and the extrinsic loading delays (t_{ex}).

• For each net, the AMCC MacroMatrix Front-Annotation (and Intermediate-Annotation) software computes an ESTIMATED metal delay based on the estimated length of the net and combines this with the actual delay due to electrical fan-out loading and any wire-OR present in the net. Intermediate-Annotation is post-placement and a closer refinement of the estimated delay. It is still an estimate.

• For each net, the Back-Annotation software uses the post-layout file to insert the ACTUAL metal delay and combines this with the actual delay due to electrical fan-out loading and any wire-OR present in the net.

COMMERCIAL SPECIFICATION

Commercial worst-case timing multipliers are for $0^{o}C$ ambient to $70^{o}C$ ambient with ±5% power supply variation and a junction temperature of $\leq 130^{o}C$. For a junction temperature that is $> 130^{o}C$ or for any other violation of the commercial environment specification, use the MILITARY worst-case timing multipliers.

MILITARY SPECIFICATION

Military worst-case timing multipliers are for $-55^{o}C$ ambient to $+125^{o}C$ case with ±10% power supply variation and a junction temperature of $\leq 150^{o}C$. MIL-STD-883C Class B screening is used. If the junction temperature is $> 150^{o}C$ or for violation of any other military environment specification, consult AMCC.

FRONT- AND BACK-ANNOTATION MODEL PARAMETERS
k-FACTORS FOR THE Q5000 SERIES

Description	k-Factors
Standard Option	
Drive Factor, k,rising	.040 ns/LU
Drive Factor, k,falling	.040 ns/LU
High Speed Option	
Drive Factor, k,rising	.020 ns/LU
Drive Factor, k,falling	.040 ns/LU
Low Power Option	
Drive Factor, k,rising	.040 ns/LU
Drive Factor, k,falling	.080 ns/LU
Driver Macro (15 load)	
Drive Factor, k,rising	.020 ns/LU
Drive Factor, k,falling	.020 ns/LU
Driver Macro (25 load)	
Drive Factor, k,rising	.010 ns/LU
Drive Factor, k,falling	.010 ns/LU
V-macros (9 loads)	
Drive Factor, k,rising	.020 ns/LU
Drive Factor, k,falling	.020 ns/LU

** Individual macro k-factors are specified in the macro library documentation in the Design Manual, Volume I, Section 6.

FRONT-ANNOTATION STATISTICAL WIRE LOADS

L_{net}

NET -1	Q1300T	Q3500T	QM1600T	Q5000T
1	1.80	2.39	1.96	3.84
2	2.86	3.80	3.12	6.11
3	3.76	4.99	4.09	8.02
4	4.56	6.05	4.96	9.72
5	5.29	7.03	5.76	11.29
6	5.98	7.94	6.51	12.76
7	6.63	8.80	7.22	14.14
8	7.25	9.63	7.89	15.47
9	7.85	10.42	8.54	16.74
10	8.42	11.18	9.17	17.96
11	8.97	11.92	9.77	19.15
12	9.51	12.63	10.36	20.29
13	10.04	13.33	10.93	21.41
14	10.55	14.01	11.49	22.50
15	11.05	14.67	12.03	23.57
16	11.54	15.32	12.56	24.61
17	12.01	15.95	13.08	25.63
18	12.48	16.57	13.59	26.63
19	12.94	17.19	14.09	27.61
20	13.40	17.79	14.59	28.58
21	13.84	18.38	15.07	29.53
22	14.28	18.96	15.55	30.46
23	14.71	19.53	16.02	31.38
24	15.14	20.10	16.48	32.29
25	15.56	20.65	16.94	33.19
26	15.97	21.20	17.39	34.07
27	16.38	21.75	17.83	34.94
28	16.78	22.28	18.27	35.80
29	17.18	22.81	18.71	36.66
30	17.58	23.34	19.14	37.50

Where NET-1 is the internal net physical pin count minus 1. Fan-outs count as one pin each, regardless of electrical fan-in represented by the load. Electrical fan-out loading is taken care of in the L_{fo} term.

FRONT-ANNOTATION LOAD UNITS

The Front-Annotation statistical wire load units table was calculated using the following :

$$LU = a * (netsize-1)^{** b}$$

FRONT-ANNOTATION LOAD UNITS

ARRAYS	b	a	wire1	wire2
Q5000T	0.67	3.84	1.80	1.80
Q3500T	0.67	2.39	1.80	1.00
Q1300T	0.67	1.80	1.80	1.00
QM1600T	0.67	1.96	1.80	1.00

BACK-ANNOTATION LOAD UNITS

The Back-Annotation delay file is derived using the following:

BACK-ANNOTATION LOAD UNITS

	METAL 1		METAL 2	
	$C_{1rising}$	$C_{1falling}$	$C_{2rising}$	$C_{2falling}$
	LU/mm	LU/mm	LU/mm	LU/mm
Q5000T	1.3	1.8	1.0	1.8
Q3500T	1.0	1.8	0.6	1.0
Q1300T	1.0	1.8	0.6	1.0
QM1600T	1.0	1.8	0.6	1.0

$$LU_{rise} = \frac{(M1 * C_{1rising}) + (M2 * C_{2rising})}{1000}$$

$$LU_{fall} = \frac{(M1 * C_{1falling}) + (M2 * C_{2falling})}{1000}$$

M1 = length of metal 1
M2 = length of metal 2

The following pages are for delay estimation use and provide the typical time delay for a given L_{net} (espressed in load units) and macro k-factor (ns/LU) for each of the arrays in the Q5000 Series.

Q5000T ARRAY

k * L_{net} TYPICAL TIME DELAYS

NET -1	k-Factor: 0.01 ns	0.02 ns	0.04 ns	0.08 ns
1	0.04	0.08	0.15	0.31
2	0.06	0.12	0.24	0.49
3	0.08	0.16	0.32	0.64
4	0.10	0.19	0.39	0.78
5	0.11	0.23	0.45	0.90
6	0.13	0.26	0.51	1.02
7	0.14	0.28	0.57	1.13
8	0.15	0.31	0.62	1.24
9	0.17	0.33	0.67	1.34
10	0.18	0.36	0.72	1.44
11	0.19	0.38	0.77	1.53
12	0.20	0.41	0.81	1.62
13	0.21	0.43	0.86	1.71
14	0.23	0.45	0.90	1.80
15	0.24	0.47	0.94	1.89
16	0.25	0.49	0.98	1.97
17	0.26	0.51	1.03	2.05
18	0.27	0.53	1.07	2.13
19	0.28	0.55	1.10	2.21
20	0.29	0.57	1.14	2.29
21	0.30	0.59	1.18	2.36
22	0.30	0.61	1.22	2.44
23	0.31	0.63	1.26	2.51
24	0.32	0.65	1.29	2.58
25	0.33	0.66	1.33	2.65
26	0.34	0.68	1.36	2.73
27	0.35	0.70	1.40	2.80
28	0.36	0.72	1.43	2.86
29	0.37	0.73	1.47	2.93
30	0.37	0.75	1.50	3.00

Index by net size minus 1 same as for Front-Annotation Table.

Q3500T ARRAY

$k * L_{net}$ TYPICAL TIME DELAYS

NET -1	k-Factor: 0.01 ns	0.02 ns	0.04 ns	0.08 ns
1	0.02	0.05	0.10	0.19
2	0.04	0.08	0.15	0.30
3	0.05	0.10	0.20	0.40
4	0.06	0.12	0.24	0.48
5	0.07	0.14	0.28	0.56
6	0.08	0.16	0.32	0.64
7	0.09	0.18	0.35	0.70
8	0.10	0.19	0.39	0.77
9	0.10	0.21	0.42	0.83
10	0.11	0.22	0.45	0.89
11	0.12	0.24	0.48	0.95
12	0.13	0.25	0.51	1.01
13	0.13	0.27	0.53	1.07
14	0.14	0.28	0.56	1.12
15	0.15	0.29	0.59	1.17
16	0.15	0.31	0.61	1.23
17	0.16	0.32	0.64	1.28
18	0.17	0.33	0.66	1.33
19	0.17	0.34	0.69	1.37
20	0.18	0.36	0.71	1.42
21	0.18	0.37	0.74	1.47
22	0.19	0.38	0.76	1.52
23	0.20	0.39	0.78	1.56
24	0.20	0.40	0.80	1.61
25	0.21	0.41	0.83	1.65
26	0.21	0.42	0.85	1.70
27	0.22	0.43	0.87	1.74
28	0.22	0.45	0.89	1.78
29	0.23	0.46	0.91	1.83
30	0.23	0.47	0.93	1.87

Q1300T ARRAY

$k * L_{net}$ TYPICAL TIME DELAYS

NET -1	k-Factor: 0.01 ns	0.02 ns	0.04 ns	0.08 ns
1	0.02	0.04	0.07	0.14
2	0.03	0.06	0.11	0.23
3	0.04	0.08	0.15	0.30
4	0.05	0.09	0.18	0.36
5	0.05	0.11	0.21	0.42
6	0.06	0.12	0.24	0.48
7	0.07	0.13	0.27	0.53
8	0.07	0.15	0.29	0.58
9	0.08	0.16	0.31	0.63
10	0.08	0.17	0.34	0.67
11	0.09	0.18	0.36	0.72
12	0.10	0.19	0.38	0.76
13	0.10	0.20	0.40	0.80
14	0.11	0.21	0.42	0.84
15	0.11	0.22	0.44	0.88
16	0.12	0.23	0.46	0.92
17	0.12	0.24	0.48	0.96
18	0.12	0.25	0.50	1.00
19	0.13	0.26	0.52	1.04
20	0.13	0.27	0.54	1.07
21	0.14	0.28	0.55	1.11
22	0.14	0.29	0.57	1.14
23	0.15	0.29	0.59	1.18
24	0.15	0.30	0.61	1.21
25	0.16	0.31	0.62	1.24
26	0.16	0.32	0.64	1.28
27	0.16	0.33	0.66	1.31
28	0.17	0.34	0.67	1.34
29	0.17	0.34	0.69	1.37
30	0.18	0.35	0.70	1.41

QM1600T ARRAY

k * L_{net} TYPICAL TIME DELAYS				
	k-Factor:			
NET -1	0.01 ns	0.02 ns	0.04 ns	0.08 ns
1	0.02	0.04	0.08	0.16
2	0.03	0.06	0.12	0.25
3	0.04	0.08	0.16	0.33
4	0.05	0.10	0.20	0.40
5	0.06	0.12	0.23	0.46
6	0.07	0.13	0.26	0.52
7	0.07	0.14	0.29	0.58
8	0.08	0.16	0.32	0.63
9	0.09	0.17	0.34	0.68
10	0.09	0.18	0.37	0.73
11	0.10	0.20	0.39	0.78
12	0.10	0.21	0.41	0.83
13	0.11	0.22	0.44	0.87
14	0.11	0.23	0.46	0.92
15	0.12	0.24	0.48	0.96
16	0.13	0.25	0.50	1.00
17	0.13	0.26	0.52	1.05
18	0.14	0.27	0.54	1.09
19	0.14	0.28	0.56	1.13
20	0.15	0.29	0.58	1.17
21	0.15	0.30	0.60	1.21
22	0.16	0.31	0.62	1.24
23	0.16	0.32	0.64	1.28
24	0.16	0.33	0.66	1.32
25	0.17	0.34	0.68	1.36
26	0.17	0.35	0.70	1.39
27	0.18	0.36	0.71	1.43
28	0.18	0.37	0.73	1.46
29	0.19	0.37	0.75	1.50
30	0.19	0.38	0.77	1.53

TYPICAL TIME DELAYS
- due to electrical fan-out loads
$k * L_{fo}$

Electrical FAN-OUT loads	k-Factor: 0.01 ns	0.02 ns	0.04 ns	0.08 ns
1	0.01	0.02	0.04	0.08
2	0.02	0.04	0.08	0.16
3	0.03	0.06	0.12	0.24
4	0.04	0.08	0.16	0.32
5	0.05	0.10	0.20	0.40
6	0.06	0.12	0.24	0.48
7	0.07	0.14	0.28	0.56
8	0.08	0.16	0.32	0.64
9	0.09	0.18	0.36	0.72
10	0.10	0.20	0.40	0.80
11	0.11	0.22	0.44	0.88
12	0.12	0.24	0.48	0.96
13	0.13	0.26	0.52	1.04
14	0.14	0.28	0.56	1.12
15	0.15	0.30	0.60	1.20
16	0.16	0.32	0.64	1.28
17	0.17	0.34	0.68	1.36
18	0.18	0.36	0.72	1.44
19	0.19	0.38	0.76	1.52
20	0.20	0.40	0.80	1.60
21	0.21	0.42	0.84	1.68
22	0.22	0.44	0.88	1.76
23	0.23	0.46	0.92	1.84
24	0.24	0.48	0.96	1.92
25	0.25	0.50	1.00	2.00
26	0.26	0.52	1.04	2.08
27	0.27	0.54	1.08	2.16
28	0.28	0.56	1.12	2.24
29	0.29	0.58	1.16	2.32
30	0.30	0.60	1.20	2.40

The typical time delay in a net due to the electrical fan-out loads. The value varies by k-factor and load size.

L_{WO} AND TYPICAL TIME DELAYS $k * L_{WO}$

		k-Factor:			
SIZE:	LU	0.01 ns	0.02 ns	0.04 ns	0.08 ns
WIREOR2	0.75	0.00	0.01	0.02	0.03
WIREOR3	1.50	0.01	0.02	0.03	0.06
WIREOR4	2.25	0.02	0.03	0.06	0.13

The typical time delays are due to the electrical load presented by the wire-ORs for the various k-Factors. The use of a wire-OR also increases the net size.

POWER-DOWN OF UNUSED OUTPUTS

When a macro output pin is terminated, the layout software will power-down the output emitter-follower (I_{OEF}) current source for that output pin thereby reducing the current dissipated by the macro. The amount of current is a function of the array series and of the macro option. Macro output pins that cannot be powered down are marked with an asterisk and noted in the macro documentation in Volume I, Section 6 of the Design Manual.

I_{OEF} FOR POWERED-DOWN OUTPUTS

	mA
S-OPTION LOGIC MACRO	0.36
H-OPTION LOGIC MACRO	0.36
L-OPTION LOGIC MACRO	0.18
VERY FAST INTERNAL LOGIC V-MACRO	***
15-LOAD DRIVER - LOGIC MACRO	0.72
25-LOAD DRIVER - LOGIC MACRO	2.16
3-STATE ENABLE-DRIVER - ANY	N/A
S-OPTION INTERFACE MACRO	0.45
H-OPTION INTERFACE MACRO	0.45
VERY FAST INTERFACE V-MACRO	***
15-LOAD DRIVER INTERFACE MACRO	1.62
25-LOAD DRIVER INTERFACE MACRO	2.79

*** Very fast V-macros are differential and both outputs MUST be used.

In most cases, when a pin is wire-ORable, it can be powered-down. The exceptions are the drivers. No driver may be wire-ORed but an unused driver macro output may be powered down.

The macro occurrence ERC will compute the total current saved due to the power-down of macro output pins and the effect will be included in the resulting power dissipation computation.

WORST-CASE MAXIMUM CURRENT MULTIPLICATION FACTOR

Array Series %	Worst-case Current Multiplier WCCM MILITARY	COMMERCIAL
Q5000 SERIES	1.40	1.40

AMCC BIPOLAR ARRAYS OVERHEAD CURRENT DRAIN (mA)

ARRAY	TTL MODE I_{CC},mA	ECL MODE I_{EE},mA	MIXED MODE I_{EE}/I_{CC},mA	+5V REF ECL/TTL I_{CC},mA
Q5000T	193	286	286/11	309
Q3500T	130	170	174/14	193
Q1300T	108	131	136/14	157
QM1600T	130	170	174/14	193

The macro occurrence ERC includes overhead current in the power dissipation computation.

ECL TERMINATION CURRENT

The ECL termination current is a function of the actual load. When a macro is selected it should be capable of driving a resistive load equal to or greater than its rating. The ERCs will assume the load to be equal to the rated load.

ECL TERMINATION CURRENT

TERMINATION	CURRENT
25ohm	28.0mA
50ohm	14.0mA
100ohm	7.0mA
200ohm	3.5mA

where the currents shown are the average current (average of I_{OH} and I_{OL}) for 50% terminations active. If other ECL output load values are used, the actual current values must be computed for use in the equation.

Use: $I = (0.7 * V) / R$

Since the macro occurrence ERC uses either a 50 ohm or a 25 ohm termination, depending on the macro, for other terminations, an adjustment on the power dissipation computation must be made by the designer.

ARRAY PAD COUNT

The array pad count is the sum of all input, all output and all bidirectional signal pads plus the fixed power and ground pads and any added power and ground pads required due to simultaneously switching outputs, 3-state drivers, etc. The array pad count of a design may not exceed the array pad count limit for the array.

EXTERNAL PAD COUNT LIMIT

ARRAY NAME	REQUIRED POWER-GROUND PADS **	CIRCUIT I/O PAD LIMIT	TOTAL ARRAY PADS
Q5000T	24	160	184
Q3500T	28	120	148
Q1300T	16	76	92
QM1600T	28	106	134

** FIXED POWER-GROUND PADS; ALL MUST BE USED

Array pad count is currently reported as the external pin count by the population ERC. The number of package pins and the number of array pads may or may not be in a one for one relationship.

OUTPUT VOLTAGE TRACKING RATE WITH TEMPERATURE

When calculating V_{OH}, compute the junction temperature T_J for the actual thermal conditions (Θ_{ja}) at the specified ambient temperature as opposed to the specified conditions as detailed on the Q5000 Series Data Sheet. Calculate the adjustment to the specified V_{OH}. Then calculate any further adjustment to V_{OH} for any desired ambient temperature.

ECL ELECTRICAL CHARACTERISTICS
OUTPUT VOLTAGE TRACKING RATE WITH TEMPERATURE
OUTPUT VOLTAGE TRACKING RATE WITH SUPPLY VOLTAGE

	$\frac{dV_{OH}}{dT}$	$\frac{dV_{OL}}{dT}$	$\frac{dV_{OH}}{dV_{EE}}$	$\frac{dV_{OL}}{dV_{EE}}$
units:	mV/°C	mV/°C	mV/V	mV/V
ECL 10K	+1.0	-0.5	+30	+100
ECL 100K	+0.8	-0.5	+30	+100

Loading is 50 ohms to V_{CCO} = -2.0V

OUTPUT VOLTAGE TRACKING RATE WITH SUPPLY VOLTAGE

When computing the adjustment in V_{OH} for supply voltage, the adjustment is linear. V_{OH} is specified on the data sheet for nominal supply (-5.2V or -4.5V).

I_{EE} DERATING WITH TEMPERATURE

CORE CURRENT VARIATION WITH TEMPERATURE *

$$\frac{dI_{EE}}{dT} == -0.1\%/^{\circ}C \text{ change in } T_j$$

* For $T_j > 0$

The ECL core, overhead and interface macro current I_{EE} is a function of temperature variations. For +5V REF ECL/TTL circuits, it applies to I_{CC} in the core and that current in the ECL macros as well as to the ECL portion of the overhead. Use the parenthisized values from the overhead current table.

For consistency, derating is done from the junction temperature, T_j. ECL parametrics are measured at thermal equilibrium and T_j is assumed to be close to $0^{\circ}C$ when $T_a = -55^{\circ}C$.

$$I_{EE_{typical}} \text{ at } T_J = I_{EE_{typical}} * (1 - (0.001 * T_j))$$

$$I_{EE_{maximum}} \text{ at } T_J = I_{EE_{typical}} * WCCM * (1 - (0.001 * T_j))$$

where T_j is the desired junction temperature after airflow, heatsinking and ambient controls are in place. Or, T_j is the actual junction temperature taken from thermal diode measurements.

PACKAGING MATRIX FOR Q5000 SERIES ARRAYS AND ESTIMATE OF THERMAL RESISTANCES

θ_{jc}/θ_{ja}

	Q1300T	QM1600T	Q3500T	Q5000T
64 LDCC 40 mil center	TBS			
84 LDCC 50 mil center	TBS			
100 LDCC 25 mil center	TBS			
100 LDCC 50 mil center	TBS	TBS	TBS	TBS
132 LDCC 25 mil center		TBS	5/24	4/21
196 LDCC 25 mil center				4/21
68 PGA cavity down	TBS			
84 PGA cavity down	TBS			
100 PGA cavity down	6/30	TBS	5/24	5/24
148 PGA cavity down			4/21	3/17
224 PGA cavity down				1.5/15