AMCC
APPLIED MICRO CIRCUITS CORPORATION

Dear AMCC Customer,

We are pleased to provide you with the AMCC MacroMatrix software for the Q5000 Logic Array Series, which includes the macro library and design support software.

The macro library and design manual are individually registered to you. To request another of the Q5000 Design Manual, contact your local AMCC sales representative. The Q5000 Design Guide is available for those not actively doing a design.

Should you require addition assistance, please do no hesitate to call any of our application engineers at (619) 450-9333.

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MacroMatrix® Design Manual

Volume I
Q5000 Series

Bipolar Logic Arrays

Applied MicroCircuits Corporation

Q5000 Series Design Manual

Includes: Q1300T, QM1600T, Q2400T, Q3500T, Q5000T
Bipolar Logic Arrays

The material in this document
supercedes all previous
documentation issued for the
Q5000 Series Logic Arrays

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Section 1:

Introduction

INTRODUCTION

This design manual provides a summary of the AMCC (Applied Micro Circuits Corporation) Q5000 Series Bipolar Logic Arrays. Volume 1 is composed of the following sections:

- Section 1: Introduction
- Section 2: Design Methodology
- Section 3: Timing Analysis
- Section 4: External t_{su}, t_h
- Section 5: Power/Packaging
- Section 6: Macro Library Documentation
  - Section 6-1: TTL Interface
  - Section 6-2: TTLMIX Interface
  - Section 6-3: ECL Interface
  - Section 6-4: Internal Logic Macros
  - Section 6-5: Special Macros
- Section 7: Quicksheets
- Section 8: Index

It also includes information on:

- Product features
- Performance specifications
- Design Interface and support

and contains a listing of the macros currently available. The AMCC Packaging Brochure should also be referenced for further information on packaging.

The Q5000 Series supports the following arrays:

TABLE 1-1
SUPPORTED ARRAYS

- Q5000T
- Q3500T
- QM1600T
- Q1300T

Volume 1 of this design manual is intended as a self-contained design aid to allow the proper selection of an array for a particular design, to indicate the packaging available for that array, and to provide the designer with a better understanding of the capabilities of the Q5000 Series Bipolar Logic Arrays.

Section 2 contains design rules specific to this array series. RAM macro usage, interconnect rules and testing requirements are included in this section.

The macro summary and detailed macro specifications are presented in reference manual format in Section 6 with a rapid graphic reference provided via quicksheets in Section 7. Either a macro-conversion of an existing design, or the direct design of a circuit can be implemented using the available macros.

Volume 2 of this design manual is composed of the following sections:

- Section 1: Introduction
- Section 2: EWS-Specific Design Methodology
- Section 3: EWS Schematic Rules and Conventions
- Section 4: Vector Submission Rules and Guidelines
- Section 5: Design Validation
- Section 6: Design Submission
- Section 7: MacroMatrix® Installation
- Section 8: MacroMatrix User's Guide
- Section 9: AMCC Glossary
- Section 10: Index

Volume 2, Section 2 of this design manual contains the Engineering-workstation (EWS) design methodology, covering both the EWS-specific operations and the AMCC MacroMatrix support software.

Section 8 contains the MacroMatrix User's Guide which details the Engineering Rules Check (AMCCERC, a.k.a., ERC) software checks and error messages and probable causes. It also includes the Vector Rules Check (AMCCVRC) user's guide. Section 9 contains the MacroMatrix Installation and Operations manual, which summarizes the EWS-specific commands required for operation of the AMCC support software.

The Design Validation document in Section 5 details the engineering rules checks that must be reviewed prior to design submission. It is the basic outline of the design review AMCC performs prior to circuit acceptance. Fill in or check off items as indicated and submit the entire document as part of the design submission package. Additional copies can be obtained from AMCC.

The Design Submission Document in Section 6 is to be completed and submitted along with the design submission package. Additional copies can be obtained from AMCC.

The following trademarks are recognized by AMCC throughout this design manual:

- COPTR - General Electric Co.
- LOGICIAN - Daisy Systems Corp.
- GATEMASTER - Daisy Systems Corp.
- Mentor Graphics
- MacroMatrix - AMCC
- Valid Logic

Q5000 SERIES DESCRIPTION

The AMCC Q5000 Series Logic Arrays provide an optimized approach to bipolar semi-custom applications. High-speed ECL logic, mixed-mode I/O and proven reliability are combined with an advanced, interactive CAD design approach to provide a quick and cost-effective solution to discrete IC replacement. Manufacturing advantages gained from the use of the AMCC logic arrays include:

- Increased circuit density
- Increased system speed
- Reduced power
- Higher reliability
- Lower system cost
- Operation over both military and commercial temperature ranges

The AMCC Q5000 Series Logic Arrays Macro Library is supported on the Daisy, Mentor Graphics and Valid Logic Systems EWS. The designer can use any of these systems in conjunction with AMCC's MacroMatrix software package to perform schematic capture, Engineering Rules Checking (AMCCERC), simulation, automatic test pattern formatting (AMCCSIMFMT), AMCCVRC rules checking, Front-Annotation and Back-Annotation.

The Q5000 Series arrays are bipolar arrays. They use an internal ECL core and have the ability to externally interface to either Schottky TTL, ECL 10K or ECL 100K. ECL 10K or ECL 100K may be standard-reference or +5V reference ECL.

As an added feature, the Q5000 Series provides the ability to mix ECL 10K and TTL or ECL 100K and TTL on the same array. ECL 10K and ECL 100K outputs are also allowed on the same array, regardless of the ECL type used for input. For other combinations, please contact AMCC Marketing.

All of the interface options are realized through the choice of appropriate macros, and are personalized with metal masks only.

AMCC macros use series gating techniques to provide both density and speed improvements over gate-oriented designs. Three-level series gating is allowed on the Q5000 Series arrays providing density and performance advantages over two-level series gating.

AMCC describes the density of its logic arrays in terms of equivalent gates (2-input NOR gates), which are a function of the density of the available macros and the number of cells available in any given array. The density of the Q5000 Series is described below.

TABLE 1-2
ARRAY DENSITY

Array	Equivalent Gates
Q5000T	5000
Q3500T	3500
QM1600T	1600 plus 1280 bits of RAM
Q1300T	1300

For any given application, the actual functions required in a design determine the equivalent gate density. The efficiency of the array design, however, depends on the macros selected and the number of cells utilized.

The arrays in the Q5000 Series share a common macro function library which contains a wide selection of fully characterized logic functions varying from SSI to MSI densities. The higher functionality macros have correspondingly higher equivalent gate densities.

Examples of the basic logic functions include simple and complex gates, EXORs, EXNORS, simple nets, latches, decoders, MUXs, 4-bit counters, a 4-bit universal register, buffered input, high-speed ECL input, buffered and unbuffered output and ECL output macros which contain logic, buffers and output translation. Many of the macros provide complementary outputs to support signal inversion in distortion-sensitive paths.

AMCC logic arrays are structured to allow the components spread across several cells to be interconnected into a single high-functionality MSI macro. These hard-wired MSI macros guarantee consistent and predetermined circuit performance. AMCC recommends that designers use the higher functionality MSI macros whenever possible.

Almost all logic and many interface macros in the Q5000 Series macro library have high-speed (H) and low-power (L) options in addition to the standard (S) option of the macro. These macro options allow a designer to selectively program critical paths with high-speed operation while implementing the remainder of the design in the standard or low-power option macros.

In addition to the logic function, the QM1600T array contains 1280 bits of high-speed static RAM. The RAM word width can be configured using macros offered in a separate section of the macro library. (See RAM20 and RAM10 in Section 6.)

TYPICAL APPLICATIONS

Typical applications include high-speed computers, graphics, communications, test equipment and instrumentation. Designed to operate in the full MIL-SPEC temperature and voltage range, the Q5000 Series also has applications in radar, EW, avionics, guidance, flight simulation and other military systems.

FEATURES

A summary of the features of the Q5000 Series includes:

- 5000, 3500 and 1300 equivalent gate versions
- QM1600T, 1280 bits of RAM with 1600 equivalent gates
- 2-micron Oxide-Isolated Bipolar washed-emitter process

- 2-layer metal to customize base array (Q3500T, Q1300T, QM1600T)
- 3-layer metal on the Q5000T, with one layer dedicated to power bus distribution
- Autoroute with up to 95% logic cell utilization
- Extensive macro library, upwardly compatible with the Q3500 and Q1500 Series libraries
- System-level multiple-cell macros
- Speed/power programmable macros
- Schottky TTL, low-power Schottky TTL, ECL 10K and ECL 100K I/O compatibility
- Standard-reference ECL or +5V referenced ECL
- On-chip translators for mixed mode interface
- Both ECL 10K and ECL 100K outputs may appear on the same array
- High internal noise immunity
- Multiple power supply options available
- Unused cells do not dissipate power
- Fully voltage- and temperature-compensated internal logic
- Radiation hard process
- Full MIL operating range (-55°C ambient to +125°C case, ±10% power supply)
- Wide selection of packaging
- Supported on engineering workstations:
  - Daisy
  - Valid Logic
  - Mentor Graphics
- Supported on TEGAS 5
- Full CAD support, including post-autoroute, worst-case timing analysis

DESIGN INTERFACE AND SUPPORT

The AMCC circuit development interface has been structured to be highly flexible with respect to the customer's desired level of involvement. The basic steps are summarized below:

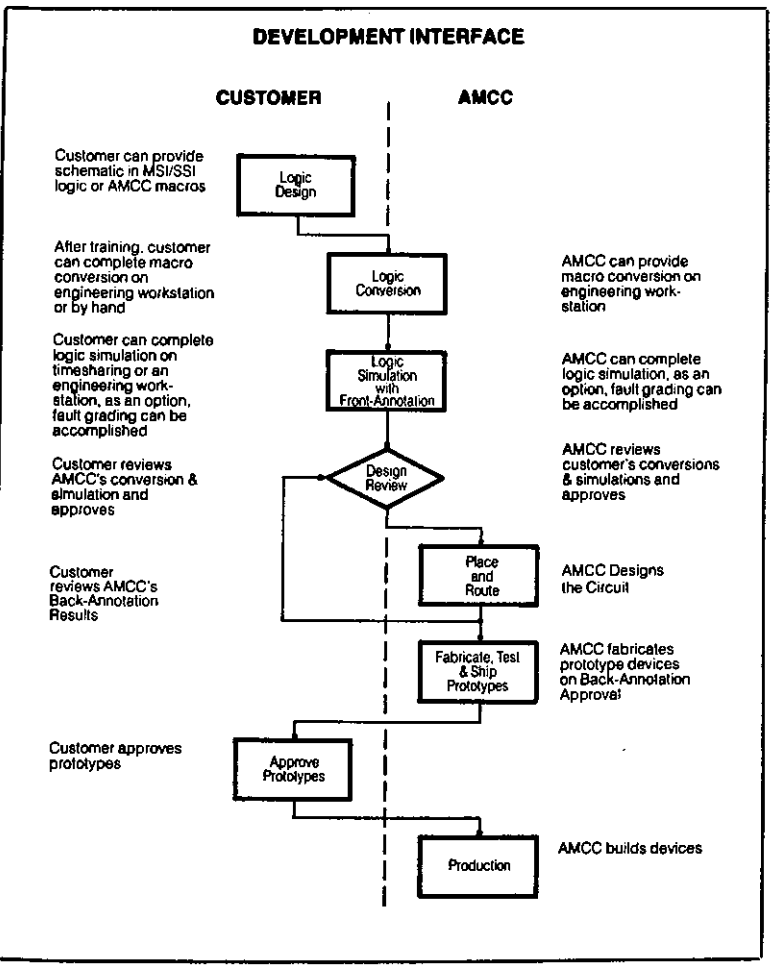

FIGURE 1-1

Section 2:

Design Methodology

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FIGURES

TABLES

DEVICE ARCHITECTURE

The AMCC logic arrays are formed from a customer specified design added to an AMCC pre-processed silicon base array. The base array for the Q5000T, Q3500T and Q1300T arrays is composed of logic and I/O cells. The QM1600T base array also contains the two 640-bit static RAM modules.

TABLE 2-1
Q5000 SERIES CELL RESOURCE SUMMARY

Cell Type	Quantity			
	Q5000T	Q3500T	Q1300T	QM1600T
Logic (L)	352	242	84	114
Interface (I/O)	160	120	76	106
Bits RAM	-	-	-	1280

The basic layout of the arrays is shown in Figure 2-1. Table 2-1 summarizes the internal cell resources and Table 2-2 summarizes the I/O resources for the Q5000 logic array series.

Each cell consists of a number of uncommitted transistors and resistors, with each cell type designed to support high-speed requirements. Unused cell sites do not use any power.

TABLE 2-2
Q5000 SERIES I/O AND POWER-GROUND RESOURCES

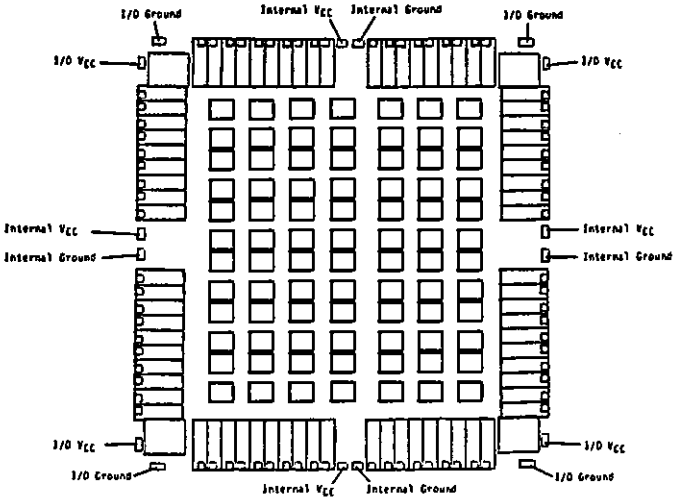
MODE	DESCRIPTION	Q5000T	Q3500T	Q1300T	QM1600T
INTERNAL CELLS		352	242	84	114
100% TTL	I/O Cells	160	120	76	106
	CORE V+ (+5V)	4	6	4	6
	CORE GND (0V)	4	6	4	6
	I/O V+ (+5V)	4	4	4	4
	I/O GND (0V)	12	12	4	12
100% ECL -5.2V or -4.5V	I/O Cells	160	120	76	106
	CORE GND (0V)	4	6	4	6
	CORE V- (**)	4	6	4	6
	I/O GND (0V)	16	16	8	16
100% ECL +5VREF	I/O Cells	160	120	76	106
	CORE V+ (+5V)	4	6	4	6
	CORE GND (0V)	4	6	4	6
	I/O V+ (+5V)	16	16	8	16
MIXED ECL/TTL -5.2V or -4.5V	I/O Cells	160	120	76	106
	CORE GND (0V)	4	6	4	6
	CORE V- (**)	4	6	4	6
	I/O V+ (+5V)	4	4	4	4
	I/O GND (0V)	12	12	4	12
MIXED ECL/TTL +5VREF	I/O cells	160	120	76	106
	CORE V+ (+5V)	4	6	4	6
	CORE GND (0V)	4	6	4	6
	I/O V+ (+5V)	8	8	4	8
	I/O GND (0V)	8	8	4	8

** CORE V-: -5.2V FOR STD-REF ECL 10K
-4.5V FOR STD-REF ECL 100K

The number of fixed power and ground pads for a given I/O mode and a given array is displayed on the chip macro for that array and I/O mode.

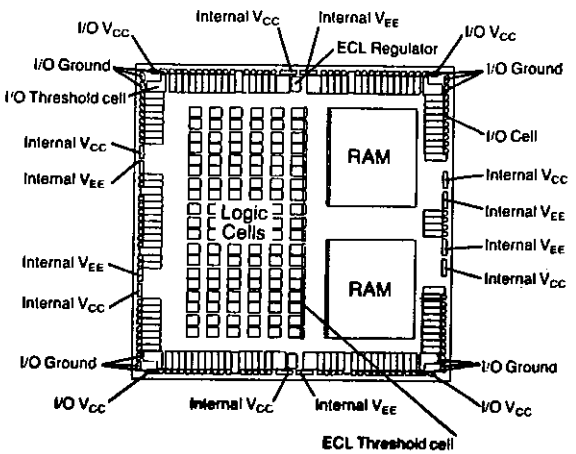
Cell and pad usage is reported by the population ERC.

Q1300T



Die Size: 225 x 213

QM1600T DIE ORGANIZATION

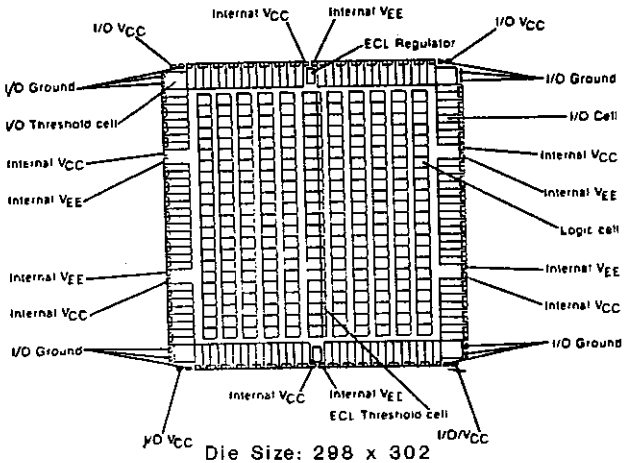


Die Size: 294 x 294

FIGURE 2-1a

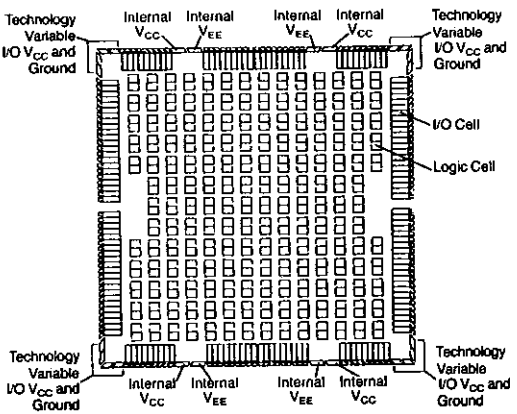
Q5000 SERIES DIE PLOTS

Q3500T



Die Size: 298 x 302

Q5000T



Die Size: 354 x 354

FIGURE 2-1b

ARCHITECTURE - CONTINUED

Macros are individually configured by interconnecting the components within a cell with the first layer metal to form the customer-selected macro functions. Placement is performed by a combination of manual and autoplace routines. Preplacement requests, pin-out requests, package selection (and the corresponding package-specific placement restrictions), macro placement rules and bus current limits are integrated in this process. Manual preplacement is performed for I/O macros, MSI macros, and for critical or distortion sentitive paths.

Placement rules include allowed pads when an array is less than 100% I/O utilized and will be placed in one of the smaller packages, allowed pads for added power and grounds when the package has internal package planes, allowed pad pairs for dual cell macros, 3-state enable placement, interspersement of added power and grounds within the distribution of simultaneously switching outputs and separation of ECL inputs from simultaneously switching outputs. For more details on the placement rules for a specific array and I/O mode in a specific package, consult AMCC.

Customization is performed by adding a 3-layer metal interconnect for the Q5000T or 2-layer metal interconnect for the other arrays in the T series, combining the customer-specified AMCC macros and the base array.

Interconnections between macros (routing) use both the first and second layers of metal, following specific routing tracks. Routing is performed automatically by AMCC proprietary CAD software. To allow for a high logic cell utilization and an optimum layout for high-speed

logic designs, a liberal allocation of first metal vertical routing tracks and second metal horizontal routing tracks have been incorporated into the architecture of each array.

CELL LOCATIONS

The core of each AMCC array consists of logic cells organized in a row-column configuration. The L cells are located in the center of the arrays (see Figure 2-1), and the I/O cells around the periphery. For all arrays, ECL- and TTL-translators and most of the required buffers are included in the I/O cells for external interfacing to both ECL and TTL.

LOGIC MACROS

The L cells are organized to provide high-level logic functions such as latches, multiplexors, decoders, etc. Simple and complex gates can also be made from these cells. Refer to the macro summary and index (Section 6) for a list of the macros available for the Q5000 Series Logic Arrays. The library and its summary sheets are for use during macro conversion or when creating a new design directly from the available functions.

MSI MACROS - HIERARCHICAL MACROS

The macro summary in Section 6 specifies the cell type and cell utilization for each macro listed. MSI macro listings specify the number of cells required to support the macro. MSI macros are hierarchical, multiple-cell macros. They increase design density (equivalent gate count) by as much as 40% over designs constructed solely from the more basic macros, while reducing design partitioning and macro-conversion efforts.

The MSI approach also may result in lower power or higher speed than is obtainable with the equivalent basic macro designs.

CHARACTERIZING THE ARRAY - THE CHIP MACROS

The AMCC EWS schematic convention for the specification of the array and its I/O mode, power supply, product grade, and circuit identification (MILitary or COMmercial) is through the use of a CHIP MACRO. Refer to EWS Schematic Rules and Guidelines (Section 3 in Volume II) for placement and hook-up procedures.

The chip macros each carry the pads designated for use by the fixed power (V_{CC}) and ground (V_{EE}) pins required for that particular array and the specified I/O mode. Any power and ground pins added by the user are in addition to the fixed power and ground requirements. Signals cannot be placed on the pads designated as being fixed power or ground pads.

I/O CAPABILITY

The interface to the arrays is accomplished in the input/output cells on the Q5000 Series Logic Arrays. Each individual I/O cell is configurable to be either TTL, ECL 10K or ECL 100K. The 3-state enable-drivers, both externally driven and internally driven, are also placed on I/O cells.

The array itself can be configured to be 100% TTL, 100% ECL 10K, 100% ECL 100K, TTL/ECL 10K or TTL/ECL 100k, with either dual power supplies or a single +5V supply available for either the 100% ECL or mixed mode I/O circuits. (See Table 2-4.)

TABLE 2-3
POWER/GROUND PAD ASSIGNMENT

MODE:	TTL V_{CC}	TTL GND	ECL V_{CC}	INT V_{CC}	INT V_{EE}
100% TTL	+5V	0V	0V	+5V	0V
100% ECL	0V	0V	0V	0V	-5.2V**
TTL/ECL	+5V	0V	0V	0V	-5.2V**
TTL/+5V ECL	+5V	0V	+5V	+5V	0V

** or -4.5V for ECL 100K

TABLE 2-4
POWER SUPPLY OPTIONS

	SINGLE POWER SUPPLY			DUAL POWER SUPPLY	
	+5V	-5.2V	-4.5V	+5V/-5.2V	+5V/-4.5V
100% TTL	•	-	-	-	-
100% ECL 10K	•	•	•	-	-
100% ECL 100K	•	•	•	-	-
ECL 10K/TTL	•	-	-	•	•
ECL 100K/TTL	•	-	-	•	•

Note: there are placement restrictions when mixing ECL 10K and ECL 100K on a single array. If you are doing preplacement, consult AMCC.

NOISE CONTROL

In an ASIC array, output buffers with a high capacitive load have a slower transition and longer-lasting transients which can cause an interface bus transient to be reflected into the internal busses. For this reason, in the larger AMCC arrays, the power busses supporting the internal array are isolated from the busses supporting the peripheral I/O cells. The threshold and reference voltage generators for the logic array and I/O cells are also independent to insure noise immunity.

In the Q1300T, the ECL VCC and the TTL GND busses are tied together on the array for all standard reference I/O modes. For +5V reference ECL modes, the ECL VCC and the TTL VCC busses are tied together. For all other arrays, the busses are internally separate.

The problem of interface bus noise due to one macro switching is magnified when there are many output macros switching. To minimize this problem, there is a limit of the number of simultaneously switching output macros that can be placed in an array quadrant given the use of the fixed power and ground pads. When it is necessary to exceed this number, there are macros available to provide extra TTL power (ITPWR), TTL ground (ITGND), and ECL power or ground (IEVCC).

The identification of simultaneously switching macros or groups of macros and the use of sufficient added power and grounds for the individual groups is required.

ADDING EXTRA TTL V_{CC} - TTL GROUND PAIRS (ITPWR-ITGND)

As a design guideline for 100% TTL circuits and for mixed mode ECL/TTL circuits, the designer should allocate a minimum of one additional TTL V_{CC} pad and one TTL GROUND pad to any quadrant of the chip that has more than eight (8) simultaneously switching TTL outputs. An additional pair is required for each additional eight (8) simultaneously switching outputs in that same quadrant. (See Table 2-5.)

TTL outputs are considered to switch simultaneously if they switch within 3ns of each other.

ADDING EXTRA ECL IO VCC (IEVCC)

As a design guideline for any standard reference or +5V reference ECL circuit, the designer should allocate a minimum of one additional ECL VCC pad to any quadrant of the chip that has more than eight (8) simultaneously switching ECL outputs. An additional ECL VCC (IEVCC) is required for each additional eight simultaneously switching ECL outputs in that same quadrant. (See Table 2-5.)

ECL outputs are considered to switch simultaneously if they switch within 2ns of each other.

TABLE 2-5
ADDITIONAL POWER/GROUND
Q5000 SERIES

# OF SIMULTANEOUSLY SWITCHING TTL OUTPUTS PER QUADRANT	ADD TTL V_{CC} - TTL GROUND ADDED ITPWR - ITGND PAIRS
0 - 8	0
9 - 16	1 (2 pins)
17 - 24	2 (4 pins)
25 - 30*	3 (6 pins)
# OF SIMULTANEOUSLY SWITCHING ECL OUTPUTS PER QUADRANT	**ADDED IEVCC**
1 - 8	0
9 - 16	1 (1 pin)
17 - 24	2 (2 pins)
25 - 30*	3 (3 pins)

* There is a MAXIMUM of 40 I/O cells per quadrant in the Q5000T array. A maximum limit of 30 cells per quadrant may be used as outputs for this array. For the other arrays in the series, the number of cells per quadrant is less than 30 and there are no restrictions of the use of those cells.

Added ground pins must be interspersed with the simultaneously switching signals. For the Q5000T array, added power and ground pads must be pads that can bond to a package place. This requirement is not considered restrictive. Placement requirements for added power and ground pads are package-specific. If you are doing placement, consult AMCC.

SPECIFYING ADDITIONAL POWER AND GROUND

When additional power and ground pads are desired on an array, the power macros, ITPWR or IEVCC, and the ground macros, IEVCC or ITGND, are placed on the schematic in the quantity desired. (Place on the same page as the chip macro.) IEVCC will be considered a power pad for +5V REF ECL circuits and a GROUND pad for STD REF ECL circuits.

The added power and ground macros each occupy one I/O cell and use its pad.

The AMCC MacroMatrix Population ERC check will correctly reflect the cell count and the array pad count resulting from the use of these macros. Inclusion of the requirements for extra power and ground is part of the required design submission documentation.

When the added power and ground is for simultaneously switching circuits, use the macro parameter SWGROUP to tag these macros to the group to which they belong. The ERCs cannot issue error or warning messages on insufficient power or ground if the parameter is not used.

The population ERC will report the number of array PADS used by a circuit (currently labeled as External Pins); the sum of all fixed power and grounds; all added power and ground; and all interface signals.

FIGURE 2-2
POWER and GROUND MACROS

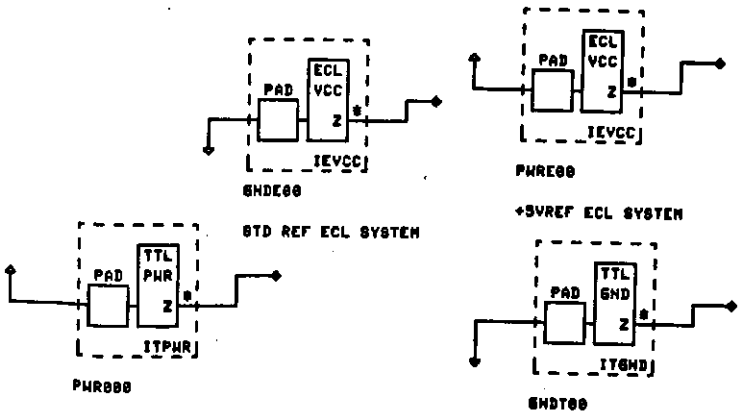


TABLE 2-6
EXTERNAL PADS

ARRAY	FIXED POWER-GROUND PADS	SIGNAL I/O PADS	TOTAL EXTERNAL PADS
Q5000T	24	160	184
Q3500T	28	120	148
QM1600T	28	106	134
Q1300T	16	76	92

INTERFACE GUIDELINES

A summary of the interface guidelines for the four I/O modes of operation are shown in Figure 2-2. Most of the I/O macros for the Q5000 Series include buffer functions, to simplify I/O selection. The designer should review the I/O options to determine where these options would enhance the circuit efficiency.

The AMCC MacroMatrix ERC technology ERC report will list errors due to improper selection of macros based on the I/O mode selected via the chip macro.

Q5000 SERIES INTERFACE MACRO GUIDELINES

100% TTL INTERFACE
Single +5V Power Supply

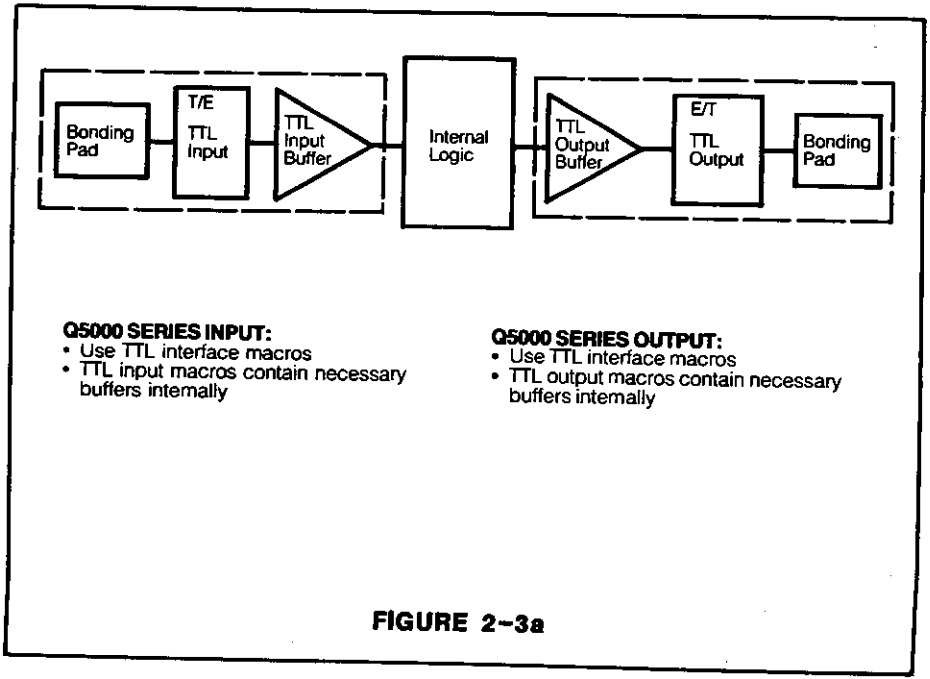
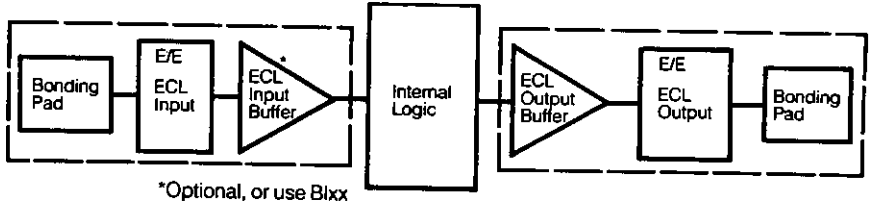


FIGURE 2-3a

Q5000 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

100% ECL INTERFACE
Single −5.2V, −4.5V
or +5V Power Supply

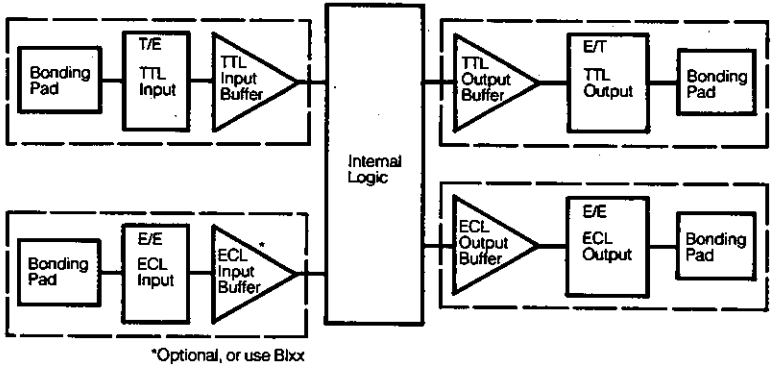


Q5000 SERIES INPUT:
- Use ECL interface macros (IExx)
- ECL input macros contain necessary buffers internally or require a separate buffer in a logic function (BIxx)
- Same macro for either +5V, −5.2V or −4.5V supply

Q5000 SERIES OUTPUT:
- Use ECL interface macros
- ECL available in 50 and 25 ohm terminations
- ECL output macros contain necessary buffers internally
- Supports both ECL 10K (OExx) and ECL 100K (OKxx)
- Same macro for either +5V, −5.2V or −4.5V supply

FIGURE 2-3b

MIXED ECL/TTL INTERFACE
Single +5V Power Supply



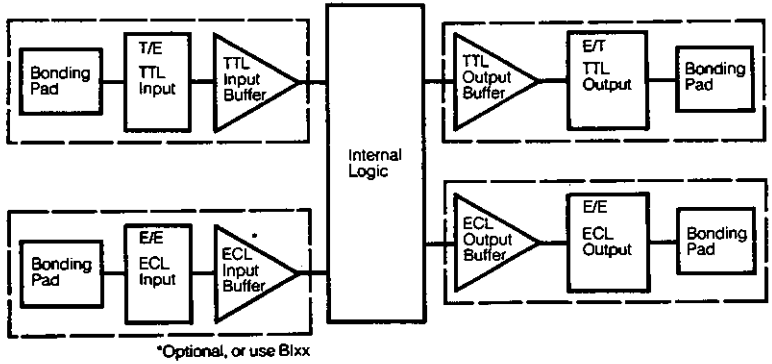
*Optional, or use BIxx

Q5000 SERIES INPUT:
- TTL: Identical to guidelines for 100% TTL circuits
- ECL: Identical to guidelines for 100% ECL circuits

Q5000 SERIES OUTPUT:
- TTL: Identical to guidelines for 100% TTL circuits
- ECL: Identical to guidelines for 100% ECL circuits

FIGURE 2-3c

MIXED ECL/TTL INTERFACE
+5V and −5.2V Power Supply
or +5V and −4.5V Power Supply



Q5000 SERIES INPUT:
- TTL: Identical to guidelines for 100% TTL circuits except use TTLMIX macros
- ECL: Identical to guidelines for 100% ECL circuits

Q5000 SERIES OUTPUT:
- TTL: Identical to guidelines for 100% TTL circuits except use TTLMIX macros
- ECL: Identical to guidelines for 100% ECL circuits

FIGURE 2-3d

MACRO SUMMARY

The macro summary in Section 6 is divided into five segments: TTL, TTLMIX, ECL, Internal Logic and Special macros. For +5V only circuits, the TTL macros are selected from the TTL section, Section 6-1. For dual power supply circuits, the TTL macros are selected from the TTLMIX section, Section 6-2. The ECL macros are selected from the ECL section, Section 6-3. The same ECL macros are available for use with standard reference voltage or for +5V reference voltage circuits.

TTL INPUT (ITxx macros)

Q5000 Series TTL input macros contain input buffers. TTL level detection is performed in this input macro. For circuits with a single +5V power supply, the buffer provides the signal buffering required to drive internal circuits. For dual power supply circuits, the buffer also provides signal translation from TTL input levels to the internal signal level needed by the array, which operates with a negative power supply.

Note: TTL inputs that invert such as ITll must be driven from a totem-pole source or from a voltage with $V_H \geq V_{CC}$ - 0.5V. This restriction does not apply to TTL MIX macros.

TTL OUTPUT (OTxx macros)

The Q5000 Series arrays provide 20mA current sink, 1mA current source capability. The TTL output is differentially driven by buffered logic that is part of the TTL output macro.

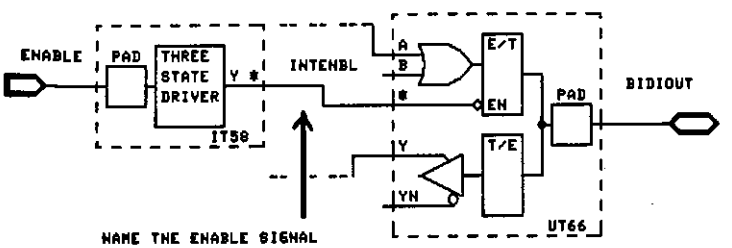
The Q5000 Series arrays handle TTL totem-pole, open-collector and 3-stated output options. The 3-state output macro enable pin must be driven by a 3-state enable-driver and the signal driving the pin must be named on the schematic and must be listed in the simulation signal format.

BIDIRECTIONAL TTL (UTxx macros)

The Q5000 Series I/O cell supports bidirectional I/O. The input and output functions follow the same design methodology as the ITxx and OTxx macros. A three-state enable driver is required to drive the enable. The signal driving the enable must be named on the schematic and must be listed in the simulation signal format.

FIGURE 2-4
BIDIRECTIONAL TTL I/O

Note the use of the bidirectional connector (this is the DAISY EWS version). Each EWS has a specific connector for bidirectional I/O and it must be used. Note the name on the wire connected to the EN pin. Its use is required.



ECL INPUT (IExx macros)

For ECL input, the output of the RC compensation network provided by the input portion of the macro is buffered by either a buffer on the input macro or by the BIxx ECL input buffered logic macros. ECL inputs function in the same manner on circuits which have +5V referenced ECL input with a single +5V power supply.

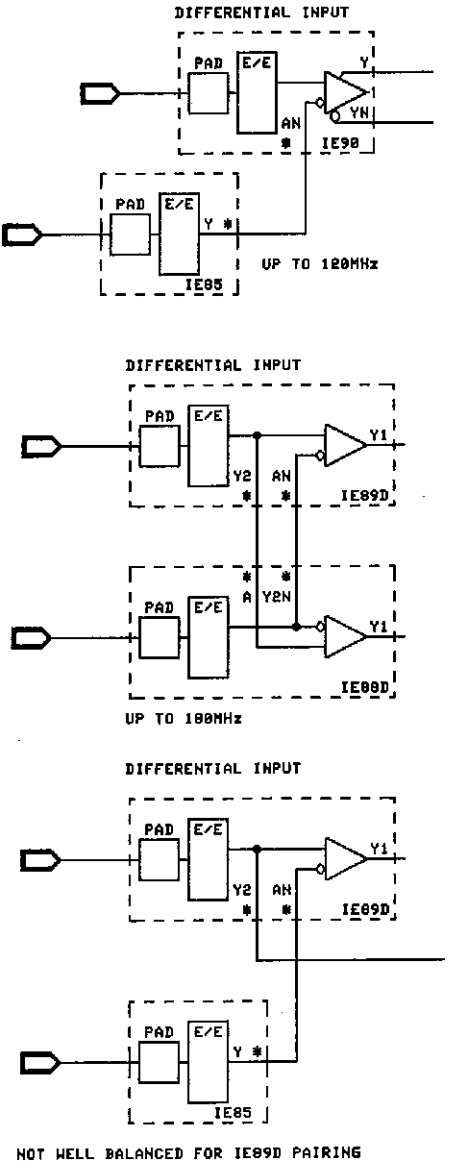
For ECL input operation at 160MHz and above, differential ECL input macros are strongly recommended. For ECL operation at 240MHz and above, differential ECL inputs are required. ECL differential inputs are also required when the signal source is remote from the array.

There are a number of different macros and macro-pairs that may be used for ECL differential input. Table 2-7 provides a list of the macros that are available and the frequency limit for that macro. When a pair of macros is used to form a differential pair, the macros must be placed adjacent to each other.

TABLE 2-7a
DIFFERENTIAL ECL INPUT MACRO SELECTION

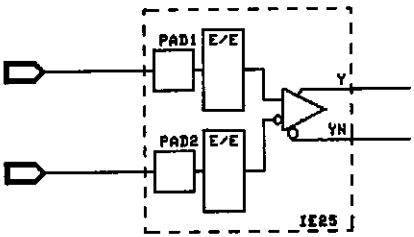
MACRO/MACRO PAIR	MHz LIMIT
IE90 with IE85	≤ 120 <--| placement
IE88D with IE89D	≤ 180 <--| restrictions
IE25 dual cell	≤ 360
IE27D dual cell *	≤ 360
IE28D dual cell *	≤ 360
IE99V dual cell	≤ 600

* some macros listed may not yet be released for the Q5000 Series Library - consult AMCC if you need them.

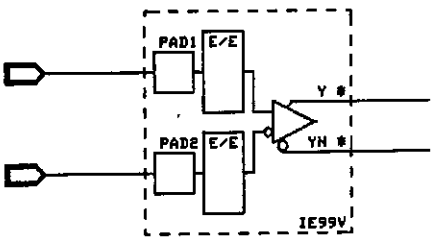


DIFFERENTIAL ECL INPUT

FIGURE 2-5



DIFFERENTIAL INPUT - UP TO 360MHz



DIFFERENTIAL INPUT - UP TO 600 MHz COMMERCIAL
UP TO 450 MHz MILITARY

FIGURE 2-5 continued

ECL OUTPUT (OExx, OKxx macros)

All ECL outputs require a buffer, and the buffer is included in the output macro. The Q5000 ECL output buffers drive 50 ohm or 25 ohm ECL outputs. The 25 ohm ECL output macros are not released. They are dual-cell output macros. Consult AMCC if you require 25 ohm terminations.

ECL output macros are grouped by logic function in Section 6. A specific version of the macro (OExx or OKxx) is selected based on ECL type. (See Table 2-8.)

For ECL output operation at 100MHz and above, pulse distortion minimization methods should be used. These include: 1)signal inversion on alternating macros; 2) short interconnect, a function of fan-out, wire-OR and metal length; and 3) balanced rising-edge and falling-edge k-factors.

As with ECL input, differential ECL output requirements depend on the chip environment as well as the operating frequency. For operating frequencies of 180MHz and higher, use OE10, a dual-cell ECL differential output. For lower speeds, when differential outputs are required, the OE80 or other OExx macro pairs may be used. The macros acting as a differential pair must be adjacent on the chip layout. Refer to Table 2-7b.

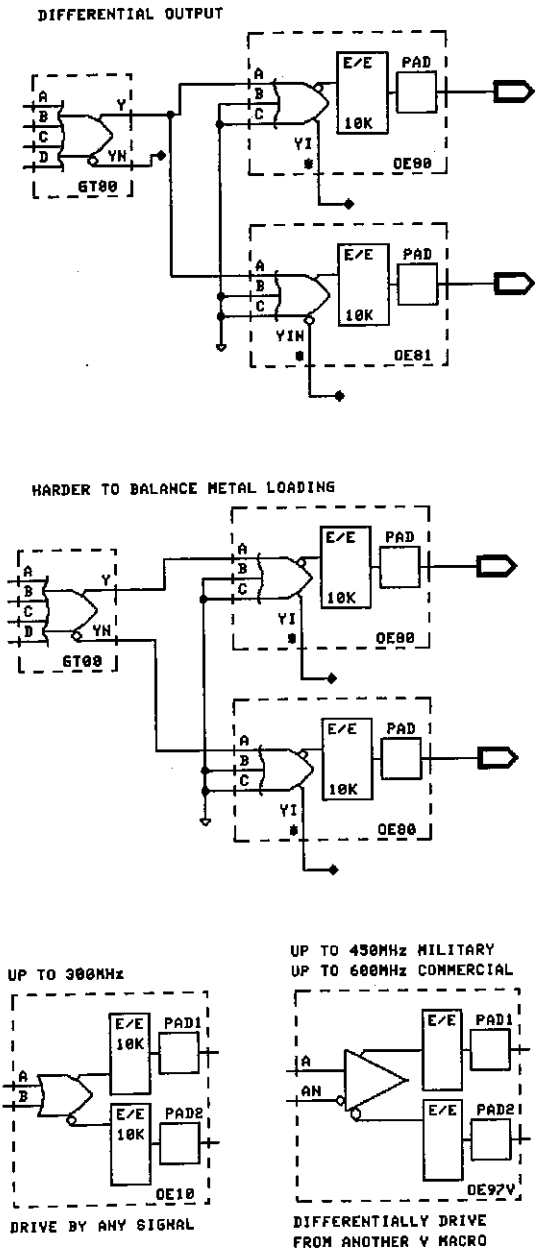


FIGURE 2-6 ECL OUTPUT

TABLE 2-7b
DIFFERENTIAL ECL OUTPUT MACRO SELECTION

MACRO/MACRO PAIR	MHz LIMIT
OExx (any pair)	≤ 180 <--| placement
OE10 dual cell	≤ 360 <--| restrictions
OE97V dual cell	≤ 600

For non-V macros, the minimum swing across differential inputs is 250mV. The minimum swing across the outputs is defined on the data sheet. The maximum input voltage is V_{CC} - 0.5V. The maximum output voltage is defined on the data sheet.

For the V macros, for commercial operation with $T_j \leq 130^oC$, the output swings are shown below:

TABLE 2-7c
V MACRO DIFFERENTIAL OUTPUTS

FREQUENCY	MINIMUM OUTPUT SWING
MHz	mV
600	200
500	250
400	300
300	350

	S	V
Delta V_{in}MIN	250	200
V_{in}MAX	VCC-0.5	VCC-0.5
Delta V_{out}MIN	(1)	(2)
V_{out}MAX	(1)	

(1) see data sheet
(2) listed above in Table 2-7c

For V macro inputs, a differential 200mV swing is required.

TABLE 2-8
ECL MACRO 10K/100K SELECTION

Q5000 Series	ECL 10K		ECL 100K	
	+5V REF	GND REF	+5V REF	GND REF
INPUTS	IExx	IExx	IExx	IExx
OUTPUTS	OExx	OExx	OKxx	OKxx
Bi-direc.	UExx	UExx	UKxx	UKxx

BIDIRECTIONAL ECL (UExx, UKxx macros)

The Q5000 Series I/O cell supports bidirectional ECL I/O. The input and output functions follow the same design methodology as the IExx and OExx/OKxx macros. Unlike TTL, where the 3-state enable driver is required to drive the enable, the enable on the bidirectional ECL macros may be driven by any internal logic signal. The signal driving the enable must be named on the schematic and must be listed in the simulation signal format.

+5V REFERENCED ECL/TTL

AMCC offers the option of having ECL 10K or ECL 100K available with the use of a single +5V power supply. The ECL logic threshold levels are shifted, but retain their high-speed characteristics. This +5V referenced ECL mode allows the partitioning of a high-speed TTL design into multiple AMCC devices using a single +5V supply, while providing high-speed ECL I/O between the arrays on the same PC board and full system TTL compatibility.

UNBUFFERED ECL INPUT

Selected unbuffered ECL input macros have a fan-out of eight (8) and the distinction that there is no propagation delay penalty for the fan-out load (the k-factor of the output pin is zero). However, input capacitance will increase at the rate of 1pf per fan-out. This input capacitance will be seen by the external circuit driving the package pin connected to the unbuffered ECL input.

ALTERNATIVE ECL TERMINATIONS

The standard ECL termination is 50ohms tied to V_{TT}, where V_{TT} = -2.0V for standard reference ECL. An alternative termination is 80ohms to ground with 130 ohms to V_{EE} where V_{EE} = -5.2V. For other termination configurations, consult AMCC.

SIGNAL BALANCING; DISTORTION MINIMIZATION

The case where two paths are required to be identical in performance is common. The best results are obtained when the macros are identical macros (identical k-factors implied), are identically loaded, including identical wire loads for metal 1 and metal 2, and are placed in the same quadrant and close together in that quadrant.

Since placement cannot be assumed to be able to solve all problems in all cases, the judicious use of parallel structures (such as buffer trees) to reduce loading in a path, avoidance of wire-ORs in these paths, and the use of pulse distortion minimization techniques, such as inversion of the signal at each macro, will help.

VERY FAST V MACROS

A special class of ECL input, ECL output and internal logic macros exist in the (804) release known as the V macros or "Very Fast Macros". These macros are specified with a maximum frequency of operation of 600MHz. There are certain design rules which must be followed when they are used in a design.

1. The outputs of all V macros are differential and must drive a differential input pair. In most cases this will be another V macro.

2. To convert from a V macro into non-V macro logic a V macro may drive either a GT64 or a GT66, differential input macros that can in turn drive any non-V macro in the library.

3. To convert from a non-V-macro into a V-macro use GT67V which provides the proper differential output. GT67V cannot drive a non-V macro.

4. The outputs of V macros are ECL differential one-half range swing. For internal outputs the swing is 250mV. For primary outputs, refer to Table 2-7c. This class of output is marked with an "*".

5. The outputs of the V macros cannot be powered-down. If an output is terminated, the AMCC ERC software will compute power-down and will not flag an error at this time. [MANUAL CHECK]

6. The outputs of V macros cannot be wire-ORed. This will be detected by the AMCC ERC software.

7. All V macro inputs are differentially driven. Internal macro inputs must be driven by other V macros.

8. The number of V macros that can be placed on an array is subject to the same maximum internal current and population checks as other macros. There are no special restrictions.

9. Placement restrictions for V macro inputs and outputs are the same as for other dual-cell, dual pad input and output macros. There are no unique placement restrictions for internal V macros.

10. As a guideline, keep interface V macros near a ground or add one. This is not required.

11. There are no AC tests for V macros at this time.

INTERNAL FAN-OUT

Each internal macro output pin is specified to drive a maximum fan-out load. Maximum fan-out limits are specified in the macro documentation in Section 6. A summary of fan-out capabilities is shown in Table 2-9.

TABLE 2-9
FAN-OUT SUMMARY

MACRO TYPE, OPTION	MAXIMUM FAN-OUT LIMIT
Input macros, unbuffered TTL	1
Input macros, unbuffered ECL	8
Input macros, buffered, S-, H-option	9
Very Fast Input V macros	9
Input macros, buffered, L-option	4
Logic macros, L-option	4
Logic macros, S-option or H-option	9
Very Fast Logic V macros	9
3-state enable-drivers	8
High fan-out drivers	15
Super Drivers	25

INTERNAL FAN-IN

Unless otherwise identified by an "*" on the input pin, any internal macro input represents one electrical load and any output macro input pin represents one electrical load.

Where the graphic may lead to confusion by showing connections to indicate two loads when there is one or by showing one load when the load is greater than one, the input pin is tagged with an "*" and a comment added to the macro description in Section 6.

DERATING FAN-OUT LIMITS

For clock or distortion-sensitive paths, at speeds up to 160MHz, the maximum fan-out for each macro output pin in the path must be derated by 20%. For clock paths at speeds equal to or greater than 160MHz, the maximum fan-out should be derated by 40%. For logic macros driving unbuffered TTL output macros, the maximum fan-out must be derated by 20%.

Macros with a k-factor of zero are not derated nor are 3-state enable drivers. Super-drivers, those high-fan-out drivers with a fan-out load limit of 25 loads, are not derated, regardless of the system operating speed. V macros are similar to drivers and are not derated.

Fan-out load limits are checked by the AMCC MacroMatrix ERC software. To allow derated fan-out load limit checking, use the FOD parameter on the net and assign the derating value (20, 40, etc.) as its value.

TABLE 2-10
DERATING GUIDELINE

OPERATING SPEED:	DERATE BY:	FOD VALUE
<160MHz	20%	20
≥160MHz	40%	40

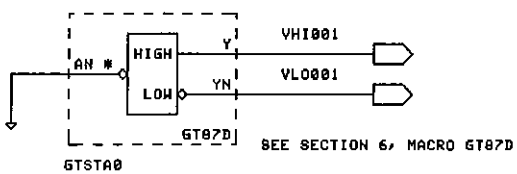


FIGURE 2-7 STATIC DRIVER

INTERNAL FAN-OUT - STATIC SIGNALS

In cases where it is desired to tie a macro input pin to "1" or to "0", the procedure is as follows:

To tie an unused macro input pin LOW (to "0"):

- For macro input pins that may be grounded, tie to global ground (allow to "float")

- For macro pins with hook-up restrictions (MUST BE DRIVEN pins) tie to either an available L-option or S-option "OR" gate (inputs grounded) or to the static low signal provided by the static driver macro, GT87. The load limit for an L-option macro is 4 loads, the load limit for an S-option macro is 9 loads and the load limit for GT87 static low is 32 static loads. Name a static low signal VLOxxx.

To tie an unused macro input pin HIGH (to "1"):

- For any pin that must be driven to "1", tie to either an available L-option or S-option "NOR" gate (inputs grounded) or to the static high signal provided by the static driver macro, GT87. The load limit for an L-option macro is 4 loads, the load limit for an S-option macro is 9 loads and the load limit for GT87 static high is 32 static loads. Name a static high signal VHIxxx.

AMCC MacroMatrix ERC reports on hook-up, unused pins and pin class will list errors due to improper connections including improper grounding of unused input pins.

WIRE-ORS

Macros may only be wire-ORed with the component macros WIREOR2, WIREOR3 and WIREOR4. No wire-OR can have more than four (4) inputs. Wire-ORs may not be cascaded (one wire-OR feeding into another). EWS parametric wire-ORs are NOT allowed.

The outputs of most of the Q5000 Series macros may be wire-ORed. Macros that CANNOT be wire-ORed are: macros whose fan-out limit is one (1); unbuffered input macros such as IE85; high fan-out drivers; super-drivers; and 3-state enable-drivers; some latches (marked with an *); some flip/flops (marked with an *); all V macros; and some MSI macro outputs.

Individual macro output restrictions can override a general rule, and all restrictions are documented in Section 6.

Wire-ORing two macros together does not increase their fan-out capability, since all but one output emitter-follower current source will be powered-down. When a mix of H-option, L-option and S-option macros appears in a wire-OR, the fan-out load limit and all other loading parameters will follow the rules for the highest drive macro (i.e., the H-option macro will be considered to be the driving macro).

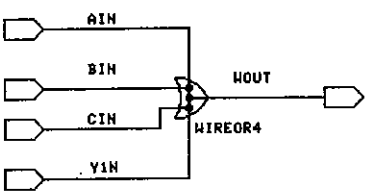


FIGURE 2-8 WIRE-OR4

THERMAL DIODE MACROS

There are three thermal diode macros: GT99, IE86 and OE87. The macros are used in a core approach, shown in Figure 2-9, or in an I/O approach, shown in Figure 2-10.

The IE86 macro consists of four thermal diodes of varying sizes. The PAD is tied to the annodes of all four of these diodes. The desired thermal diode is selected by the output connection. Three of the outputs will be terminated.

TABLE 2-11
THERMAL DIODE CONNECTION VALUES

OUTPUT	DIODE Q3500 SERIES	Q5000 SERIES
Y0	minimum sized transistor = x (typical of core array devices)	
Y1	3.5x	4x
Y2	8x	9.5x
Y3	15.5x	17.5x

The output selected on the IE86 should be tied to the input of an OE87.

PLACEMENT: This macro pair (IE86, OE87) should be placed close to each other with no more than 3 I/O macros/cells placed between them.

The GT99 is a core macro and consists of a minimum sized transistor. Connect this macro with two OE87 macros. The base is tied to the collector (B to C) to form the annode. The emitter (E) becomes the cathode of the diode.

PLACEMENT: The GT99 macro can be placed anywhere in the core of the array without restriction. The OE87 macros should be as close as possible to the GT99.

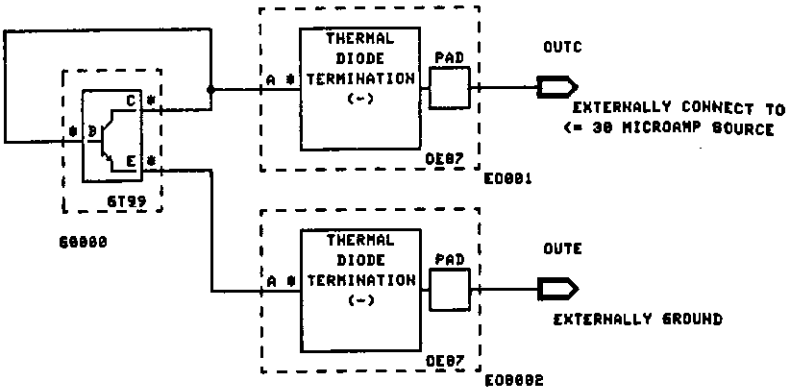


FIGURE 2-9

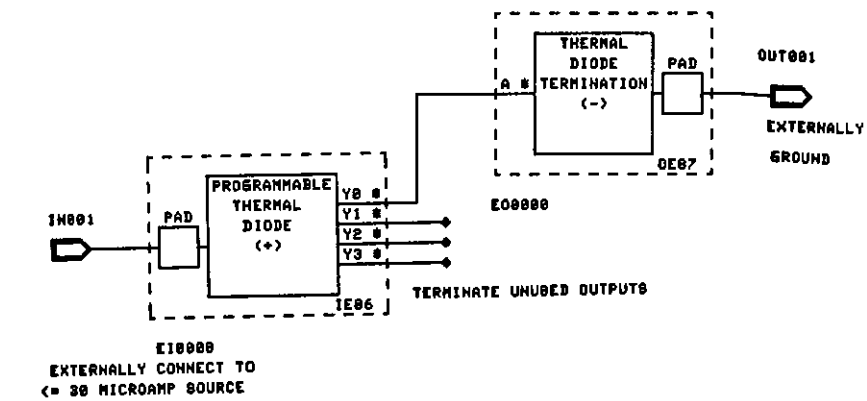


FIGURE 2-10

The common use for these diodes is AC/DC characterization of NREs over transistor junction temperature. In addition, by placing several of these diodes in the I/O and the core, thermal gradients across the chip can be determined.

The following procedure should be followed to characterize thermal diodes over junction temperature:

- Check that all power supplies are turned off.
- Place the packaged part in the test fixture.
- Attach a thermocouple to the top center of the package.
- Apply a known DC current (Il) from the annode to the cathode.
- Apply temperature (Tj) to the package and wait for the part to reach thermal equilibrium.
- Measure Vbe across the diode.
- Repeat the last two steps for at least 5 temperatures. The Vbe will decrease linearly with increasing temperature.
- Determine the value for k in the equation:

$$Vbe = Vbe0 - K * Tj$$

where:

Vbe0 = Vbe at 0 degrees Celsius
K = constant
Tj = junction temperature in degrees Celsius

For maximum thermal characterization accuracy, this procedure should be repeated on every part to be characterized.

Once this procedure has been carried out on a part, characterization over junction temperature may be performed. This is done by applying the same current Il through the junction diode, applying power to the part, and then measuring Vbe across the diode. Plug this Vbe value into the above equation and solve for the junction temperature Tj.

INTERNAL CELL UTILIZATION

To insure routability, the recommended maximum internal cell utilization (cell population) for arrays in the Q5000 Series is 95%. Starting designs should target a 75% internal cell utilization to allow for the typical 20% design expansion during debug, re-design, enhancement, and testing logic additions. Designs in excess of 95% internal cell utilization for these arrays are considered risky if their internal pin count exceeds recommended limits.

Compute internal cell utilization by first summing the number of L cells used by the circuit, and then by dividing that sum by the number of L cells available for the particular array.

AMCC MacroMatrix ERC software computes the internal cell utilization.

TABLE 2-12
MAXIMUM INTERNAL CELL UTILIZATION
L CELLS

ARRAY	%
Q5000T	95
Q3500T	95
Q1300T	95
QM1600T	95

INTERNAL PIN COUNT

The internal pin count is a measure of the routability of a circuit for a given array.

- Prior to schematic capture, the internal routable pin count should be estimated and used to determine the array required. In this case, refer to the ESTIMATED limits in Table 2-13.

- After capture, the AMCC MacroMatrix ERC software provides a detailed report on the internal pin count of the circuit. For a captured circuit, refer to the ACTUAL limits in Table 2-13.

TABLE 2-13
MAXIMUM INTERNAL PIN COUNT
I/O AND L CELLS

ARRAY	ACTUAL	ESTIMATED *
Q5000T	3572	3393
Q3500T	2470	2346
Q1300T	906	860
QM1600T	1200	1140

* Estimated = 0.95 * actual
Actual = ((# L cells) * 10
+ (# I/O cells) * 1.5) * 0.95
Estimated assumes expansion as the design is completed

- A circuit with an actual internal pin count that is less than the limit is routable.

- A circuit with an actual pin count that is 1-10% over the limit is considered risky (may have problems).

- A circuit with an actual pin count of 11-18% over the limit is considered very risky and may not successfully route.

- A circuit with an actual pin count of 18% or more over the limit is considered unroutable and a redesign or repartitioning is required if a larger array cannot be used.

Q5000 SERIES BASIC DESIGN RULES AND GUIDELINES

Once the macros have been selected, and the basic circuit defined, the designer should review the circuit prior to submission to AMCC to verify that basic design rules have not been violated. Some of these rules and design checks are listed below.

Guidelines are suggestions to help ensure first-design success; rules are design requirements that cannot be violated. For further information, refer to the Design Submission and Design Validation documents, Section 6 and Section 5 of Volume II of this design manual.

- Fan-out - no macro drives more than its rating. Unbuffered input macros are limited to one load. Output buffers are limited to one load.

TABLE 2-14
FAN-OUT SUMMARY

MACRO TYPE	MAXIMUM FAN-OUT
Input macros, buffered H-, S-option	9
Input macros, unbuffered TTL	1
Input macros, unbuffered ECL	8
Input macros, 3-state enable-drivers	8
Logic macros, H- and S-options	9
Logic macros, L-option	4
Very Fast V Macros, logic or input	9
High-fan-out drivers	15
Super-drivers	25

- Fan-out derating - critical clock or distortion sensitive paths have derated clock loading: 20% up to 160MHz; 40% for ≥160MHz. Use the FOD parameter to allow ERC checking.

- Fan-out - high speed differential paths are kept lightly loaded and the loads are balanced.

TABLE 2-15
20%/40% DERATED FAN-OUT SUMMARY

MACRO TYPE, OPTION	20%/40% DERATED FAN-OUT
Input macros, buffered H-, S-option	7/5
Input macros, unbuffered TTL	1
Input macros, unbuffered ECL	8
Input macros, 3-state enable-drivers	8
Logic macros, H- and S-options	7/5
Logic macros, L-option	3/2
Very Fast V Macros, logic or input	9
High-fan-out drivers	12/9
Super-drivers	25

- Fan-out - do not derate 25 load drivers or V macros.

- Static driver - use GT87 or L-option, S-option gate. Gates drive 4 or 9 loads. Static driver can drive 32 static loads, HIGH or LOW.

- Fan-in - any macro with an asterisk on an input pin has been checked for fan-in > 1.

- Pin-restrictions - any macro with an asterisk has been cross-checked to be certain that it is connected to or driven from a legal macro connection. (Some macro input pins cannot be grounded.)

- Wire-OR restrictions - No more than 4 wires per wire-OR and no cascading; all wire-ORs are component wire-ORs.

- Wire-OR restrictions - No driver macros can be wire-ORed and no macro with a fan-out of one or two can be wire-ORed. Certain other macros (whose outputs are flagged with an asterisk) cannot be wire-ORed. No V macro may be wire-ORed.

- Unused macro input pins - EWS convention is to ground any unused inputs and terminate unused outputs, unless the macro documentation indicates that a pin cannot be grounded. (Grounded signals assume low level logic and physically float.)

- Unused macro input pins - Do NOT ground pins that are hook-up restricted. If a pin must be driven by a macro, then a static driver must be used to drive the pin high or low as needed. Refer to the individual macro documentation.

- Unused input to an AND gate - These must be connected to the output of an inverted static driver to drive a logical "1" into the unused input.

- Pin connections - Make certain that input and output pins are properly connected, including PAD connections.

- Bidirectional signals - Be certain that bidirectional macro pins have been connected to a bidirectional connector (EWS convention). Refer to Volume II, Section 7 for additional information.

- Grounded output pins - These are not allowed.

- Terminated input pins - These are not allowed.

- Macro type - Check that the proper TTL I/O macros were chosen based on the circuit type.

- Macro type - Check that the proper ECL versions of the ECL macros were chosen based on the circuit type.

- Signal names - Check that all connections - intra-page, inter-page, off-chip and 3-state and bidirectional enables - have been properly named. Refer to Volume II, Section 3 for naming conventions and rules.

- Cell utilization - Do not violate the 95% internal cell utilization limit without AMCC approval. (Initial designs should target a lower utilization figure to allow for the addition of macros for design changes, debug fixes and testing logic.)

- Output latch restriction - Do not use an ECL output macro latch to build a flip/flop. These macros should only be used as latches.

- Asynchronous data paths - Use FF70, FF71 or FF72 when the data path to a latch or flip/flop is asynchronous. LA70 and LA71 are not released.

- Internal pin count - Do not exceed the array limit and supply AMCC with a total internal pin count.

- Additional power and ground - Provide additional power and ground pins as needed by using the ITPWR, ITGND and IEVCC macros on the schematic. Use the SWGROUP macro parameter to allow the simultaneously switching output ERC check.

- When leaded chip carriers are to be used, care should be taken to supply sufficient ground pins to allow separation of any signals where cross-talk may be of concern, e.g., between input and output signals. Spare pins should be grounded.

- External pin count - Do not exceed the maximum array pad count limit. ITGND, IEVCC, ITPWR macros use cells and pads and are counted. The final external pin count depends on the selected package.

- Input levels - inverting TTL input macros must be driven from a totem-pole source or from a source providing $V_{IHmax} \leq V_{CC} - 0.5V$.

- Power - Do not violate the maximum internal current specification. Compute the circuit internal current and reduce by the powered-down outputs. Do not terminate any V macro outputs.

- Power - Compute the maximum worst case power.

- Packaging - Verify that the package selected is appropriate for the environment and junction temperature (compute based on power).

- Critical paths - Compute and clearly identify the critical paths, specify the critical paths.

- Differential ECL I/O - use when the speed is ≥100MHz or when the signal is remote for +5V REF ECL.

- Differential ECL input - Use the dual-cell macros or the IE88D-IE89D pair placed adjacent on the layout when the speed is greater than 100MHz.

- Differential ECL input - Use the dual-cell macros when the speed is greater than 150MHz but less than 360MHz. (Consult AMCC.)

- Differential ECL input - Use the V macros (dual cell differential) for speeds up to 600MHz (COMMERCIAL) and 450MHz (MILITARY).

- Differential ECL output - Use the dual-cell macros such as OE10 when the speed is greater than 180MHz and less than 360MHz.

- Differential ECL output - Use the V macro (dual cell differential) for speeds up to 600MHz.

- Generate and include reports on macro occurrence, current and power; fan-out; pin count; etc. as indicated in the Design Submission and Design Validation documents. (AMCC MacroMatrix ERC software generates most of these reports.) Refer to Section 8, Volume II. Fill in as required.

- Use a chip macro to characterize the circuit as to array, ECL type and power supply. Follow the rules in AMCC EWS Schematic Rules and Conventions. Refer to Section 3, Volume II.

- Complete simulation documentation must be submitted with the design, including source files. Refer to the Design Submission and Design Validation documents.

- For guidance in constructing simulation vectors, refer to the AMCC document: Vector Submission Rules and Guidelines. Refer to Section 4, Volume II.

- For test vectors, limit the number of simultaneously switching outputs PER VECTOR to 8 for mixed ECL/TTL circuits and 16 for 100% TTL or 100% ECL circuits. This applies to functional vectors and AC test vectors. This is a test limit and not an array limit.

POWER BUS DISTRIBUTION AND DECOUPLING

Optimal Power Bus Distribution and Decoupling is dependent on a number of interactive device and system variables, including the package design used, the number of simultaneous switching outputs on the device, output loading, the amount of switching noise contributed by other system components, the number of power busses and the design of the system and module power distribution.

AMCC recommends the use of multi-layer PC boards that provide dedicated low impedence power and ground planes. Besides maintaining a constant characteristic impedence for transmission lines, the planes provide for a low impedence return path to the ECL or TTL circuitry and act as an electromagnetic shield for the signal lines. The distributed capacitance will also improve noise margins by minimizing "ground bounce" and crosstalk.

The 2-layer PC boards, on the other hand, may require successive approximations to optimize the system noise margins and reduce external noise from being fed back into the chip through the power and ground pins. This approach should only be attempted in lower performance systems.

The I/O ECL V_{CC} and the Internal V_{CC} package pins should be tied together as close to the chip as possible, using good high frequency practices. When mixed I/O is combined with multiple power busses, the TTL GND and ECL V_{CC} (0V) can be tied directly together at the chip on multi-layer boards.

For 2-sided boards, the location will be system dependant and may require some experimentation. The primary considerations are the amount of simultaneous switching, the signal/ground pin ratio and the isolation between the TTL and ECL signal lines (and return paths).

Low frequency (bulk) decoupling is generally provided in the range of 0.5 to 2.0 uf/WATT, while high frequency by-passing should be 100 to 1,000 pF/quadrant. The by-pass capacitors are generally placed as close to the chip as possible using high frequency techniques to minimize the inductance in the leads, traces, feed-throughs and components.

AMCC's Q3500 performance boards use a luf tantalum in parallel with a 470pf ceramic chip capacitor for each of the Internal V_{EE}/V_{CC} pairs. This same combination is used for any V_{CC} or additional V_{CC} package pins with excellent results.

TESTABILITY

Concepts of testing and testability must be considered from the beginning of any circuit design. AMCC encourages: (1) the use of testability techniques in circuit design; (2) the use of testability analysis early in the design process so that testability problems can be corrected by design; (3) the use of fault grading to assess test vector fault coverage; and (4) an understanding of the capabilities of today's advanced test equipment in the development of semi-custom circuits.

STRUCTURED DESIGN

Structured approaches to ensure circuit testability such as LSSD, Scan Path and BILBO are generally driven by an overall system philosophy to testing. While AMCC does not promote one structured technique over another, each of these measures during design can improve circuit testability. AMCC does promote the use of overall structured design procedures, including functional modularity, bus architectures and clear documentation.

TESTABILITY ANALYSIS

All testability measures have one common goal: to enhance controllability and observability of the circuit. It is a grade on the logic design itself. Controllability is a measure of the ease in setting a particular node to a logic level of zero or one, while observability determines the ease of propagating the node's state to one or more primary outputs. After a netlist has been created and logic simulation has verified correct functional performance, testability can be verified by running testability analysis programs such as DTA (DAISY) or COPTR (TEGAS).

FUNCTIONAL SIMULATION

The object of functional testing is to detect a single stuck-at 1 (SA1) or stuck-at-0 (SA0) fault in the circuit if one exists. This ideally requires sufficient vectors to "cover" all possible fault locations. The percent of coverage is the fault grade of the vector set. To this end, one approach is to cycle all inputs and outputs through 1-0 and 0-1 transitions as a first check after initialization. (This should cycle all internal nodes as well.) This 2^n (n = number of inputs) brute force approach is not necessary. Minimum vector test sets and minimum vector test sequences will cover 100% of all observable faults.

Functional simulation vector fault-grading can be performed using the TEGAS simulator. Fault-grading is used to verify that the simulation bit vectors sufficiently exercise nodes within the circuit to assure that the outgoing product matches the customer specification. Insufficient fault coverage as determined in a fault grading run may require the addition of vectors to the set developed to evaluate logical functionality.

AMCC recommends the creation of a sufficient number of vectors to achieve a fault coverage of 90% or higher, and is prepared to perform the fault grading task upon request.

For guidelines in performing functional simulation, refer to Vector Submission Rules and Guidelines in Section 4, Volume II of this design manual.

AT-SPEED SIMULATION

In addition to functional simulation, the customer must perform an at-speed simulation and timing analysis for all critical (i.e., timing-sensitive) paths in the circuit. Refer to the previously referenced document.

AC TESTS SIMULATION

AC path propagation delay tests require simulation vectors to initialize the circuit path to be measured and to support the measurement of the path. One vector set is required per path measurement. A path is defined as a single input to a single output. Refer to Volume II, Section 4, (708 REV A).

DESIGN FOR TESTABILITY

Some specific design suggestions for improved circuit testability are:

- Become familiar with the macro library BEFORE beginning the macro conversion or design.
- Use synchronous rather than asynchronous circuits whenever possible - functional tests are synchronous.
- Partition the design (use structured design techniques) into smaller, testable sections, usually along a functional boundary.
    - Use degating logic to isolate modules for test.
    - Use modular architecture, bus structures.
    - Break up long counters (>8).
- Don't bury states.

- Use transparent latches instead of Flip/Flops where possible and use I/O latches instead of Flip/Flops.
- Use macros, especially F/Flops and latches, with RESET or SET controls where possible to simplify initialization.
- Avoid feedback loops.
  - If unavoidable, provide a means to break up feedback loops during test (degating, enables).
- Avoid redundant logic - minimize! - or add test points to unmask masked faults.
- Avoid derived clocks - they complicate testing.
- Design in test points, especially in sequential logic. Add test points to improve controllability and observability. Perform testability analysis.
- If I/O pins are limited, use demultiplexors to control and multiplexors to observe internal nodes with otherwise poor observability (buried states).
- Any 3-state enable control signal that is internally generated must be externally observable, and should be externally controllable during test.
- Add parity trees for error detection. Or use Scan Path Design to simplify test sequence generation or use Level Sensitive Scan Design to simplify test sequence generation. Keep test generation in mind while designing the circuit.

DESIGN FOR RELIABILITY

Some specific design suggestions for improved circuit reliability are:

- Become familiar with the macro library BEFORE beginning the macro conversion or design.
- Be aware of "glitch" circuits. Do not use potential glitch circuits to drive clock inputs.
- Avoid one-shot pulse generators.

- Avoid gated and derived clocks.

- Avoid race and hazard conditions. (PRINT_ON_CHANGE files can help identify these.) These are generated by having a signal follow two or more paths to a common circuit element (a.k.a. reconvergent fan-out.)

- Avoid feedback loops.
  - If unavoidable, provide a means to break up feedback loops during test (using degating, enables).

- Avoid feedback paths between registers. If present, compute the worst-case set-up and hold times and verify operation. (Feedback from the ECL output macros must be handled with care if used to input to internal latches and Flip/Flops.)

- Add sufficient GROUND for the number of simultaneously switching outputs and distribute among these outputs (similar to distributed ground in a ribbon cable). Add additional extra ground if there are extra I/O pins available.

- Add extra V_{CC} as needed for the number of simultaneously switching outputs.

- Properly derate fan-out on all distortion-sensitive paths and all clock paths. Keep clock path loading balanced.

- Avoid floating nodes on internal 3-state busses or external bidirectional busses.

- Use Johnson (a.k.a. Mobius, Ring or Twisted-tail) counters or separate Flip/Flops to decode terminal counts. The loading on the Q outputs is identical, eliminating the loading skew (not the metal skew), and the outputs are a Gray code - only one output changes state per clock cycle. (Binary counter decoding can cause glitches.)

- Compensate for rising and falling edge loading skews and the reversed TTL input translator rising and falling edge skews by inversion as needed to reduce pulse stretch and pulse shrink phenomena.

The following tables are taken from the Q5000 Series data sheet and define the operating conditions, maximum chip ratings, DC parametrics and TTL load circuits.

RECOMMENDED OPERATING CONDITIONS – COMMERCIAL

PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE})V_{CC} = 0				
10K Mode	−4.94	−5.2	−5.46	V
100K Mode	−4.2	−4.5	−4.8*	V
ECL Input Signal Rise/Fall Time	–	1.5	5.0	ns
TTL Supply Voltage (V_{CC})	4.75	5.0	5.25	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	0 (ambient)		70 (ambient)	°C
Junction Temperature			130	°C

RECOMMENDED OPERATING CONDITIONS – MILITARY

PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE})V_{CC} = 0				
10K Mode	−4.7	−5.2	−5.7	V
100K Mode	−4.5†	−4.5	−4.8*	V
ECL Input Signal Rise/Fall Time	–	1.5	5.0	ns
TTL Supply Voltage (V_{CC})	4.5	5.0	5.5	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	−55 (ambient)		125 (case)	°C
Junction Temperature			150	°C

† −4.2V is possible. Consult AMCC for DC parametrics for $V_{EE} \geq -4.5V$

* −5.7V is possible. Consult AMCC for ECL 100K DC parametrics operating at this voltage.

ABSOLUTE MAXIMUM RATINGS

ECL Supply Voltage V_{EE} (V_{CC} = 0)	−8.0 VDC
ECL Input Voltage (V_{CC} = 0)	GND to V_{EE}
ECL Output Source Current (continuous)	−50 mA DC
TTL Supply Voltage V_{CC} (V_{EE} = 0)	7.0 V
TTL Input Voltage (V_{EE} = 0)	5.5 V
Operating Temperature	−55°C (ambient) to +125°C (case)
Operating Junction Temperature T_j	+150°C
Storage Temperature	−65°C to +150°C

ECL 10K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -5.2V$[1]

	$T_{ambient}$				T_{case}	
	−55°C	0°C	25°C	75°C	125°C	UNIT
$V_{OH\,max}$	V_{CC}–850	V_{CC}–770	V_{CC}–730	V_{CC}–650	V_{CC}–575	mV
$V_{IH\,max}$[5]	V_{CC}–800	V_{CC}–720	V_{CC}–680	V_{CC}–600	V_{CC}–525	mV
$V_{OH\,min}$	V_{CC}–1080	V_{CC}–1000	V_{CC}–980	V_{CC}–920	V_{CC}–850	mV
$V_{IH\,min}$[5]	V_{CC}–1255	V_{CC}–1145	V_{CC}–1105	V_{CC}–1045	V_{CC}–1000	mV
$V_{IL\,max}$[5]	V_{CC}–1510	V_{CC}–1490	V_{CC}–1475	V_{CC}–1450	V_{CC}–1400	mV
$V_{OL\,max}$	V_{CC}–1655	V_{CC}–1625	V_{CC}–1620	V_{CC}–1585	V_{CC}–1545	mV
$V_{OL\,min}$	V_{CC}–1980	V_{CC}–1980	V_{CC}–1980	V_{CC}–1980	V_{CC}–1980	mV
$V_{IL\,min}$[5]	V_{CC}–2000	V_{CC}–2000	V_{CC}–2000	V_{CC}–2000	V_{CC}–2000	mV
I_{in} H max[2]	30	30	30	30	30	µA
I_{in} L min[2]	—.5	—.5	—.5	—.5	—.5	µA

ECL 100K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -4.5V$[3]

SYMBOL	PARAMETER	TEST DC CONDITIONS	COMM 0°/+70°C $V_{EE} = -4.2V$ to $-4.8V$			MIL −55°/+125°C $V_{EE} = -4.5V$ to $-4.8V$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	Output Voltage HIGH	Loading is 50 Ohms to −2V	V_{CC}-1035		V_{CC}-850	V_{CC}-1080		V_{CC}-835	mV
V_{OL}	Output Voltage LOW	Loading is 50 Ohms to −2V	V_{CC}-1830		V_{CC}-1605	V_{CC}-1880		V_{CC}-1595	mV
$V_{IH\,min}$	Input Voltage HIGH	Maximum input voltage HIGH	V_{CC}-1145		V_{CC}-800	V_{CC}-1145		V_{CC}-800	mV
$V_{IL\,max}$	Input Voltage LOW	Maximum input voltage LOW	V_{CC}-1950		V_{CC}-1475	V_{CC}-1950		V_{CC}-1475	mV
I_{INL}[2]	Input Current	$V_{IN} = V_{IL\,min}$	−0.5			−0.5			µA

TTL INPUT/OUTPUT DC CHARACTERISTICS

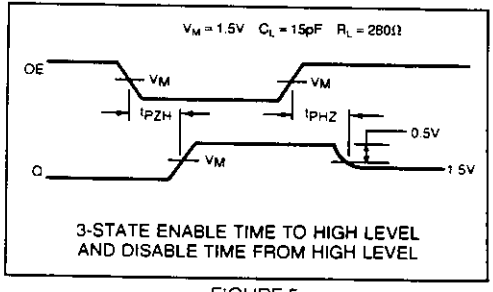
SYMBOL	PARAMETER	TEST DC CONDITIONS	COMM'L 0°/+70°C			MIL 55°/+125°C			UNIT
			MIN	TYP[4]	MAX	MIN	TYP[4]	MAX	
V_{IH}[5]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			2.0			V
V_{IL}[5]	Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = −18mA		−.8	−1.2		−.8	−1.2	V
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = −1mA	2.7	3.4		2.4	3.4		V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 4mA			0.4			0.4	V
		I_{OL} = 20mA			0.5			0.5	V
I_{OZH}	Output "off" current HIGH (3-state)	V_{CC} = Max, V_{OUT} = 2.4V	−50		50	−50		50	µA
I_{OZL}	Output "off" current LOW (3-state)	V_{CC} = Max, V_{OUT} = 0.4V	−50		50	−50		50	µA
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7V			50			50	µA
I_I	Input HIGH current at Max.	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
I_{IL}[6]	Input LOW current	V_{CC} = Max, V_{IN} = 0.5V			−0.4			−0.4	mA
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} = 0.5V	−25		−100	−25		−100	mA

1 Data measured with V_{EE} = −5.2 ± .1V (or V_{CC} = 5.0 ± .1V for +5V ref. ECL 10K) assuming a +50°C rise between ambient (T_a) and junction temperature (T_J) for −55°C, 0°C, +25°C, and +70°C, and a +25°C rise for +125°C. Specifications will vary based upon T_J. See AMCC Packaging and Design Guides concerning V_{OH} and V_{OL} adjustments associated with T_J for packages and operating conditions.
2 Per fan-in.
3 Data measured at thermal equilibrium, with maximum T_J not to exceed recommended limits. See AMCC Packaging Guide to compute T_J for specific package and operating conditions. For +5V ref. ECL 100K, V_{OH} and V_{OL} specifications will vary based upon power supply. See AMCC Design Guide for adjustment factors.
4 Typical limits are at 25°C, V_{CC} = 5.0V.
5a These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
5b Use extreme care in defining input levels for dynamic testing. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using V_{IL} ≤0.4V and V_{IH} ≥2.4V for dynamic TTL testing.
6 For standard speed options only

FIGURE 2

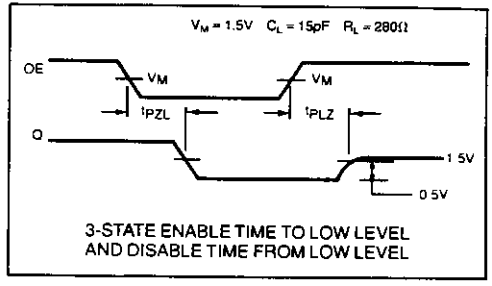
FIGURE 3

FIGURE 4



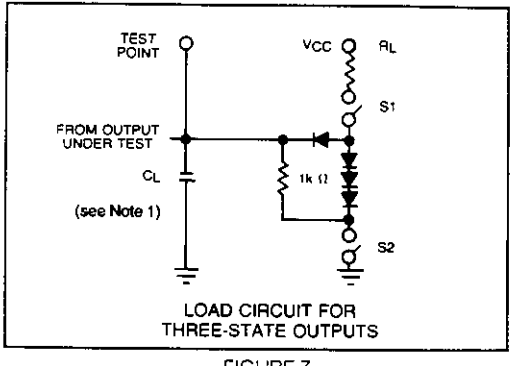
3-STATE ENABLE TIME TO HIGH LEVEL
AND DISABLE TIME FROM HIGH LEVEL

FIGURE 5



3-STATE ENABLE TIME TO LOW LEVEL
AND DISABLE TIME FROM LOW LEVEL

FIGURE 6



LOAD CIRCUIT FOR
THREE-STATE OUTPUTS

FIGURE 7

3-STATE TEST CIRCUIT SWITCH TABLE

TEST FUNCTIONS	S1	S2
tp_{ZH}	Open	Closed
tp_{ZL}	Closed	Open
tp_{HZ}	Closed	Closed
tp_{LZ}	Closed	Closed

NOTES:

1 Standard TTL load circuit used for macro specification, see Figures 2 and 7. CL includes probe, jig and package capacitance.
2 V_{IN} = 0 to 3.0 volts.

Section 3:

Timing Analysis

COMPUTING PROPAGATION DELAY

The macros selected, the options of those macros, the loading on the macros, the use of wire-ORs, and the final layout of the circuit are all factors in the propagation delay of any path. There are two approaches that can be used to compute propagation delay: Front-Annotation, where a statistical estimate of metal delays based on net sizes is used; and Back-Annotation, where the actual metal delay is used in the computation.

• PRELIMINARY COMPUTATION - PRIOR TO CAPTURE

Path propagation delays can be estimated using the statistical wire delay tables, wire-OR load factor and the appropriate k-factors for the macros chosen. The generalized equation for the typical extrinsic (load) delay for a single net is shown below and discussed in detail on the following pages.

$$t_{ex} = k * (L_{fo} + L_{net} + L_{wo})$$

The sum of all typical intrinsic macro delays in the path (t_{in}; specified as Tpd in the macro documentation) and all extrinsic loading (t_{ex}) is then multiplied by the proper ANNOTATED worst-case timing multiplication factor.

Note that the statistically-generated Front-Annotation delays do not account for the differences in rise and fall delays due to metal capacitance. Therefore, set-up, hold or recovery errors may be present at simulation with Back-Annotation delays since Back-Annotation does account for these differences.

- FRONT-ANNOTATION - AFTER CAPTURE (REQUIRED)

After schematic capture, Front-Annotation software is available on the individual workstations to provide the designer with Front-Annotation delay files. In each file, the estimated rising and falling edge delays per net (expressed as NOM, MIN and MAX) are provided. The files are identified as FNTMIL.ews, FNTCOM.ews, FNTNOM.ews and FTNMIN.ews. Either FNTMIL.ews or FNTCOM.ews will be present and represents the maximum worst-case net delays. FNTNOM.ews provides the nominal delays and FNTMIN.ews provides the minimum worst-case delays. The extension "ews" is workstation-dependent.

By incorporating these files into the simulation database, the designer can obtain a statistical estimate of circuit performance. Front-Annotation simulation results are not to be considered to be the specification of circuit performance.

- INTERMEDIATE ANNOTATION - AFTER PLACEMENT (OPTIONAL)

AMCC can provide Intermediate-Annotation files after placement has been completed and approved and before routing is begun. Intermediate-Annotation is a closer approximation to the circuit performance but it is still considered to be an estimate. It uses the macro placements in an algorithm to estimate the net delays. It is not a specification of circuit performance but can allow further identification of problem areas in a time-sensitive circuit. Early identification of problems due to placement is cost-effective since it allows placement changes to be made before the routing process.

Intermediate-Annotation software uses a VAX-based database and is not available on the individual workstations. Intermediate-Annotation delay files are used in simulations in the same manner as the Front-Annotation files. The files are identifed as IBAMIL.ews, IBACOM.ews, IBANOM.ews and IBAMIN.ews.

- BACK-ANNOTATION - AFTER ROUTING (REQUIRED)

The most accurate method of computing a circuit propagation delay requires that the circuit be completed through layout. Back-annotation software adds the actual metal delay, fan-out and wire-OR delays into the path. Back-Annotation accounts for the differences in rise and fall times due to differences in metal load units for the rising and falling edges of metal 1 and metal 2. Back-Annotation must be run and approved prior to the generation of the actual silicon arrays.

The Back-Annotation software uses a VAX-based database and is not available on the individual workstations. The Back-Annotation program provides files which include the ACTUAL metal delays of each net. The Back-Annotation delay files are used in the simulations in the same manner as the Front-Annotation files. The files are identified as BCKMIL.ews, BCKCOM.ews, BCKNOM.ews and BCKMIN.ews.

AMCC guarantees that the silicon will match (will not be slower than) the Back-Annotation results.

• TYPICAL INDIVIDUAL MACRO PROPAGATION DELAY

AMCC macro documentation specifies typical, unloaded macro path propagation delays (Tpd) for each path through a macro. Macro specifications include delays for both rising edges and falling edges. For multiple-input macros, there are delay differences for a path based on the number of other inputs changing state. Three-state macros have specifications for high-Z switching delays T_{PHZ}, T_{PZH}, T_{PZL} and T_{PLZ}.

The actual macro path delay will be a function of:

- unselected inputs along the path (e.g., in a 2:1 mux, the state of an unselected I1 will affect the propagation delay of a selected I0->Y);
- the state of the input data (low data may have different set-up and hold times than high data);
- multiple inputs changing state (when several OR/NOR inputs change simultaneously the delay increases).

AMCC macro specifications, as documented in the Design Guides and Design Manuals for each array series, show the typical propagation delay for a path through a macro, under worst-case conditions.

To account for some of these path delay variations, the AMCC macro specifications have been expanded to show the model behavior in more detail. The specifications are interpreted as follows:

Non-inverting:
- Tpd++ rising edge input to rising edge output
- Tpd-- falling edge input to falling edge output

Inverting:
- Tpd+- rising edge input to falling edge output
- Tpd-+ falling edge input to rising edge output

All AMCC EWS simulation models are accurate to within 10ps.

• INTRINSIC SET-UP AND HOLD TIMES

The intrinsic set-up and hold times for latches, flip/flops, and MSI or multiple-cell macros that include one or more of these types of devices, are specified in the macro summary in Section 6. The parameters represent the behavior of the macro as observed at its input and output nodes. Set-up time (Tsu) is the time that a signal must be stable prior to the active clock edge. Hold time (Th) is the time that a signal must be held after the active clock edge.

• RECOVERY TIME

Recovery time (Trec) is specified for any latch, flop/flop or MSI which has a set or reset. It is the length of time that a reset/set signal has to have been inactive prior to an active clock edge. Clocking within the recovery time period will result in unpredictable behavior.

Set-up time, hold time, recovery time and minimum pulse width are all specified as worst-case minimums as opposed to all other propagation delays which are specified as typical values. Set-up time, hold time, recovery time and minimum pulse width are not multiplied by a worst-case timing multiplier. Macro intrinsic delays and extrinsic delays are multiplied by the worst-case multiplier.

• EFFECT OF LOADING ON OUTPUT MACRO DELAYS

For output macros, Tpd is specified for a specific load limit. For TTL or ECL output loads up to but less than 100pf use Table 3-1. For TTL or ECL output loads over 100pf, consult AMCC.

TABLE 3-1
OUTPUT LOADING DELAYS
TYPICAL

TTL RISING EDGE	.072ns/pf
TTL FALLING EDGE	.072ns/pf
ECL RISING EDGE	.045ns/pf
ECL FALLING EDGE	.037ns/pf

The delay adjustment values for both TTL and ECL output capacitive loading are typical and must be multiplied by the worst-case timing multiplier for the selected operating conditions. Therefore, at this step, the nominal capacitive load delay should be added to the nominal path propagation delay.

• COMPUTING THE LOADING DELAY FOR A NET - FRONT ANNOTATION

The method for manual computation of the effect of load units on the propagation path is:

For each net:

$$t_{ex} = k * (L_{fo} + L_{net} + L_{wo})$$

where

k = the k-factor for the series and the macro type and/or option as listed in Section 6. An overview of k-factors is listed in Table 3-2.

L_{fo} = the sum of the electrical fan-out loads in a net. (Pins with a fan-in of 2 count as 2 electrical loads)

L_{net} = the estimated metal delay from Table 3-3, indexed by the sum of the number of pins in the net minus 1 (i.e., index by [net size - 1]) (Pins with a fan-in of 2 count as 1 physical load)

L_{wo} = W * (n-1) where W is the wire-OR load factor and n is the size of the wire-OR (see Table 3-4)

TABLE 3-2
k FACTORS - Q5000

		ns/LU	
k_{rise}	S-option	0.040	
k_{fall}	S-option	0.040	
k_{rise}	L-option	0.040	
k_{fall}	L-option	0.080	
k_{rise}	H-option	0.020	
k_{fall}	H-option	0.040	
k_{rise}	DRIVER	0.020	(15 loads)
k_{fall}	DRIVER	0.020	(15 loads)
k_{rise}	V-macro	0.020	(9 loads)
k_{fall}	V-macro	0.020	(9 loads)
k_{rise}	DRIVER	0.010	(25 loads)
k_{fall}	DRIVER	0.010	(25 loads)

Refer to Section 6 for the k-factors for a specific macro.

- COMPUTING L_{net}

Compute the statistical metal estimate by counting the physical pin in the net (driving or source pins and destination pins), subtracting one (1), and using this number as the index to the following table. The number listed under a specific array is the estimate for the load units due to metal in the net. This value does not reflect the differences in rise and fall due to the specific ratio of metal 1 and metal 2 in the load. Back-Annotation is the only source of this information.

TABLE 3-3
FRONT-ANNOTATION
STATISTICAL WIRE LOADS

NET -1	Lnet Q1300T	Q3500T	QM1600T	Q5000T
1	1.80	2.39	1.96	3.84
2	2.86	3.80	3.12	6.11
3	3.76	4.99	4.09	8.02
4	4.56	6.05	4.96	9.72
5	5.29	7.03	5.76	11.29
6	5.98	7.94	6.51	12.76
7	6.63	8.80	7.22	14.14
8	7.25	9.63	7.89	15.47
9	7.85	10.42	8.54	16.74
10	8.42	11.18	9.17	17.96
11	8.97	11.92	9.77	19.15
12	9.51	12.63	10.36	20.29
13	10.04	13.33	10.93	21.41
14	10.55	14.01	11.49	22.50
15	11.05	14.67	12.03	23.57
16	11.54	15.32	12.56	24.61
17	12.01	15.95	13.08	25.63
18	12.48	16.57	13.59	26.63
19	12.94	17.19	14.09	27.61
20	13.40	17.79	14.59	28.58
21	13.84	18.38	15.07	29.53
22	14.28	18.96	15.55	30.46
23	14.71	19.53	16.02	31.38
24	15.14	20.10	16.48	32.29
25	15.56	20.65	16.94	33.19
26	15.97	21.20	17.39	34.07
27	16.38	21.75	17.83	34.94
28	16.78	22.28	18.27	35.80
29	17.18	22.81	18.71	36.66
30	17.58	23.34	19.14	37.50

• COMPUTING L_{wo}

The wire-OR load factor is 0.40 for the Q5000 Series resulting in the following values of L_{wo} for the three wire-OR sizes. This represents the electrical load of any wire-ORs present in a net.

TABLE 3-4
WIRE-OR LOADING
(L_{wo})

WIRE-OR SIZE	LU
WIREOR2	0.40
WIREOR3	0.80
WIREOR4	1.20

• COMPUTING L_{fo}

Compute L_{fo} by adding the sum of the electrical loads of all loads driven. Unless marked by an asterisk and so noted, the fan-in on a macro pin is taken as one. If a destination pin has a fan-in of 2, it counts as two electrical loads and as one physical pin. A destination may appear to have two physical loads internal to the macro. In these cases, the macro documentation will clearly identify the fan-in load represented by that pin. Physical fan-out internal to the macro does not affect the physical pin count.

• WORST-CASE TIMING MULTIPLICATION FACTORS

Once the sum of all of the intrinsic and extrinsic propagation delays in a path or path segment is computed and adjusted for any external capacitive loading, then the result must be multiplied to obtain the worst-case delay as follows:

$$Tpd_{|typical} * M.F. = Tpd_{|worst\text{-}case}$$

Multiplication factors are shown in Table 3-5. The worst-case timing or delay multipliers take into account the following:

- Process variations
- Temperature variations
- Voltage variations
- Signal skew

and apply to the intrinsic macro delays (t_{in} = Tpd) and to the extrinsic net and loading delays (t_{ex}).

TABLE 3-5
WORST-CASE TIMING MULTIPLICATION FACTORS
WORST-CASE MULTIPLIERS FOR FRONT- AND BACK-ANNOTATION

		WCM
MINIMUM *	min.	0.70
	typ.	0.78
	max.	0.86
NOMINAL	min.	0.90
	typ.	1.00
	max.	1.10
COMMERCIAL	min.	1.11
	typ.	1.23
	max.	1.35
MILITARY	min.	1.19
	typ.	1.32
	max.	1.45

* Guideline only

TABLE 3-6
APPLICATION RULES FOR THE WORST-CASE TIMING MULTIPLIERS

- Set-up time, hold time, recovery time and minimum pulse width are not multiplied by any worst-case timing multiplier.
- Macro intrinsic delays and extrinsic delays are multiplied by the worst-case timing multipliers.
- Output loading delays are multiplied by the worst-case timing multipliers.
- Multipliers at a given operating condition represent 20% on-chip signal tracking.

SELECTING THE CORRECT WORST-CASE TIMING MULTIPLIER

Commercial worst-case timing multipliers are for circuits operating in the 0°C ambient to 70°C ambient temperature range with a ±5% power supply variation and a junction temperature maintained at ≤130°C. Violation of any of these three parameters requires the use of the Military timing multipliers.

Military worst-case timing multipliers are for circuits operating in the -55°C ambient to +125°C case temperature range with a ±10% power supply variation and a junction temperature maintained at ≤150°C. If any of these parameters are violated, the military timing multipliers no longer apply. Consult AMCC.

MINIMUM PROPAGATION DELAY

AMCC does not specify minimum circuit delays. However, a guideline for minimum propagation delay is 70% of the typical path delay (the annotated worst-case minimum multiplier is 0.70). Where the performance of a circuit would be affected by excessive speed in an array, the minimum performance requirements must be clearly documented in the design submission.

- RESULT

The total of the macro delays, net loading delays as computed with Front-Annotation, added output capacitive load delays, all summed for each path of interest, multiplied by the proper multiplication factor provides the estimated propagation delay for the paths.

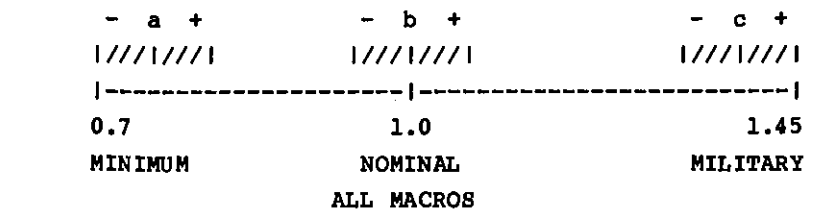
ASYMMETRY IN THE WORST-CASE PATH

Each potentially critical path must be evaluated for worst-case conditions. Both the propagation delay of a rising edge input signal and that of a falling edge input signal must be computed and compared for pulse stretch and pulse shrink. For multiple-input macros, the worst-case specification may be the one with one or more inputs switching or not. The worst potential circuit behavior as represented by the macro specifications must be reviewed.

Minimum pulse-width requirements must be verified and the minimum path delay adjusted as necessary to meet these requirements. Only Back-Annotation is capable of reflecting the rise and fall effects from differences in metal 1 and metal 2.

In some cases the minimum delay may be the worst case. AMCC MacroMatrix releases contain the NOMINAL, MAXIMUM-MILITARY, MAXIMUM-COMMERCIAL and MINIMUM timing libraries for the array series.

FIGURE 3-1
EXAMPLE OF TRACKING FOR THREE OPERATING CONDITIONS:



From the diagram, for unlike structures, 1.1 * c = 1.45 for all macros.

For hold time analysis, see Appendix 3-A.

SIGNAL BALANCING; DISTORTION MINIMIZATION

The case where two paths are required to be identical in performance is common. The best results are obtained when the macros are identical macros and are identically loaded, including wire load. Since placement is not always an option, the judicious use of parallel structures (such as buffer trees) to reduce loading in a path and the use of pulse distortion minimization techniques, such as inversion of the signal at each macro, will help.

For ECL output operation at 100MHz and above, pulse distortion minimization methods should be used. These include: 1) signal inversion on alternating macros; 2) short interconnect, a function of fan-out, wire-ORs and metal length; and 3) balanced rising-edge and falling-edge k-factors.

The final anaylsis for pulse stretch and shrink and balanced path delays must be performed using Back-Annotation.

MAXIMUM OPERATING FREQUENCY

The Q5000 series is capable of supporting high I/O switching rates. The following is a summary of I/O and internal logic performance capabilities. Refer to individual flip/flop, latch and MSI macro specifications for specific information on their performance.

TABLE 3-7a
MAXIMUM OPERATING FREQUENCY
GENERIC MINIMUM PULSE WIDTH

TYPE OF I/O:	OPTION:	< MHz	PW (ns)	
TTL INPUT	S	120	4.16	
	H	160	3.12	
TTL OUTPUT	S	65	7.69	
	H	90	5.55	
	L	30	16.66	
ECL INPUT	S,D	240	2.08	(single-ended)
	S,D	360	1.38	(differential)
COMMERCIAL	V-MACRO	600	0.83	(differential)
MILITARY	V-MACRO	450	1.11	(differential)
ECL OUTPUT	S	180	2.77	(single-ended)
	S	360	1.38	(differential)
COMMERCIAL	V-MACRO	600	0.83	(differential) *
MILITARY	V-MACRO	450	1.11	(differential) *
INTERNAL MACRO	S	210	2.38	
	H,D	360	1.38	
	L	150	3.33	
COMMERCIAL	V-MACRO	600	0.83	(differential) *
MILITARY	V-MACRO	450	1.11	(differential) *

* A V-macro is a differential driver operating with an output range 1/2 of standard.

Selected MSI macros carry their own specifications for maximum operating frequency.

As a reference, the (804) release ECL input macros are listed in Table 3-7b.

TABLE 3-7b
MAXIMUM FREQUENCY FOR ECL INPUT MACROS

IE23D	240	2.08	
IE25	360	1.38	
IE80	240	2.08	
IE85	240	2.08	with IE80
IE85	120	4.16	with IE88D/89D/90
IE86	THERMAL DIODE		
IE88D	180	2.77	
IE89D	180	2.77	
IE90	120	4.16	
IE93	240	2.08	
IE99V	600	0.83	COMMERCIAL
IE99V	450	1.11	MILITARY

FRONT-ANNOTATION LOAD UNITS

The Front-Annotation statistical wire load units table was calculated using the following :

$$LU = a * (netsize-1)^{** b}$$

TABLE 3-8
FRONT-ANNOTATION LOAD UNITS

ARRAYS	b	a	q,wire1	q,wire2
Q5000T	0.67	3.84	1.80	1.80
Q3500T	0.67	2.39	1.80	1.00
Q1300T	0.67	1.80	1.80	1.00
QM1600T	0.67	1.96	1.80	1.00

BACK-ANNOTATION LOAD UNITS

The Back-Annotation delay file is derived using the following:

TABLE 3-9
BACK-ANNOTATION LOAD UNITS

	METAL 1		METAL 2	
	$C_{1rising}$	$C_{1falling}$	$C_{2rising}$	$C_{2falling}$
	LU/mm	LU/mm	LU/mm	LU/mm
Q5000T	1.3	1.8	1.0	1.8
Q3500T	1.0	1.8	0.6	1.0
Q1300T	1.0	1.8	0.6	1.0
QM1600T	1.0	1.8	0.6	1.0

$$LU_{rise} = \frac{(M1 * C_{1rising}) + (M2 * C_{2rising})}{1000}$$

$$LU_{fall} = \frac{(M1 * C_{1falling}) + (M2 * C_{2falling})}{1000}$$

M1 = length of metal 1 in microns
M2 = length of metal 2 in microns

PREVENTING HOLD VIOLATIONS DUE TO CLOCK SKEW

INTRODUCTION

Hold Time violations are a concern wherever 2 storage elements interface with each other, and are clocked by different drivers. Any multiple clock organization or clock distribution tree is subject to this design hazard. The error typically shows up when the Q output of one F/F directly feeds the D input of another.

If the clock to the second F/F is delayed due to tracking or skew, the D input will change during the set-up/hold window. This can easily be avoided by using the guidelines and design checks described below.

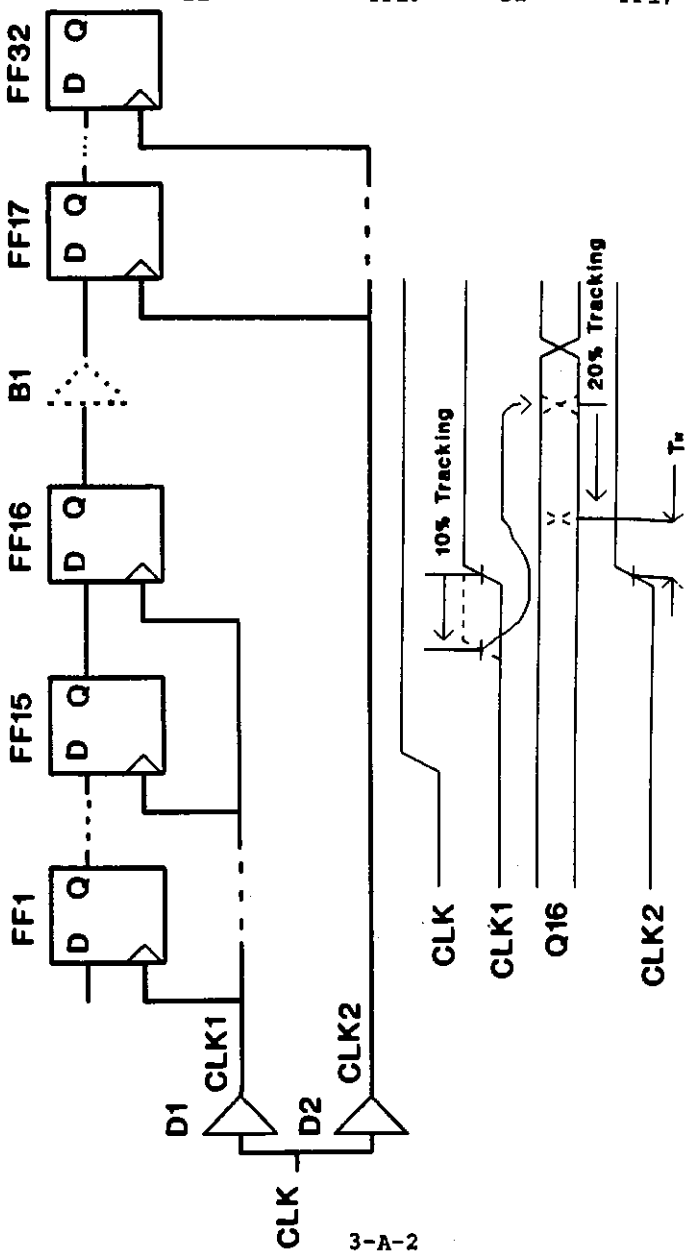
HOLD TIME CONSIDERATIONS

Figure 3-A-1 shows a typical 32-Bit shift register being driven by two clocks. Virtually no considerations are needed to maintain hold time when the Q output and D input are on flip/flops that are driven by the same clock net, i.e., FF15/FF16 driven by CLK1.

If the clocks are different as in FF16/FF17, two paths need to be analyzed to determine if the required hold time has been satisfied. Path 1 flows through macros D1 and FF16 (CLK to Q) to the D input of FF17, while Path 2 is through D2 to the clock input of FF17. Differences in tracking, fan-out and metal lengths between the paths can be significant and cause enough delay in Path 2 to create a hold time error.

FIGURE 3-A-1
32-Bit Shift Register Driven by Two CLocks

$$M * [\ 0.9 * Tpd_{D1} + 0.8 * Tpd_{FF16} - Tpd_{D2}\ ] \geq Th_{FF17}$$



Two options are available to overcome the problem:

1. Add 1 or more gates in Path 1 to offset the delay. Generally, a single gate as shown in Figure 3-A-1 (B1) will suffice.

2. Minimize the differences to an acceptable level through macro selection, placement, load balancing and reduced metal lengths as follows.

   * Use identical clock driver macros to improve tracking.

   * Balance the clock fan-out loading (L_{fo}) to within 10%.

   * Balance the clock loads (fan-out + metal) (L_{fo} + L_{net}) to within 30%.

   * Add a buffer if computation still shows hold time violation

DESIGN CHECK

To compute the hold time of the design, the propagation delay of both paths needs to be determined while factoring in the effects of tracking.

For Like edges:

- If they are placed on adjacent cells on the same row or column, a 5% tracking should be used.

- If the two drivers are of the same macro type and they are placed within the same quadrant, a tracking of 10% should be used.

- If they are not the same macro but are placed within the same quadrant, 20% tracking should be used.

For unlike edges:

- If unlike edges and unlike structures but placed within the same quadrant, 20% tracking should be used.

Other placement options are not recommended.

Note: It is unlikely that two paths whose tracking in relation to each other is of concern, would be placed in different quadrants.

The worst-case tracking direction is to reduce the path propagation delay of both D1 and FF16 by the indicated amount. This includes both the intrinsic and extrinsic delays.

The general equation for the example is as follows:

$$WCMmax * [TRK_1 * Tpd_{D1} + TRK_2 * Tpd_{FF16} - Tpd_{D2}] > Th_{FF17}$$

The TRK_1 tracking factor applies to D1 in the example and is 0.9. This assumes identical driver macros that are placed within the same chip quadrant (10% tracking). For other options, this should be changed to 0.95 (5% tracking) or 0.8 (20% tracking) as applicable.

The TRK_2 tracking factor applies to FF16. In the example, FF16 should use a 20% tracking to account for the unlike edges and unlike structures between FF16 and D2. This assumes that the two macros (D2 and FF16) are both placed within the same chip quadrant.

The computation should be tested at the AMCC minimum test condition (WCMmax = 0.86) if the expression within the brackets results in a positive number. If the result is negative, then the worst-case maximum operating condition needs to be tested (WCMmax = 1.35 for Commercial, or 1.45 for Mil).

For the example, for a MILITARY circuit, the equation becomes:

$$0.86 * [0.9 * Tpd_{D1} + 0.8 * Tpd_{FF16} - Tpd_{D2}] > Th_{FF17}$$

or

$$1.45 * [0.9 * Tpd_{D1} + 0.8 * Tpd_{FF16} - Tpd_{D2}] > Th_{FF17}$$

whichever is worse.

Note: While success can be estimated using Front-Annotation, final calculations must be made after Back-Annotation using the actual metal delays. The layout and/or design must be changed if the appropriate test fails.

Section 4:

External Tsu, Th

EXTERNAL SET-UP and HOLD TIMES

When the input to the data or the clock or both pins on a flip/flop or a latch are supplied from an external signal, then the external set-up and hold times must be computed. The computations must be for worst-case and account for processing skew. Both the rising edge and the falling edge of the data signal must be examined to allow evaluation of signal asymmetry.

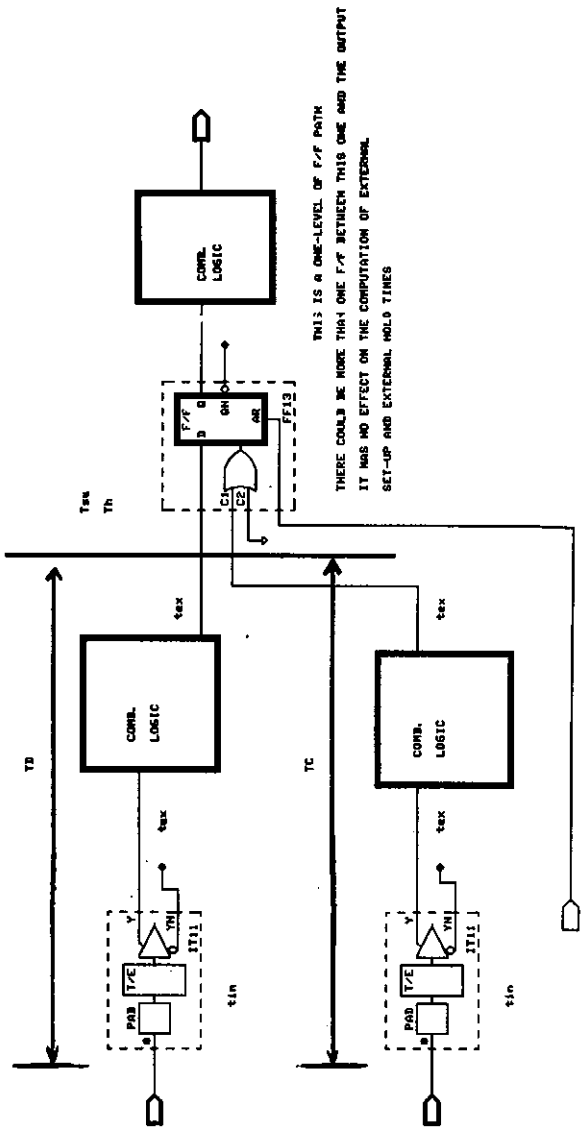
To meet design submission requirements, both the maximum worst-case (1.45 or 1.35) and the minimum worst-case (0.70) equations may need to be computed to determine the worst-case window for external set-up and hold times. Both rising edge input and falling edge input path propagation must be evaluated.

Use the MILITARY or COMMERCIAL equations for set-up time when $t_D - 0.82 * t_C \geq 0$. Use the MINIMUM equations for set-up time when $t_D - 0.82 * t_C < 0$.

Use the MILITARY or COMMERCIAL equations for hold time when $t_C - 0.82 * t_D \geq 0$. Use the MINIMUM equations for hold time when $t_C - 0.82 * t_D < 0$.

Results computed or derived from simulations using Front-Annotation data cannot be considered as the circuit specification.

FIGURE 4-1
EXTERNAL SET-UP AND HOLD FOR ANY CIRCUIT



When computing the set-up time, it is desirable to assume that the data propagation path delay is the worst-case maximum and that the clock path propagation delay is a worst-case minimum for the operating conditions. The generic equation is:

$$t_{su_{external}} = WCMmax * t_D - WCMmin * t_C + Tsu_{macro}$$

When computing the hold time, it is desirable to assume that the data propagation path delay is the worst-case minimum and that the clock path propagation delay is a worst-case maximum for the operating conditions. The generic equation is:

$$t_{h_{external}} = WCMmax * t_C - WCMmin * t_D + Th_{macro}$$

The equations are based on the maximum worst-case 20% variation in on-chip signal tracking discussed earlier in this design manual.

Table 4-1 provides the external set-up and hold equations for the Q5000 and Q3500 Series Bipolar arrays for the four defined operating conditions. Figure 4-1 illustrates the delay path terminology. Table 4-2 provides the definitions for the terms used in the text, the equations and in the figure.

TABLE 4-1
SET-UP AND HOLD EQUATIONS
Q3500, Q5000 SERIES BIPOLAR ARRAYS

MILITARY OPERATING RANGE	t_{su} = 1.45 * t_D - 1.19 * t_C + $T_{su(macro)}$ $t_{h_{external}}$ = 1.45 * t_C - 1.19 * t_D + $T_{h(macro)}$
COMMERCIAL OPERATING RANGE	t_{su} = 1.35 * t_D - 1.11 * t_C + $T_{su(macro)}$ $t_{h_{external}}$ = 1.35 * t_C - 1.11 * t_D + $T_{h(macro)}$
MINIMUM OPERATING RANGE	t_{su} = 0.86 * t_D - 0.70 * t_C + $T_{su(macro)}$ $t_{h_{external}}$ = 0.86 * t_C - 0.70 * t_D + $T_{h(macro)}$

TABLE 4-2
TERMINOLOGY DEFINITIONS

t_D = NOMINAL data path propagation delay from the circuit input and up to the memory macro data input pin computed using Front-Annotation methodology prior to layout; Back-Annotation after layout.

t_C = NOMINAL clock path propagation delay from the circuit input and up to the memory macro clock input pin computed using Front-Annotation methodology prior to layout; Back-Annotation after layout.

Tsu_{macro} = Tsu as specified in Section 6 (specified as minimum)

Th_{macro} = Th as specified in Section 6 (specified as minimum)

WCMxxx: The specific worst-case multipliers (WCMmax and WCMmin) are based on the operating conditions

WCMmax = MILmax, COMmax or MINmax
WCMmin = MILmin, COMmin or MINmin See Table 4-3

Table 4-3 provides a complete summary of the worst-case timing multipliers for the four operating conditions. For each operating condition there is a maximum, a typical and a minimum multiplier. The minimum multiplier is 90% of the typical multiplier. The maximum multiplier is 110% of the typical multiplier. The maximum timing variation possible on a single array is 20%.

TABLE 4-3
WORST-CASE TIMING MULTIPLIERS

ARRAY SERIES: ---> Operating Conditions:		Q3500 Q5000 ambiguity V	abbreviations	
			|	WCMmin
			|	WCMtyp
			V	WCMmax
MINIMUM OPERATING RANGE	minimum	0.70	0.9*typ	MINmin
	typical	0.78	typ	MINnom
	maximum	0.86	1.1*typ	MINmax
NOMINAL OPERATING RANGE	minimum	0.90	0.9*typ	NOMmin
	typical	1.00	typ	NOMnom
	maximum	1.10	1.1*typ	NOMmax
COMMERCIAL OPERATING RANGE	minimum	1.11	0.9*typ	COMmin
	typical	1.23	typ	COMnom
	maximum	1.35	1.1*typ	COMmax
MILITARY OPERATING RANGE	minimum	1.19	0.9*typ	MILmin
	typical	1.32	typ	MILnom
	maximum	1.45	1.1*typ	MILmax

All macros and all delay k-factors are multiplied by these worst-case multipliers. In the bipolar arrays, all macros use the same multipliers for a given operating condition.

Section 5:

Power/Packaging

Table of Contents 5-2

INTRODUCTION

The internal current dissipated by a circuit in a bipolar logic array must be examined to determine if the Maximum Current Specification for the **INTERNAL** array (L cells) has been exceeded. The **TOTAL** current (internal cells and I/O interface cells) is used to compute the worst-case power dissipated by the logic array. The worst-case power as it relates to junction temperature is used to examine the packaging and the heat-sink requirements of the final product.

The total worst-case current is a function of the macros used, the options selected for those macros, the number of unused (terminated) macro output pins that can be powered-down, and the overhead current, which is a function of the array chosen. The current is also a function of the output terminations. I_{EE} is derated based on the actual junction temperature of the device.

V_{OH} derating is as a function of junction and ambient temperature and of power supply voltage.

An unused cell does not dissipate power. An internal or interface macro uses the full current as specified in the Design Guide Macro Summary only if all of its outputs are used, or if unused outputs cannot be powered-down.

MACRO OCCURRENCE TABLE

A macro occurrence table can be constructed prior to design capture to assist in the computation of internal and total circuit current and power dissipation. At the minimum, a macro occurrence table should provide:

- A list of the different macros differentiated by option;
- The number of times (n) each macro appears on the schematics;
- The current (I_{CC} or I_{EE}) for one instance of the macro;
- The total current due to the n occurrences of each macro.
- The sums of the I_{CC} and I_{EE} currents.
- The adjustment for powered-down outputs.

THE WORST-CASE CURRENT MULTIPLIER (WCCM)

For the Q5000 Series, the worst-case current multiplier, WCCM, is the constant 1.4 for MILITARY and 1.4 for COMMERCIAL grade circuits. The worst-case current multiplier is used to compute the worst-case values for all specified macro currents and to compute the worst-case value for the overhead current.

MACRO OPTIONS

Macros for the various AMCC Bipolar Logic Arrays come with options. The Q5000 Series offers the H-option and the L-option (low-power) on nearly all internal macros in its library. The L-option macros are slower than the S-option with a lower fan-out load capability and have a lower dissipated current. The H-option macros are faster than the S-option with a higher dissipated current.

During design, H-option macros, high fan-out drivers (15 and especially 25 load drivers), and other high-current macros should be used judiciously to avoid unnecessary high current/power dissipation. The use of L-option macros can help balance the use of high-current macros providing speed/power programmability.

HIGH-CURRENT INTERNAL MACRO LIMITS

The design guidelines for H-option, drivers, and other high-current internal logic macros vary with the array and are related to the Maximum Internal Current Specification for the array. The design guidelines are shown in Table 5-1. The Q1300T and QM1600T are designed to allow up to 100% high-current internal macros, depending on the macros selected. The Q5000T, because it is 3-layer metal, has no restrictions and can also accommodate 100% high-current macros.

TABLE 5-1
MAXIMUM INTERNAL CURRENT SPECIFICATION
L CELLS ONLY

Array:	Maximum Current mA	Guideline (%H, D macros)	Row Limit mA/row
Q5000T	1383	100%	54
Q3500T	843	50%	39
QM1600T	427	100%	23
Q1300T	405	100%	34

• QM1600T: 160mA TYPICAL for half of the RAM (640 bits)

The maximum current dissipated by the macros that are placed on the internal L cells of an array must be checked against the overall maximum current specification for the array. When a circuit is undergoing placement, the more detailed maximum row current limits are checked.

POWER-DOWN OF UNUSED MACRO OUTPUT PINS

When a macro output pin is terminated, if the output current for that macro pin can be powered-down, the layout software will power-down the output emitter-follower current source, I_{OEF}, thereby reducing the current dissipated by the macro. The amount of the current reduction is a function of the array series and of the macro option as seen in Table 5-2.

With the exception of drivers, this does not apply to any macro output pin that cannot be wire-ORed. Any other pins that cannot be powered-down are noted in the macro documentation in Section 6.

The AMCC MacroMatrix ERC software computes the powered-down current and adjusts the power dissipation table. For 100% TTL or a +5VREF circuit, the powered-down current is considered to be I_{CC} (as is all current in the circuit). For 100% ECL or a TTLMIX circuit, the powered-down current is considered to be I_{EE}.

TABLE 5-2
TYPICAL I_{OEF} in mA FOR POWERED-DOWN OUTPUTS

MACRO	mA	WIRE-ORABLE*
S-OPTION LOGIC MACRO	0.36	YES
H-OPTION LOGIC MACRO	0.36	YES
L-OPTION LOGIC MACRO	0.18	YES
15-LOAD DRIVER - LOGIC	0.72	NO
25-LOAD DRIVER - LOGIC	2.16	NO
V MACRO - LOGIC **	----	NO
S-OPTION I/O MACRO	0.45	YES
H-OPTION I/O MACRO	0.45	YES
L-OPTION I/O MACRO	-	none available
15-LOAD DRIVER - I/O	1.62	NO
25-LOAD DRIVER - I/O	2.79	NO
V MACRO - I/O **	----	NO
3-STATE ENABLE-DRIVER	-	NO

* wire-ORable in the general case
** differential macros, both outputs must be used.

COMPUTING THE MAXIMUM WORST-CASE INTERNAL CURRENT

To compute the internal worst-case current:

- Sum the total typical current dissipated by the internal logic macros (those placed on L cells); set this aside; (total typical internal current);
- Count the number of unused macro outputs by macro option type (S-option, H-option, L-option, or driver; interface or logic);
- Multiply the number of unused outputs of each type by the current saved per output;
- Sum all of these products together and subtract from the total typical internal current;
- Multiply the result by the worst-case current multiplier to find the worst-case maximum current;
- Compare this to the specification for the array;
- If the computed value exceeds the specified limit, adjust the design. Excessive current at this level, when coupled with other placement constraints, could prevent a successful layout.

COMPUTING THE MAXIMUM WORST CASE POWER

- COMPUTE THE TOTAL TYPICAL MACRO CURRENT

To compute the worst-case power for a circuit on an array, all of the macros used must be listed. To estimate power prior to schematic capture, create a macro occurrence table as described earlier and compute the total current dissipated.

- REDUCE CURRENT DUE TO POWERED-DOWN OUTPUTS

Reduce the current for the powered-down macro outputs as previously done when computing the maximum internal current. In this case, compute the amount of current saved by the power-down of both internal and interface macro outputs. As before, this affects the I_{EE} sum unless the circuit has a single +5V power supply, then $I_{EE} = 0$ and the I_{CC} term is the one reduced.

- ADD THE OVERHEAD CURRENT

The overhead current is the base array current dissipated by the internal regulators, reference generators, selected I/O mode (TTL, ECL, MIXED), and power supply configuration (+5V, -5.2V, dual supply or other). The overhead current for the array is specified in the Overhead Current Drain table. (Refer to Table 5-3.)

TABLE 5-3
AMCC BIPOLAR ARRAYS TYPICAL OVERHEAD CURRENT (mA)

CHIP	TTL MODE	ECL MODE	MIXED MODE	+5V REF ECL/TTL
V	I_{CC},mA	I_{EE},mA	I_{EE}/I_{CC},mA	I_{CC},mA
Q5000	193	286	286/11	309 (298/11) *
Q3500	130	170	174/14	193 (179/14)
Q1300	108	131	136/14	157 (143/14)
QM1600	130	170	174/14	193 (179/14)

* numbers in parenthesis are for use in temperature derating

Add the overhead current drain to the appropriate current dissipation sum already computed:

$$\text{SUM OF MACROS } I_{CC} + I_{CC}|_{\text{OVERHEAD}}$$
$$\text{SUM OF MACROS } I_{EE} + I_{EE}|_{\text{OVERHEAD}}$$

- MULTIPLY BY THE WORST-CASE CURRENT MULTIPLIER (WCCM)

Multiply the results by the appropriate worst-case current multiplier to obtain the worst-case I_{CC} and worst-case I_{EE} current. Unless the circuit uses a single-power supply these two sums must be kept separate.

$$(\text{SUM OF MACROS } I_{CC} + \text{OVERHEAD } I_{CC}) * \text{WCCM} = I_{CCwc}$$
$$(\text{SUM OF MACROS } I_{EE} + \text{OVERHEAD } I_{EE}) * \text{WCCM} = I_{EEwc}$$

- MULTIPLY BY THE WORST-CASE VOLTAGE

The worst-case voltage is dependent on whether the circuit is COMMERCIAL or MILITARY. The typical variation is shown in Table 5-4. For COMMERCIAL circuits, the voltage variation is usually ±5%. For MILITARY circuits, the voltage variation is usually ±10%. Note the worst-case voltage for the -4.5V supply as listed in Table 5-4 and on the data sheet.

TABLE 5-4
WORST-CASE VOLTAGE

NOMINAL	COMMERCIAL	MILITARY
+5.0V	+5.25V	+5.5V
-5.2V	-5.46V	-5.72V
-4.5V	-4.8V	-4.8V

Multiply the worst-case current with the appropriate worst-case voltage:

$$I_{EEwc} * V_{EEwc}$$
$$I_{CCwc} * V_{CCwc}$$

- SUM THE RESULT

Sum these together. If there are ECL outputs, compute the ECL static power dissipation and add to the sum. The result is the total worst-case power dissipated by the circuit on the target array.

- ECL STATIC POWER

The equation used by the AMCC MacroMatrix ERC software to compute ECL static power dissipation for ECL outputs is:

XXmA * 1.3V * NUMBER_OF_ECL_OUTPUTS

where XX is the current based on the termination.

The 1.3V term represents the absolute average of the -0.8V to -1.8V (NOM) voltage drop in the output transistor. This is considered to be the statistical worst-case for this function.

- ECL OUTPUT TERMINATION CURRENT

Table 5-5 provides the ECL output termination currents used by the AMCC MacroMatrix ERC software to compute the general case. The currents shown are the average current (average of I_{OH} and I_{OL}) for 50% terminations active.

TABLE 5-5
ECL 10K/100K TERMINATION CURRENT

25ohm	28.0mA
50ohm	14.0mA
100ohm	7.0mA
200ohm	3.5mA

* the average current (average of I_{OH} and I_{OL}) for 50% terminations active

If other ECL output load resistances are used, the actual current value must be computed for use in this equation. The termination current can be computed using the equation:

I = (0.7 * V) / R for any R.

The duty cycle of the outputs will also affect this value.

PACKAGE SELECTION

AMCC offers an assortment of packages for the Q5000 Series Logic Arrays. The maximum external pin counts for these arrays are shown in Table 5-6. AMCC standard packages for each array are presented in Table 5-7. For any special packaging requirements, please consult AMCC.

Package selection requires that the designer have two computations completed: 1) the total maximum worst-case power dissipation; and 2) the total number of array pads required. The array pads required is provided by the AMCC MacroMatrix ERC software Population Check Report and is the sum of all signals, all power (fixed and added) and all ground (fixed or added) pins as indicated on the schematics. The report is labeled as "EXTERNAL PIN COUNT".

The designer also needs the current AMCC Packaging Brochure, which lists the package options for the bipolar arrays as well as the tables providing the θ_{jc} and θ_{ja} and the reductions possible with forced air and heatsinks. AMCC placement instructions are required for the placement of added power and grounds for the Q5000T packages. Placement is pad-restricted and all added power and grounds should attach to internal package planes and not to external package pins.

Compute the junction temperature for the product grade (MILITARY or COMMERCIAL) based on the specified operating environment, i.e., temperature; heat sink, if any; air flow, if any; etc.

TABLE 5-6
ARRAY PAD COUNT LIMIT

ARRAY NAME	REQUIRED POWER-GROUND PADS **	CIRCUIT I/O PAD LIMIT	TOTAL EXTERNAL PADS
Q5000T	24 *	160	184 *
Q3500T	28	120	148
Q1300T	16	76	92
QM1600T	28	106	134

* ARRAY PAD LIMIT
** FIXED POWER-GROUND PADS; ALL MUST BE USED

TABLE 5-7
AMCC STANDARD PACKAGING MATRIX

	Q1300T	QM1600T	Q3500T	Q5000T
64 LDCC 40 mil center	x			
84 LDCC 50 mil center	x			
100 LDCC 25 mil center	x			
100 LDCC 50 mil center	x	x	x	x
132 LDCC 25 mil center		x	x	x
196 LDCC 25 mil center				x
68 PGA cavity down	x			
84 PGA cavity down	x			
100 PGA cavity down	x	x	x	x
148 PGA cavity down			x	x
224 PGA cavity down				x

The QM1600T 148 PGA provides 106 signal and 28 power/ground pins. The Q3500T PGA provides 120 signal pins and 28 power/ground pins. For specific information on the power/ground pins and packaging planes consult AMCC.

AMCC has custom designed certain packages to accommodate high-speed requirements. Special packages such as the 100 LDCC with 25 mil spacing, the 196 LDCC, the 84 PGA and the 224 PGA have been designed to significantly decrease crosstalk, reduce ground bounce and decrease thermal resistance. These packages include:

- Customized cavity and bonding finger layout to match each array and package combination.
- Controlled impedance for minimum ringing and reflection.
- Power pads bonded to a common package power plane to minimize lead resistance and improve shielding effects.
- Minimum inductance on the power and signal pins.
- Ground traces between signal pins.
- Ground planes above and below signal pins for complete isolation.
- Adjacent signals isolated by alternating bonding shelves.
- Optional external bypass capacitors provided.
- Heat spreaders for low thermal resistance.
- Thermal vias for improved thermal conductance.

AMCC prefers that you use only AMCC-standard packages for the Q5000T.

For frequencies above 400 MHz, consult AMCC during package selection for your application. For power dissipation above 12 Watts. consult AMCC.

ECL DC OUTPUT VOLTAGE TRACKING

The data sheet provides ECL VOH and VOL DC parameterics for both ECL 10K and ECL 100K under specific test conditions. Table 5-8 lists the tracking characteristics to estimate the variance in VOH/VOL as an independent function of voltage (V_{EE}) and temperature.

TABLE 5-8
ECL ELECTRICAL CHARACTERISTICS
OUTPUT VOLTAGE TRACKING RATE WITH TEMPERATURE
OUTPUT VOLTAGE TRACKING RATE WITH SUPPLY VOLTAGE

	$\frac{dV_{OH}}{dT}$	$\frac{dV_{OL}}{dT}$	$\frac{dV_{OH}}{dV_{EE}}$*	$\frac{dV_{OL}}{dV_{EE}}$*
units:	mV/°C	mV/°C	mV/V	mV/V
ECL 10K	+1.0	-0.5	+30	+100
ECL 100K	+0.8	-0.5	+30	+100

Loading is 50 ohms to V_{TT} = -2.0V

* For +5V REF ECL, the voltage is V_{CC}.

To estimate values at a target condition from a referenced measured value taken at a specific V_{EE} and temperature, apply the appropriate value from Table 5-8 to the change in V_{EE}, junction temperature, ambient temperature or case temperature. If the temperature or voltage of the target condition is increased over the measured condition, the table values are taken directly. If the new condition is at a lower temperature or voltage, the sign for the appropriate adjustment value in the table should be reversed.

ECL OUTPUT VOLTAGE TRACKING - DATA SHEET CONSIDERATIONS

Estimations are more complex if the data sheet is used as the reference. The temperature conditions on the data sheet assume a specific θ_{ja} or θ_{jc}, while the array being considered may have a different thermal resistance due to package selection, heatsink, forced air, etc.

To estimate VOH_{min}, VOH_{max}, VOL_{min} or VOL_{max} at a specific target temperature, both the data sheet and target temperatures must first be converted into junction temperatures.

Tracking can now be determined the same as above by using the table (TABLE 5-8). The target junction temperature can be computed by calculating or estimating the thermal resistance for the operating environment of the chip.

Note 1 on the data sheet identifies the assumed thermal resistances for ECL 10K, and Note 3 implies maximum junction temperature for ECL 100K (+130°C for COMMERCIAL and +150°C for MILITARY). At high target temperatures, I_{EE} derating as a function of temperature can be factored into the conversion calculations to obtain further accuracy.

WHile the data sheet provides minimum and maximum values, the actual D.C. value for a given process lot or environment will fall somewhere within the range. To estimate actual values at various V_{EE} and temperature conditions, the reference should be a measured value.

I_{EE} DERATING WITH TEMPERATURE

TABLE 5-9
CORE CURRENT VARIATION WITH TEMPERATURE *

$\frac{dI_{EE}}{dT}$ == -0.1%/°C change in T_j

* For $T_j > 0$

The ECL core, overhead and interface macro current I_{EE} is a function of temperature variations. For +5V REF ECL/TTL circuits, it applies to I_{CC} in the core and that current in the ECL macros as well as to the ECL portion of the overhead. Use the parenthisized values from the overhead current table.

Worst-case current occurs at cold temperatures. All computations in the AMCC Design Manual are for the worst-case maximum I_{EE}.

Derating is done from the junction temperature, T_j. ECL parametrics are measured at thermal equilibrium and T_j is assumed to be close to 0°C when T_a = -55°C.

$$I_{EE_{typical\ at\ T_J}} = I_{EE_{typical}} * (1 - (0.001 * T_j))$$

$$I_{EE_{maximum\ at\ T_J}} = I_{EE_{typical}} * WCCM * (1 - (0.001 * T_j))$$

where T_j is the desired junction temperature after airflow, heatsinking and ambient controls are in place. Or, T_j is the actual junction temperature taken from thermal diode measurements.

EXAMPLE COMPUTATION FOR I_{EE}

For a maximum worst-case I_{EE} as computed using the methods in this section of 284mA, a junction temperature of 125 in a Military circuit, the derated maximum I_{EE} would be:

= 284 * (1 - .001*125)

(284 already includes the WCCM = 1.4 multiplier)

= 284 * (.875)

= 249 mA (rounded)

V_{OH}

	SPECIFIED CONDITIONS	ACTUAL JUNCTION TEMPERATURE	ACTUAL AMBIENT TEMPERATURE	
Ambient	25	25	40	°C
Junction	75	50	65	°C
V_{OH}	VCC-a	-1.6(25)	+1.6(15)	V
	θ_{ja} given	θ_{ja} computed	same	

The data sheet calls out (VCC - a), adjust down for the lower junction temperature and then adjust up for the higher ambient temperature.

To adjust for power supply variation, compute the difference (-5.5 vs -5.2), multiply by adjustment constant from the table (0.3 * 0.03).