APNOTE 2.DNIX

(809)

INTRODUCTION

The (708) release includes a new DAISY netlister for use with 5.01 and 5.02 versions of DAISY-DNIX II. Under the new netlister, nested and hierarchical designs are more fully supported.

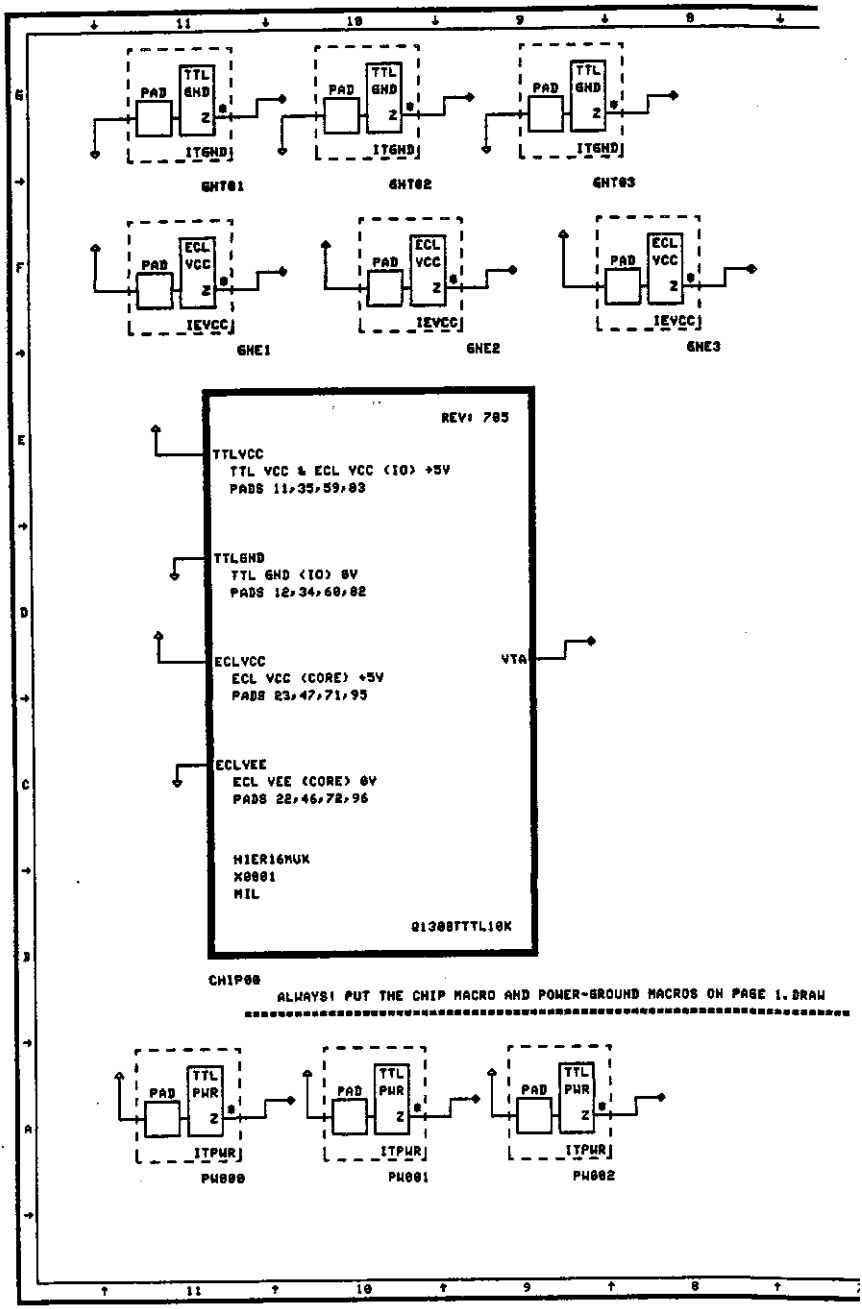
Nested applications are covered in APNOTE 3.DNIX.

The following are the design methodologies that apply to hierarchical designs.

First, DAISY defines such a design to be centered at a top-level directory and to be spread downward in a directory tree. All circuit operations such as DRINK, AGIF, ERCs, Front-Annotation, SIFT, SOM, DLS, etc., are to be performed with the current context set to the top of the design tree.

- Place the chip macro and extra power and ground macros on page 1.DRAW and begin the hierarchy block diagram on page 2.DRAW at the top level.

All extra power and ground macros and the chip macro should be on one page. Extra power and ground macros are named for placement. REGARDLESS OF THE TECHNOLOGY OF THE CHIP, all extra power and ground macro input pins are tied to global ground (NOT VDD) and all extra power and ground macro output pins are tied to a terminator. On DAISY, that is usually /LWTERM. Wire the terminator to the macro pin. Touching pins will sometimes cause a reboot.



PAGE 1.DRAW

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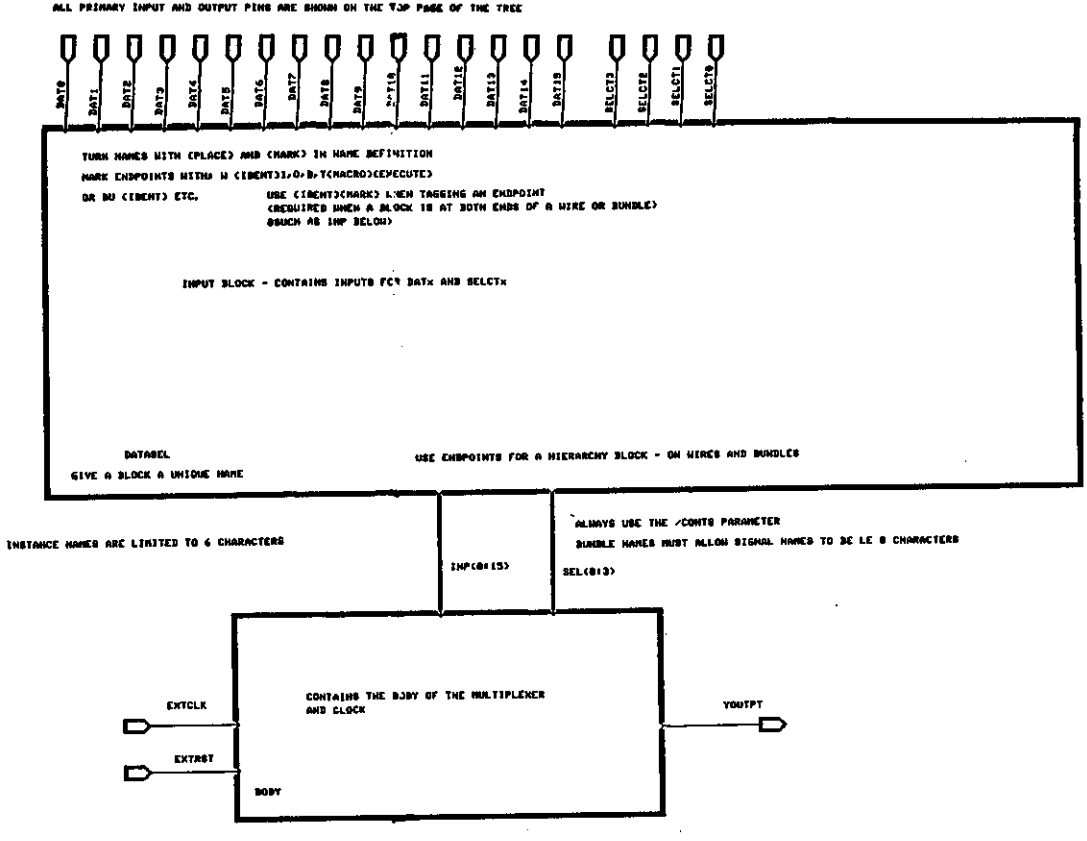
PAGE 2.DRAW


ALL PRIMARY INPUT AND OUTPUT PINS ARE SHOWN ON THE TOP PAGE OF THE TREE
DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
DAT8
DAT9
DAT10
DAT11
DAT12
DAT13
DAT14
DAT15
SELCT3
SELCT2
SELCT1
SELCT0
TURN NAMES WITH (PLACE) AND (MARK) IN NAME DEFINITION
MARK ENDPOINTS WITH: W (IBCNT)3,0,B,Y(MACRO)(EXECUTE)
OR BU (IBCNT) ETC.
USE (IBCNT)(MARK) WHEN TAGGING AN ENDPOINT
(REQUIRED WHEN A BLOCK IS AT BOTH ENDS OF A WIRE OR BUNDLE)
@SUCH AS INP BELOW)
INPUT BLOCK - CONTAINS INPUTS FOR DATx AND SELCTx
DATASEL
GIVE A BLOCK A UNIQUE NAME
USE ENDPOINTS FOR A HIERARCHY BLOCK - ON WIRES AND BUNDLES
INSTANCE NAMES ARE LIMITED TO 6 CHARACTERS
INP(0:15)
ALWAYS USE THE /CONTG PARAMETER
BUNDLE NAMES MUST ALLOW SIGNAL NAMES TO BE LE 8 CHARACTERS
SEL(0:3)
EXTCLK
EXTRST
CONTAINS THE BODY OF THE MULTIPLEXER
AND CLOCK
BODY
YOUTPT

- Create the blocks top down so the system will create the directory for each as it goes.

As a block is created on the drawing page, the system creates a directory for it. If you copy hierarchy pages, you must create the directory for the system or it will become confused. If you rename a block, the system renames the directory at the same time. Try to plan your names in advance and minimize the interference with the system's book-keeping.

- The top sheet or all sheets at the top directory level show all primary inputs and outputs.

Although the input and output macros themselves are probably not on that sheet, all primary inputs and outputs must be placed on a top directory level drawing page. A block diagram may run to more than one page. The primary I/Os must be on one of those pages.

- Use wires and bundles between blocks

There is no restriction on the use of bundles and wires. AMCC prefers that you be consistent across a boundary, i.e., if you leave a block as a bundle and enter the next as a bundle, that the definition pages for those blocks also show bundles.

- If a block is defined as a page which references an additional level of blocks, that is still hierarchy. In DAISY, if the blocks referenced are not unique (are the same), that is nested. DAISY also has a cell - an on-page nested block. Refer the APNOTE 3.DNIX for nested rules.

- Name wires.

Always name wires according to the AMCC EWS Schematic Rules, Volume II, Section 3. All wires crossing a block boundary are named.

- Place a contents parameter on the bundles, not a name.

```
PARA {SELECT}/CONTS{EXTRACT}value
                    {DEF}{PLACE}...{EXECUTE}
```

You may name bundles. AMCC software uses the /CONTS parameter definition.

ALways use the /CONTS parameter for bundles. Bundle nets do not have to be given /CONTS parameters when they are branches from the main bundle on the page. If they are, use the "local" and not the "global" parameter.

Wires feeding into/out of bundles are named with the contents parameter name and the appropriate digits. For example, a bundle with a /CONTS parameter of DTD(0:12) would have signals such as DTD0 and DTD12.

- Place endpoints on wires and bundles:

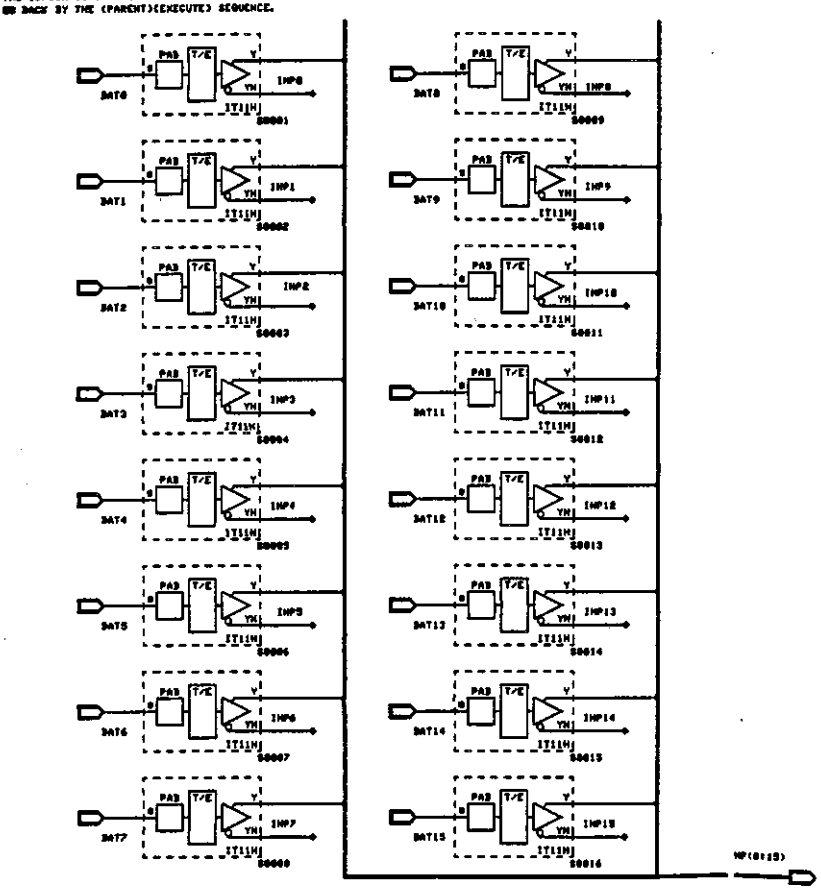
  W {IDENT}x{MACRO}[{MARK}]{EXECUTE} where x = I|O|T|B

  for input, output, tristate, or bidirectional.

  {MARK} is used to position the endpoint and is required when a bus runs between two blocks. The endpoints tend to dissappear when notes are added. Use the {REDRAW} key to get them back.

  - Place both endpoints on by:

    W {IDENT}I{MACRO}O{MACRO}{EXECUTE}



INPUTS

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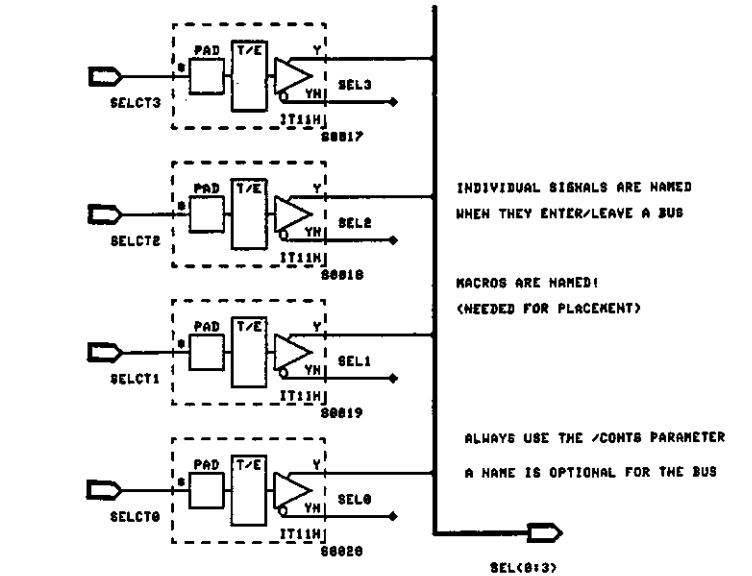
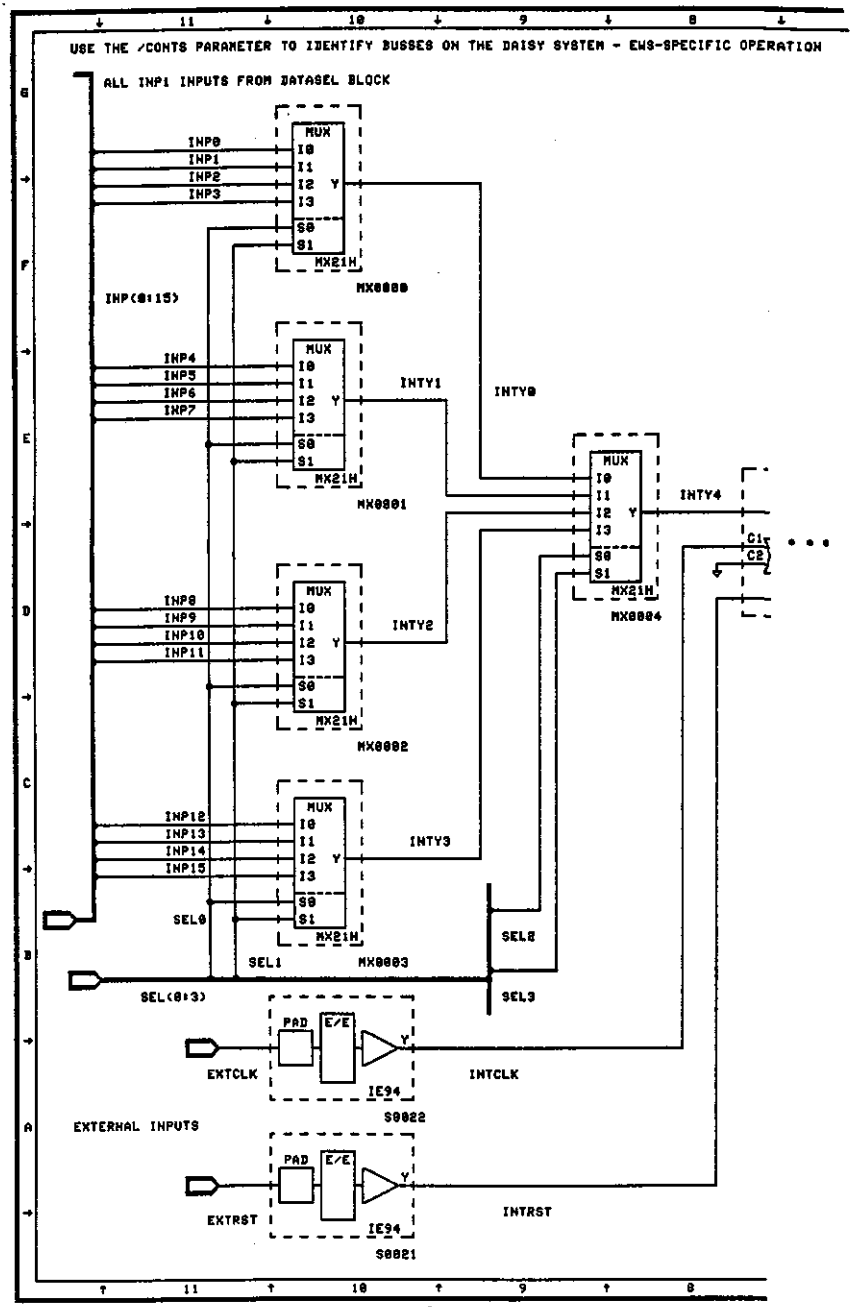


INPUTS CONTINUED



BODY

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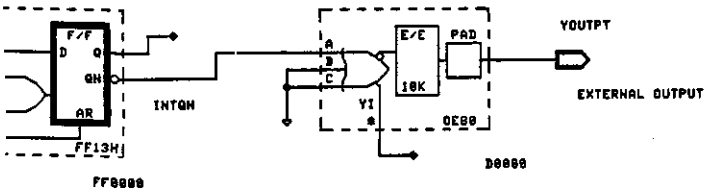


ALL I/O TO/FROM A BLOCK (SIGNALS CROSSING BLOCK BOUNDARIES)
ARE CONNECTED TO HIERARCHY CONNECTORS

USE /RWHICON/ /RWHOCON/ /RBHICON/ RBHOCON/ ETC.

BODY CONTINUED

- Endpoints dissappear when a pin attribute table is deleted. Pin attribute tables are not used for hierarchy blocks; Pin attribute tables are mandatory for nested blocks. Refer to APNOTE 3.DNIX.

- When on the top level, place a cursor on the block whose directory you wish to go to. Use the {CHNGE} key or type CHANGE THEN {SELECT}{EXECUTE}. The system moves down the hierarchy to the lower directory, page 1.draw.

  {CHANGE}{SELECT}{EXECUTE}

- To go back up, use

  {PARENT}{EXECUTE}

Moving up and down the design tree is via the change key and the select key or via the parent key. Moving around within the tree level, as in multiple page definitions, is done via the next and previous keys. The system will prompt for saving a page if it was edited. Always execute a SAVE command once every 10-20 minutes, or at the end of a difficult edit step, if that step took less than 10 minutes. Protect yourself.

Always save to floppy and to a hard disk at the end of a session.

- Name macros if the design is not nested (if a block is not called more than once in a design).

If the hierarchy structure is deep (more than two levels), the user defined name and the block reference may be too long in which case the AMCC netlister will rename the macro (or signal). Refer to AMCCXREF.LST in the /ERC subdirectory. ALL MACROS MUST BE NAMED. ALL BLOCKS MUST BE NAMED.

```
/* Daisy design pathname:  /USER/CLASS/MUXHIER  */
$CONTROL
MODE ADD
SECTION DELAY:N:6
$DELAY
/*                                    R I S E          F A L L      */
/*                                  Typ  Min  Max   Typ  Min  Max   */
@MUXHIER 2:INPØ          =        23    21    25    39    35    42 ;
@MUXHIER 2:INP1          =        23    21    25    39    35    42 ;
@MUXHIER 2:INP1Ø         =        23    21    25    39    35    42 ;
@MUXHIER 2:INP11         =        23    21    25    39    35    42 ;
@MUXHIER 2:INP12         =        23    21    25    39    35    42 ;
@MUXHIER 2:INP13         =        23    21    25    39    35    42 ;
@MUXHIER 2:INP14         =        23    21    25    39    35    42 ;
@MUXHIER 2:INP15         =        23    21    25    39    35    42 ;
@MUXHIER 2:INP2          =        23    21    25    39    35    42 ;
@MUXHIER 2:INP3          =        23    21    25    39    35    42 ;
@MUXHIER 2:INP4          =        23    21    25    39    35    42 ;
@MUXHIER 2:INP5          =        23    21    25    39    35    42 ;
@MUXHIER 2:INP6          =        23    21    25    39    35    42 ;
@MUXHIER 2:INP7          =        23    21    25    39    35    42 ;
@MUXHIER 2:INP8          =        23    21    25    39    35    42 ;
@MUXHIER 2:INP9          =        23    21    25    39    35    42 ;
@MUXHIER/BODY 1:INTCLK           =     23    21    25    39    35    42 ;
@MUXHIER/BODY 1:INTQN            =     23    21    25    39    35    42 ;
@MUXHIER/BODY 1:INTRST           =     23    21    25    39    35    42 ;
@MUXHIER/BODY 1:INTYØ            =     23    21    25    39    35    42 ;
@MUXHIER/BODY 1:INTY1            =     23    21    25    39    35    42 ;
@MUXHIER/BODY 1:INTY2            =     23    21    25    39    35    42 ;
@MUXHIER/BODY 1:INTY3            =     23    21    25    39    35    42 ;
@MUXHIER/BODY 1:INTY4            =     23    21    25    39    35    42 ;
@MUXHIER 2:SELØ          =        7Ø    63    77   117   1Ø6   129 ;
@MUXHIER 2:SEL1          =        7Ø    63    77   117   1Ø6   129 ;
@MUXHIER 2:SEL2          =        23    21    25    39    35    42 ;
@MUXHIER 2:SEL3          =        23    21    25    39    35    42 ;
$END
```

FNTMIL.DSY FILE

```
/****
*
* DESIGN PATH /USER/CLASS/MUXHIER   DATE 3Ø MAR 1986 11:59
*
* COMPANY _______________   CIRCUIT_NAME _____________
*
* ARRAY _________   PO# _____________   REV ______
*
* DESIGNER ____________________________
*
* What tests does this control file support: _________
*
* ____________________________________________________
*
* ____________________________________________________
*
****/

/***   Configuration section    ****/

$CONFIGURATION
GATE_ACTIVITY_LEVEL := 1ØØ;
IMMEDIATE_ACTIVITY_LEVEL := 1ØØ;
TIMING_CHECK := 1;

/***  Signal generator section  ****/

$SIGNAL_GENERATORS
@MUXHIER/DATASEL/1:DATØ := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT1 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT1Ø := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT11 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT12 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT13 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT14 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT15 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT2 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT3 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT4 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT5 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT6 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT7 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT8 := ØØ:FØ ;
@MUXHIER/DATASEL/1:DAT9 := ØØ:FØ ;
@MUXHIER/BODY/1:EXTCLK := ØØ:FØ ;
@MUXHIER/BODY/1:EXTRST := ØØ:FØ ;
@MUXHIER/DATASEL/1:SELCTØ := ØØ:FØ ;
@MUXHIER/DATASEL/1:SELCT1 := ØØ:FØ ;
@MUXHIER/DATASEL/1:SELCT2 := ØØ:FØ ;
@MUXHIER/DATASEL/1:SELCT3 := ØØ:FØ ;
```

UNEDITED SOM_MCF.SING FILE

APNOTE 3.DNIX

(809)

INTRODUCTION

The (708) release includes a new DAISY netlister for use with 5.01 and 5.02 versions of DAISY-DNIX II. Under the new netlister, nested and hierarchical designs are more fully supported.

If a block is defined as a page which references an additional level of blocks, that is still hierarchy. In DAISY, if the blocks referenced are not unique (are the same), that is nested. Design structures may be combinations of these.

Cells are an on-page nest (where a block definition does not require an entire schematic page).

Non-nested hierarchy applications are covered in APNOTE 2.DNIX.

The new AMCC AGIF netlister handles a deeply structured drawing. It can handle a top-level hierarchy block calling a nested block or blocks which in turn call other hierarchy structures.

The following are the design methodologies that apply to DAISY nested hierarchical designs.

First, DAISY defines such a design to be centered at a top-level directory and to be spread downward in a directory tree. All circuit operations such as DRINK, AGIF, ERCs, Front-Annotation, SIFT, SOM, DLS, etc., are to be performed with the current context set to the top of the design tree.

- Place the chip macro and extra power and ground macros on page 1.DRAW and begin the hierarchy block diagram on page 2.DRAW at the top level.

All extra power and ground macros and the chip macro should be on one page. Extra power and ground macros are named for placement. REGARDLESS OF THE TECHNOLOGY OF THE CHIP, all extra power and ground macro input pins are tied to global ground (NOT VDD) and all extra power and ground macro output pins are tied to a terminator. On DAISY, that is usually /LWTERM. Wire the terminator to the macro pin. Touching pins will sometimes cause a reboot.

- Create the blocks top down so the system will create the directory for each as it goes.

As a block is created on the drawing page (the box drawn and given a unique instance name), the system creates a directory for it. If you copy hierarchy pages, you must create the directory for the system or it will become confused. If you rename a block, the system renames the directory at the same time. Try to plan your names in advance and minimize the interference with the system's book-keeping.

- Cells are on-page nesteds, can be off-page nesteds and use the CELL command. Put the cell name inside of the cell.

- Nested pages (definition thereof) can not be at the top level. They require their own individual directory.

Create a directory that is one down from the tree top and name it the same as the LREF parameter you will use to reference it. This makes it easier to find and use by a reviewer. The pathname to this directory is what goes into the /AMCC/CONFIG/NESTED file. A nested block may require more than one definition page.

- For nested blocks, they must have:
  instance name (6 character limit)
  /CTL parameter defined as N
  /LREF parameter with the name the system will use to find the nested page
  pins must be named by the PIN attribute command

The AGIF netlister does recognize and use the /LREF parameter. Make the instance name of the block unique. Use the /LREF parameter to link the structure. Place the /LREF parameter and the path location for the block/cell definition in the /AMCC/CONFIG/NESTED file.

- The top sheet or all sheets at the top directory level show all primary inputs and outputs.

Although the input and output macros themselves are probably not on that sheet, all primary inputs and outputs must be placed on a top directory level drawing page. A block diagram may run to more than one page. The primary I/Os must be on one of those pages.

- Use wires and bundles between blocks

There is no restriction on the use of bundles and wires. AMCC prefers that you be consistent across a boundary, i.e., if you leave a block as a bundle and enter the next as a bundle, that the definition pages for those blocks also show bundles.

- Name wires.

Always name wires according to the AMCC EWS Schematic Rules, Volume II, Section 3. All wires crossing a block boundary are named.

- Name bundles when they are inside a nested block definition.

Bundles may be named at any time but they MUST be named when inside a nested block definition.

- Place a contents parameter on the bundles, not a name.

  PARA {SELECT}/CONTS{EXTRACT}value
  {DEF}{PLACE}...{EXECUTE}

  You may name bundles. AMCC software uses the /CONTS parameter definition.

ALways use the /CONTS parameter for bundles. Bundle nets do not have to be given /CONTS parameters when they are branches from the main bundle on the page. If they are, use the "local" and not the "global" parameter.

Wires feeding into/out of bundles are named with the contents parameter name and the appropriate digits. For example, a bundle with a /CONTS parameter of DTD(0:12) would have signals such as DTD0 and DTD12.

- Place endpoints on wires and bundles going into or out of non-nested blocks.

  W {IDENT}x{MACRO}[{MARK}]{EXECUTE}

  where x = I|O|T|B

  for input, output, tristate, or bidirectional.

  {MARK} is used to position the endpoint and is required when a bus runs between two blocks. The endpoints tend to dissappear when notes are added. Use the {REDRAW} key to get them back.

  - Place both endpoints on by:

    W {IDENT}I{MACRO}O{MACRO}{EXECUTE}

- Endpoints dissappear when a pin attribute table is deleted.

Pin attribute tables are not used for hierarchy blocks; Pin attribute tables are mandatory for nested blocks. Endpoints are required for non-nested blocks.

- When on the top level, place a cursor on the block whose directory you wish to go to. Use the {CHNGE} key or type CHANGE THEN {SELECT}{EXECUTE}. The system moves down the hierarchy to the lower directory, page 1.draw.

  {CHANGE}{SELECT}{EXECUTE}

- To go back up, use

  {PARENT}{EXECUTE}

Moving up and down the design tree is via the change key and the select key or via the parent key. Moving around within the tree level, as in multiple page definitions, is done via the next and previous keys. The system will prompt for saving a page if it was edited. Always execute a SAVE command once every 10-20 minutes, or at the end of a difficult edit step, if that step took less than 10 minutes. Protect yourself.

Always save to floppy and to a hard disk at the end of a session.

- Name macros.

If the hierarchy structure is deep (more than two levels) or is nested, the user defined name and the block reference may be too long in which case the AMCC netlister will rename the macro (or signal). Refer to AMCCXREF.LST in the /ERC subdirectory. ALL MACROS MUST BE NAMED. ALL BLOCKS MUST BE NAMED.

- Identify pins by the PIN command when blocks are nested. For DED2, refer to its manual for the equivalent operation.

PIN {PLACE}
    at this point the block and the pin definition block will flash.
    - the word "name" will be flashing
name{DEF}
    type in the pin name and hit the define key
number{DEF}
    physical identification, default is one
BU{DEF} or just {CONF}
    type of connection, wire is default
OUTPUT{DEF} or INPUT{DEF} or BIDIRECTIONAL{DEF}
    the attribute default is INPUT.
n{DEF}
    n is the width, default is one.

- A pin name must match with the definition page(s) name
  - if the pin is a bundle then a bundle connector must be on the lower level page
  - the pin name at the upper level; the bundle name (if used), the contents parameter, and the individual signal names on the lower page should all match in a nested definition.

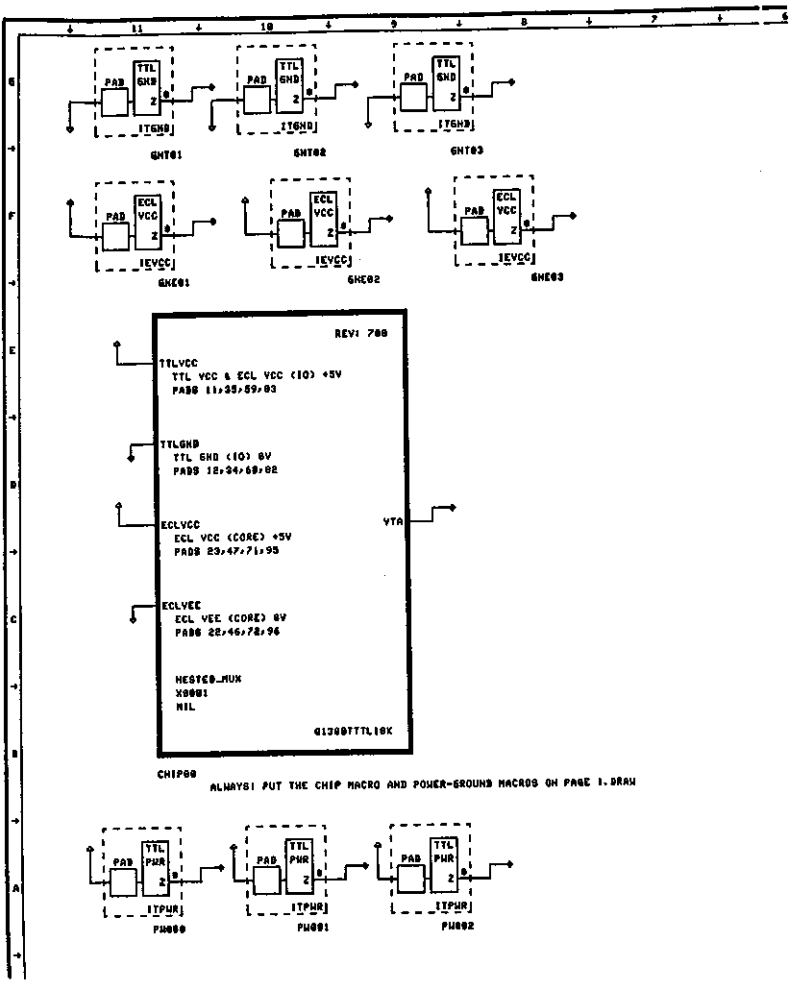
- View a pin definition by PIN {SELECT}
- Confirm an item's definition by {CONF}
- exit a pin edit by {EXECUTE}
- Edit the /AMCC/CONFIG/NESTED file
  LREF_name path_name

path_name is the path where the definition page can be found.

LREF_name is the value you assigned to LREF for each block that will reference the same DEFINITION. The definition can be a page or several pages. It must be uniquely identifiable in the nested file.

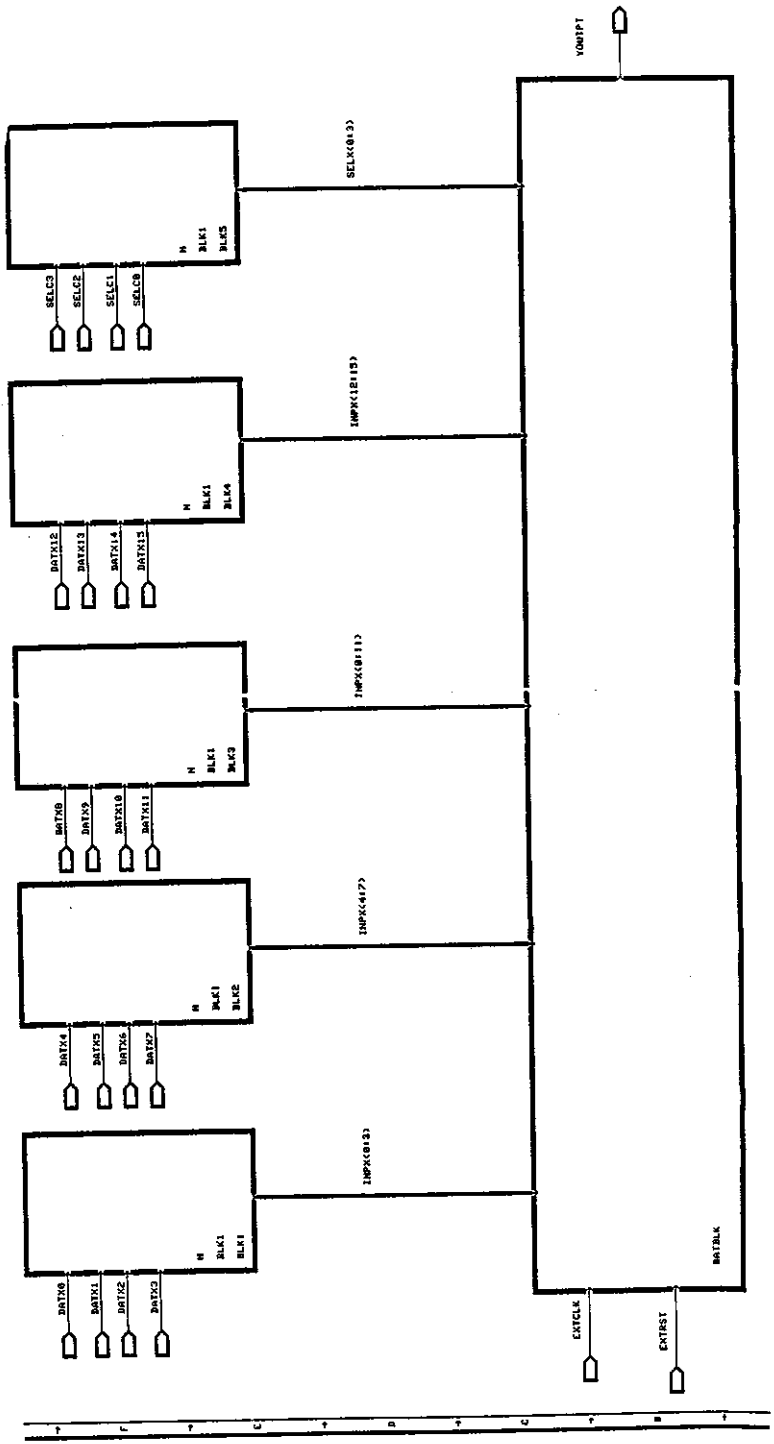
If you are using RAM or other predefined nested macros, copy over the library nested file first, such as: /AMCC/Q3500_LIBS/Q3500_RAM.NEST. Copy this file into the /AMCC/CONFIG/NESTED file before adding your structures. Be sure to save the edited file and to submit it on the floppy(s) sent for design submission. The /AMCC/CONFIG/NESTED file will not be changed when you log on or off.

```
Date:  14 SEP 88 14:37   File:  /AMCC/Q5000_LIBS/Q5000_RAM.NEST

$FORMAT_CARD$
16A 60C
$END$

RAM10  $(NETPATH)/Q5000_LIBS/NESTED/MM10
RAM10H $(NETPATH)/Q5000_LIBS/NESTED/MM10H
RAM20  $(NETPATH)/Q5000_LIBS/NESTED/MM20
RAM20H $(NETPATH)/Q5000_LIBS/NESTED/MM20H
```



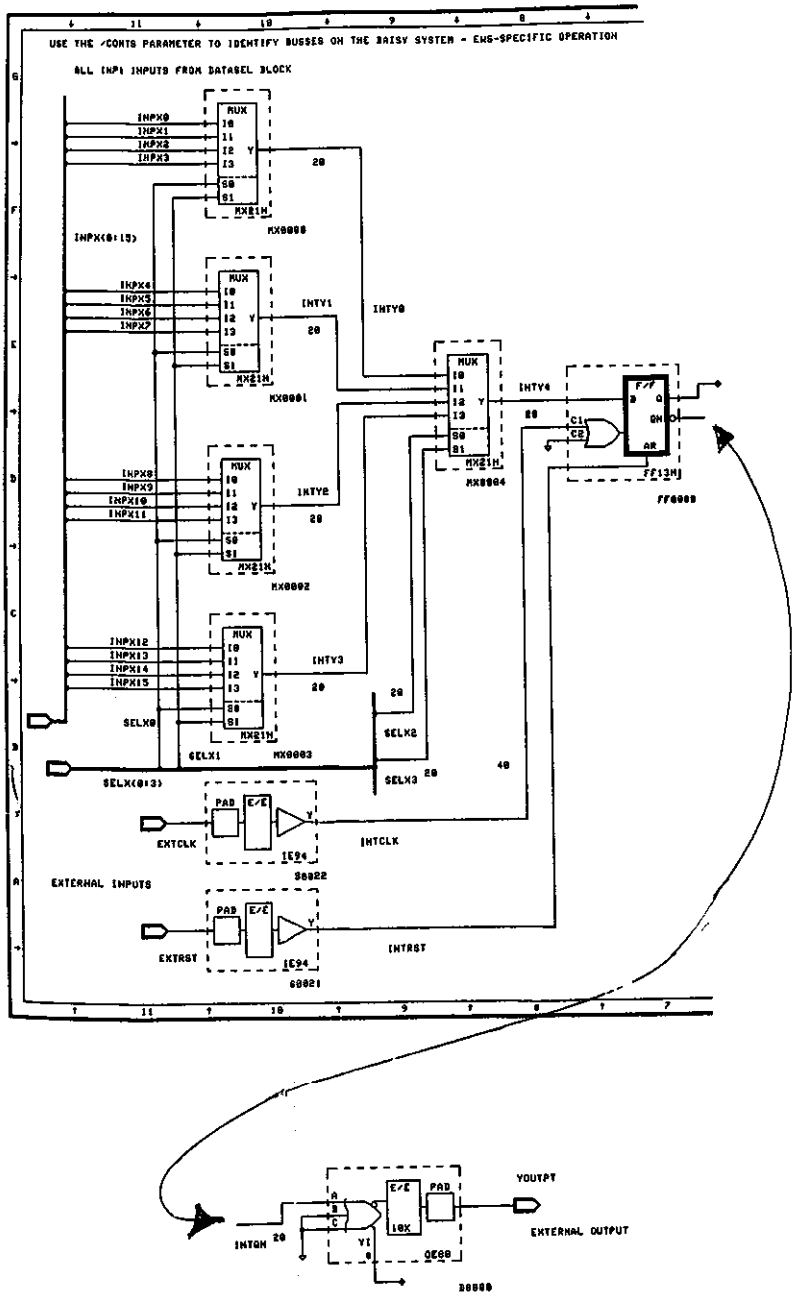
PAGE 1.DRAW

APPNOTE 3.DNIX9



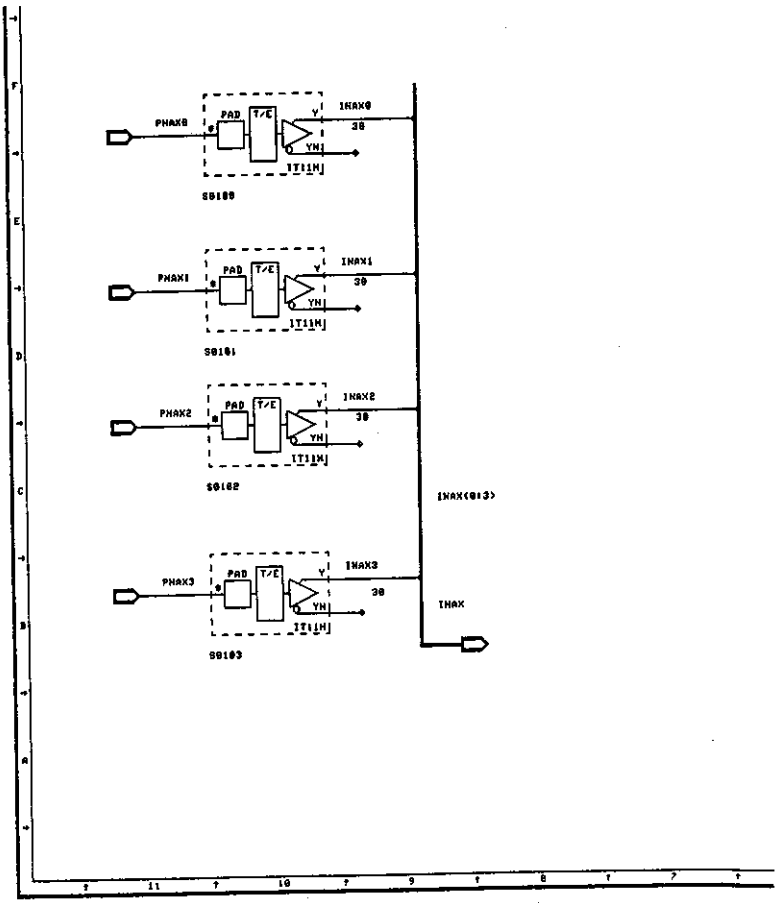
PAGE 2.DRAW

APPNOTE 3.DNIX10



DATBLK PAGE

APPNOTE 3.DNIX11



NESTED BLOCK DEFINITION

APPNOTE 3.DNIX12

FNTMIL.DSY

```
Date:  03 JUN 86 13:26   File:  FNTMIL.DSY

/* Daisy design pathname:  /USER/CLASS/NESTED1  */
$CONTROL
MODE ADD
SECTION DELAY:N:6
$DELAY
/*                                    R I S E        F A L L      */
/*                                  Typ  Min  Max   Typ  Min  Max  */
@NESTED1 2:INPX0          =    23     21   25     39     35    42 ;
@NESTED1 2:INPX1          =    23     21   25     39     35    42 ;
@NESTED1 2:INPX10         =    23     21   25     39     35    42 ;
@NESTED1 2:INPX11         =    23     21   25     39     35    42 ;
@NESTED1 2:INPX12         =    23     21   25     39     35    42 ;
@NESTED1 2:INPX13         =    23     21   25     39     35    42 ;
@NESTED1 2:INPX14         =    23     21   25     39     35    42 ;
@NESTED1 2:INPX15         =    23     21   25     39     35    42 ;
@NESTED1 2:INPX2          =    23     21   25     39     35    42 ;
@NESTED1 2:INPX3          =    23     21   25     39     35    42 ;
@NESTED1 2:INPX4          =    23     21   25     39     35    42 ;
@NESTED1 2:INPX5          =    23     21   25     39     35    42 ;
@NESTED1 2:INPX6          =    23     21   25     39     35    42 ;
@NESTED1 2:INPX7          =    23     21   25     39     35    42 ;
@NESTED1 2:INPX8          =    23     21   25     39     35    42 ;
@NESTED1 2:INPX9          =    23     21   25     39     35    42 ;
@NESTED1/DATBLK 1:INTCLK        =     23     21     25     39     35     42 ;
@NESTED1/DATBLK 1:INTQN         =     23     21     25     39     35     42 ;
@NESTED1/DATBLK 1:INTRST        =     23     21     25     39     35     42 ;
@NESTED1/DATBLK 1:INTY0         =     23     21     25     39     35     42 ;
@NESTED1/DATBLK 1:INTY1         =     23     21     25     39     35     42 ;
@NESTED1/DATBLK 1:INTY2         =     23     21     25     39     35     42 ;
@NESTED1/DATBLK 1:INTY3         =     23     21     25     39     35     42 ;
@NESTED1/DATBLK 1:INTY4         =     23     21     25     39     35     42 ;
@NESTED1 2:SELX0          =    70     63   77    117    106   129 ;
@NESTED1 2:SELX1          =    70     63   77    117    106   129 ;
@NESTED1 2:SELX2          =    23     21   25     39     35    42 ;
@NESTED1 2:SELX3          =    23     21   25     39     35    42 ;
$END
```

```
Date:  Ø3 JUN 86 13:32   File:  SOM_MCF.SING

/****
*
* DESIGN PATH /USER/CLASS/NESTED1   DATE 29-MAY-1986 13:17
*
* COMPANY _____          CIRCUIT_NAME _____
*
* ARRAY   _____     PO#  _____     REV  _____
*
* DESIGNER _____
*
* What tests does this control file support:  _____
*
* _____
*
* _____
*
****/

/***   Configuration section    ****/

$CONFIGURATION
GATE_ACTIVITY_LEVEL := 1ØØ;
IMMEDIATE_ACTIVITY_LEVEL := 1ØØ;
TIMING_CHECK := 1;

/***  Signal generator section  ****/

$SIGNAL_GENERATORS
@NESTED1/2:DATXØ := ØØ:FØ ;
@NESTED1/2:DATX1 := ØØ:FØ ;
@NESTED1/2:DATX1Ø := ØØ:FØ ;
@NESTED1/2:DATX11 := ØØ:FØ ;
@NESTED1/2:DATX12 := ØØ:FØ ;
@NESTED1/2:DATX13 := ØØ:FØ ;
@NESTED1/2:DATX14 := ØØ:FØ ;
@NESTED1/2:DATX15 := ØØ:FØ ;
@NESTED1/2:DATX2 := ØØ:FØ ;
@NESTED1/2:DATX3 := ØØ:FØ ;
@NESTED1/2:DATX4 := ØØ:FØ ;
@NESTED1/2:DATX5 := ØØ:FØ ;
@NESTED1/2:DATX6 := ØØ:FØ ;
@NESTED1/2:DATX7 := ØØ:FØ ;
@NESTED1/2:DATX8 := ØØ:FØ ;
@NESTED1/2:DATX9 := ØØ:FØ ;
@NESTED1/DATBLK/1:EXTCLK := ØØ:FØ ;
@NESTED1/DATBLK/1:EXTRST := ØØ:FØ ;
@NESTED1/2:SELCØ := ØØ:FØ ;
@NESTED1/2:SELC1 := ØØ:FØ ;
@NESTED1/2:SELC2 := ØØ:FØ ;
@NESTED1/2:SELC3 := ØØ:FØ ;
```

UNEDITED

SOM_MCF.SING

APPNOTE 3.DNIX14