Section 6:

Design Submission

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INTRODUCTION
SUBMITTING A BIPOLAR or BiCMOS ARRAY-BASED CIRCUIT DESIGN TO AMCC

The following document has been designed to ensure you, the customer, of a successful transition from concept to finished part. It is a summary of the items required for the submission of a BiCMOS or bipolar array-based circuit design to AMCC, when the schematic capture and simulation vector generation has been performed by the customer. These items must be submitted to AMCC for use in the acceptance design review prior to committing the design to layout.

These are the critical information transfer areas which, if not completed, may delay the acceptance of your circuit.

This list was prepared for those customers who design with the DAISY, MENTOR, or VALID engineering workstation (EWS), or who will submit via the LASAR VERSION 6 system.

Schematics are to be prepared following AMCC schematic conventions. Refer to Volume II, Sections 3 and 7 for further information. These sections provide a detailed description of the AMCC rules for both EWS-generated and hand-generated schematics.

Functional and at-speed simulation or timing verification are required prior to releasing a design to layout. A design cannot be processed without customer-generated test vectors. For additional information on the test vector requirements and simulation procedures, refer to Volume II, Section 4, Vector Submission Rules and Guidelines.

Provided in the above-referenced document is a detailed description of the requirements for: a) functional; b) at-speed (or timing verifier); c) the optional AC test vectors and d) the optional parametric test vectors. Information is also included on the submission requirements for other hardware tests.

AMCC ARRAY DESIGN SUBMISSION CHECKLIST (REQUIRED)

Attached to this document is the AMCC DESIGN SUBMISSION CHECKLIST. It must be filled in and submitted with the design documentation.

The design submission checklist is a summary of the minimum documentation REQUIRED for a successful design submission.

The checklist is generic to all design submissions with the exception of one section which is EWS-specific. If non-standard operation of a system has been performed, add files as required to allow AMCC to duplicate the simulation conditions. Fill in the requested information for the EWS system used for the design submission.

AMCC ASSIGNED CIRCUIT NAME (REQUIRED IDENTIFICATION)
PRODUCT_NAME

When AMCC has received a purchase order for a circuit, AMCC assigns a code name (a.k.a circuit name, product name) to protect the proprietary nature of the customer's circuit. This code name should appear on the submission document and on all hardcopy documents as a single point of reference. It should be attached to the schematic chip macro as the PRODUCT_NAME parameter. If no such name assignment exists, use the first 4-6 letters of the company name as the ID.

DEVICE_NUMBER

Assigned with the PRODUCT_NAME, the DEVICE_NUMBER serves to identify the individual circuit. It may be defaulted if no number has been assigned.

ARRAY SERIES and SPECIFIC ARRAY

Clearly identify which array family and which array with that family is the one used for this design. The selection should match the chip macro identification.

MACRO LIBRARY VERSION (REQUIRED IDENTIFICATION)

The macro library release version number is on the label of the release media and on the upper right hand corner of the chip macros. The version used for the drawings and all execution files must be supplied on the submission checklist. Designers should always verify that they have the latest version of a library immediately prior to beginning schematic capture. Contact your local AMCC representative or sales office.

MACROMATRIX RELEASE VERSION

The MacroMatrix release number may vary from the library release. At present, the two numbers are the same. Supply this number on the checklist.

EWS SYSTEM OPERATING SYSTEM VERSION

Volume II, Section 7 clearly defines AMCC-EWS release compatibility and defines the minimum release level that is compatible with the AMCC MacroMatrix package. Where an EWS software package is available on several platforms, that information is also clearly defined in Section 7.

• VALID SOFTWARE VERSION (REQUIRED IDENTIFICATION)

The software release versions for ValidSIM, ValidTIME, and the Valid Operating System used in the simulations must be included on the checklist. Refer to Section 7 (809) of this manual for the latest AMCC-VALID release compatibility.

INDEX FILE FOR FLOPPY DISKS, TAPE (REQUIRED)

Each floppy disk (tape) submitted must contain its own text index file listing all files contained on that disk (tape), with a description of each file. Each disk (tape) should be clearly labeled as to its name and contents. All file names should be meaningful. One disk (tape) should contain a master file listing all disk (tape) files and their contents. A hardcopy of this master index file should also be submitted.

The index should comply with the instructions given in Volume II, Section 4.

SCHEMATIC DRAWING PAGES (REQUIRED)

The final versions of all schematic pages are to be submitted both on magnetic media and in hardcopy format. Two sets of the printed schematics (minimum) are required. One set must be clearly marked (highlighted) to show AC test paths and critical paths. Label AC test paths with the documentation AC test number. Label the critical paths with the timing correlation report path number.

AGIF NETLIST (CIRCUIT.SDI) (REQUIRED)

The final version of the AGIF (AMCC Generic Interface Format) netlist that was used as input to AMCCERC, AMCCANN, AMCCSIMFMT and AMCCVRC must be included on the media (disk or tape). The file is called CIRCUIT.SDI and is located in the .../ERC subdirectory.

ERC REPORT (REQUIRED)

The printed ERC report, AMCCERC.LST, must be submitted with the hardcopy and media documentation. Any error messages must be accompanied with an AMCC waiver (approved Pre-Approval Request or PAR) and a description as to their intended resolution.

DESIGN VALIDATION REVIEW (REQUIRED)

A complete and comprehensive validation review is required for design submission.

The Design Manuals for the individual array series contain a summary of the basic design rules and recommended checks for that array series as well as recommendations for ensuring both testability and reliability in the final circuit.

AMCC MacroMatrix support software includes the Engineering Rules Checks (ERC) program (AMCCERC) which supports many of the design rules and guidelines. In cases where there is no software support, the designer must perform the validation check manually.

More extensive information is available in Volume II, Section 5, Design Validation. The validation checklist covers BiCMOS and bipolar arrays. It is to be completed as part of the design submission package.

I/O LIST (REQUIRED)

The list of all signal I/O, added power and ground pads and fixed power and ground pads including signal I/O type (TTL standard, TTL open-collector, TTL 3-state, ECL 10K, ECL 100K, etc.) and clear identification of simultaneously switching outputs is called **AMCCIO.LST**. It must be included in the hardcopy and media documentation.

ANNOTATION and OUTPUT LOADING (REQUIRED)

AMCCANN AMCCPKG.LST
OUTPUT.DLY

Space is provided for annotation level, either Front-Annotation or Back-Annotation. Back-Annotation submissions are currently handled as special cases.

This release includes a user interface (AMCCANN) which allows the package, package pin capacitance and system loading to be specified for the circuit. Commentary information on frequency must be added for high-speed I/O (see Section 4). The list of all signals with pad placement (if known), package pin capacitance (Front-Annotation or final), and system load is called **AMCCPKG.LST**. It must be included in the hardcopy and media documentation. **OUTPUT.DLY** must be included on media.

The output capacitive load delays are included in the annotation files and is reflected in the simulation results. The delay files used in the simulations must be submitted on media. For Front-Annotation these are: **FNTNOM.ews**, **FNTMIN.ews**, and **FNTMIL.ews** or **FNTCOM.ews**.

CROSS REFERENCE (OPTIONAL)

The AMCC cross-reference file, AMCCXREF.LST can be submitted on media.

AMCCVRC (REQUIRED)
AMCCVRC.LST; signal analysis file

The vector rules check software, AMCCVRC, must have been run once for each submitted maximum worst-case sampled functional, AC test and parametric simulation file. The AMCCVRC.LST report for each case must be submittted on the media and any errors accompanied by an AMCC waiver. Space is provided on the simulation forms for the different AMCCVRC reports. Rename them when more than one is being submitted. (Refer to Volume II, Section 8, Appendix B.)

The AMCCVRC signal analysis file must also be submitted. Submit the AMCCVRC.LST reports on media and hardcopy.

FUNCTIONAL DESCRIPTION OF THE CIRCUIT (OPTIONAL)

AMCC prefers that a high-level functional description of the circuit on the array be included in the hardcopy documentation. This description should include the required performance of the circuit, any timing constraints, interface requirements, testing specifications and the operating environment.

BLOCK DIAGRAM OF THE CIRCUIT (OPTIONAL)

Unless a hierarchical schematic capture has been performed, AMCC prefers that a top-level block diagram of the circuit as configured for the array be included in the hardcopy documentation. If a hierarchical schematic capture has been performed, the top-level schematic may be sufficient.

PREPLACEMENT REQUESTS (OPTIONAL)

Preplacement of macros for critical timing requirements can be submitted to AMCC if the designer feels it to be necessary. All preplacement requests will be evaluated by AMCC, and the designer will be notified if they can or cannot be met.

PIN-OUT REQUESTS (OPTIONAL)

I/O placement may be of concern in a design, and the designer may wish to specify a pin-out request to AMCC. The final pin-out is driven by layout considerations and restrictions. The pin-out requests will be evaluated by AMCC, and the designer will be notified if they can or cannot be met.

CRITICAL PATH AND TIMING REQUIREMENTS (REQUIRED)

The maximum required frequency of operation for the circuit and the expected performance for the critical paths should be clearly stated in the hardcopy documentation following the procedure discussed in Volume II, Section 4, Vector Submission Rules and Guidelines. Use the Timing Correlation report form for any path not covered by an AC test.

FUNCTIONAL SIMULATION SUBMISSION (REQUIRED)

The functional simulation output vectors, consisting of all of the input and the expected output signals generated by the input stimulus file, are the actual vectors used by the AMCC test department to verify the correct functional operation of the part. The customer must supply all functional simulation vectors. AMCC uses functional vectors for fault grading and recommends 90% or better fault coverage of the final circuit.

AMCC requires that functional simulations be performed once using the MINIMUM library and then once using the maximum worst-case (MILITARY or COMMERCIAL) library.

Documentation included on disk or tape for the functional simulation includes:

1) the commented simulation control file;
2) a clear indication of which timing library and which simulation extreme was used (MAX or MIN);
3) the referenced data input file, if any, or any other referenced simulation input file;
4) submit procedures, a transcript of system operation during simulation, including VIEW, RUN, START, LIST, WRITE, etc. statements as required for the specific EWS;
5) the MAXIMUM worst-case sampled AMCCSIMFMT files produced (each page limited in size to a SENTRY tester page size of 4K);*
6) a text file version of the data or the control file which clearly describes the testing performed;
7) the Front-Annotation [FNTxxx.DSY] file used to perform the simulation. If more than one version of the Front-Annotation file is used, be certain that the media index clearly identifies which annotation file goes to which control and output files (see the simulation submission form);
8) the AMCCVRC.LST report with reset, set clearly documented if they caused Vector SSO errors;
9) the AMCCVRC signal analysis file;
and 10) MINIMUM worst-case sampled AMCCSIMFMTed simulation results if different from the worst-case MAXIMUM results.

Hardcopy documentation consists of any timing checks errors and the AMCCVRC.LST (may be more than one) commented for errors and AMCC waivers. Refer to the AMCCVRC User's Guide for RESET/SET errors. Errors due to RESET/SET are allowed but must be clearly documented.

The functional simulation should be performed following the procedures described in Volume II, Section 4, Vector Submission Rules and Guidelines.

* See Vector Length Check, AMCCVRC manual, Section 8, Appendix B.

AT-SPEED SIMULATION SUBMISSION (REQUIRED) *

The submitted at-speed simulation is one of the simulations that is rerun after layout to verify the actual timing performance for the array. The Back-Annotation file, which provides the ACTUAL metal delays for the layout, is used in place of the Front-Annotation file. At-speed simulation results provide an evaluation of the timing performance and help identify timing violations and potential timing problems. VALID users may use the Timing Verifier option in place of at-speed simulation.

AMCC requires that at-speed simulations be performed at the specified maximum operating frequency, and be performed using the MINIMUM library and then again using the maximum worst-case (MILITARY or COMMERCIAL) library.

Documentation included on disk or tape for the at-speed simulation includes:

1) the commented simulation control file;
2) the referenced data input file, if any (remote input vector file);
3) the type of simulation (MAX or MIN);
4) submit procedures, including VIEW, RUN, START, LIST, WRITE statements as required for the specific EWS;
5) the AMCCSIMFMT files produced (no limit on size - these files are not for tester use), one file is sampled and one file is print-on-change;
6) a file clearly describing the tests performed;
and 7) the Front-Annotation [FNTxxx.DSY] file used to perform the simulations. If more than one version of the Front-Annotation file is used, the individual simulation must reference the appropriate file (see the simulation submission form).

Hardcopy documentation consists of any timing checks errors and AMCC waivers.

The at-speed simulation should be performed following the procedures described in Volume II, Section 4, Vector Submission Rules and Guidelines.

VALID TIMING VERIFIER SUBMISSION (OPTIONAL)

The VALID timing verifier may be used to perform the required timing analysis prior to design submission in place of the at-speed simulation. It is used to verify the correct maximum operating frequency of the circuit and analyzes the internal set-up time, hold time and minimum pulse width requirements of the macros to guarantee that they are satisfied. It can also be used to verify external set-up and hold time conditions for the circuit.

The timing verifier may also be used to supply the maximum worst-case path propagation delay measurements in lieu of functional or at-speed simulation print-on-change output files.

The timing verifier is rerun after layout to verify the actual timing performance for the array. The Back-Annotation file, which provides the ACTUAL metal delays for the layout, is used in place of the Front-Annotation STATISTICAL metal-delay file.

Documentation included on tape for the timing verifier execution includes:

1) the verifier directives file (verifier.cmd);
2) the plottime directives file (td.cmd);
3) the Front-Annotation delay file used (delay.dat);
4) the case analysis file (case.dat);
5) the ASCII output file (plotsig.dat);
6) the timing verifier execution files (tvlog.dat and tvlst.dat);
7) the timing drawings (GED plots of verifier results);
8) the cmp*.dat compiler filesn;
and 9) the compiler.cmd file.

Hardcopy documentation should contain one copy of each media file.

AC TESTS:
PROPAGATION PATH DELAY VECTOR SUBMISSION (OPTIONAL)

AC testing is an automated testing method used to examine in close detail circuit performance measurements of propagation delay. A separate set of vectors is required for each measurement, and each set must initialize and bias the path and provide the means by which the measurement can be made. If this testing option is desired, then these vectors must be supplied in addition to the functional and at-speed vectors.

A maximum of 10 paths and 20 tests can be tested per array. Refer to the Vector Submission Rules and Guidelines concerning a concatenated set of vectors (rather than up to 40 individual files).

AMCC requires that AC test simulations be performed using the MINIMUM library and then again using the maximum worst-case (MILITARY or COMMERCIAL) library.

AC test maximum worst-case sampled simulation output files must be processed through AMCCVRC. Documentation requirements are the same as for Functional simulation, with the addition of the print on change files.

The vector set is simulated and documented as for a functional simulation (100ns MINIMUM step) with the addition of the AMCCSIMFMT PRINT_ON_CHANGE output files tracing the paths in question. (Media copies only.)

The AC Test simulations should be performed following the procedures described in Volume II, Section 4, Vector Submission Rules and Guidelines. AMCC will run the AC test simulation after the Back-Annotation file is available.

The AC tests have their own set of forms for the sampled files and for the print-on-change files attached to the submission checklist. AC test submission will be automated in the next MacroMatrix release.

PARAMETRIC VECTORS (OPTIONAL)

Parametric testing is optional. The Vector Submission Rules and Guidelines document defines the type of vectors required if parametric testing is to be performed.

Documentation included on disk or tape for the parametric simulation includes:

1) the commented simulation control file;
2) the referenced data input file, if any, or any other referenced simulation input file;
3) submit procedures, a transcript of system operation during simulation, including VIEW, RUN, START and LIST, etc. statements as required for the specific EWS;
4) the sampled AMCCSIMFMT files produced (each page limited in size to a tester page size of 4K);*
5) a text file version of the data or the control file which clearly describes the testing performed (optional);
6) the Front-Annotation [FNTxxx.DSY] file used to perform the simulation;
7) the AMCCVRC.LST report with reset, set clearly documented if they caused Vector SSO errors, (special parametric checks will be added in a future release);
8) the AMCCVRC signal analysis file;

Hardcopy documentation consists of AMCCVRC.LST commented for errors and AMCC waivers.

The parametric simulation should be performed following the procedures described in Volume II, Section 4, Vector Submission Rules and Guidelines.

* Refer to the Vector Length Check in the AMCCVRC User's Guide, Volume II, Section 8, Appendix B for exceptions to this.

REQUESTING HARDWARE TESTING (OPTIONAL)

This is an optional service. These are characterization-only tests, performed on a limited quantity, one-time basis. Refer to Volume II Section 4, Vector Submission Rules and Guidelines for further information.

MACROMATRIX INSTALLATION AND OPERATION

Refer to Volume II, Section 7 of the AMCC Design Manual for library installation information, EWS software release levels supported, and EWS-specific schematic rules. A design flow overview is also included in Section 7. A beginning EWS designer should review Application Note 1 in the appendix of Volume II, Section 2, Design Methodology, for further detail on design flow and the steps involved.

[As of the (809) release, DAISY and MENTOR Application Note 1.DNIX and Application Note 1.MENTOR have been released. Application Note 1.VALID and Application Note 1.LASAR are in preparation.]

Refer to Volume II, Section 8, for the listing of the AMCC MacroMatrix ERC error messages and the possible circuit design errors that would cause those messages to be printed.

Also refer to Section 7 for information on AMCCANN, AMCCSIMFMT, the AMCC Vector Rules Checker (AMCCVRC) and AMCCFILUTL (DAISY).

ADDITIONAL COPIES OF THIS DOCUMENT

Additional copies of this document, AMCC Design Submission, and of the validation checklist, AMCC Design Validation, are available from AMCC in an 8.5x11" format.

FUNCTIONAL, AT-SPEED and PARAMETRIC SIMULATION FORM

The simulation submission forms require at least one functional simulation run at worst-case maximum. The items requested are:

File # Item number, 1,2,3...

AMCCSIMFMT OUTPUT FILENAME The user-defined name assigned to the formatted simulation output file (the vectors being submitted). The input to AMCCSIMFMT is from a VALID tabular trace output, MENTOR LIST or DAISY VLAIF output file.

MIN Check if this is a MINIMUM simulation. This assumes a MIN timing library and FNTMIN.ews.

MAX Check if this is a MAXIMUM simulation. This assumes a MAX timing library and FNTMIL.ews or FNTCOM.ews.

SIMULATION CONTROL FILENAME The file required by the EWS to input stimulus, etc. that was used to perform the submitted simulation. It is called the M_MCF.SING file on DAISY, the transcript file on MENTOR, the directives file on VALID.

SIMULATION INPUT FILENAME Any other required input file. Called the remote data VLAIF file on DAISY, the stimulus input file on VALID. Mentor may have a data file called from the force file. The existance of this file depends on the method used to create the stimuli.

SIMULATION COMMAND FILENAME The transcript or log of operations or submit process, i.e., what it would take for AMCC to duplicate the simulation.

AMCCVRC REPORT FILENAME Either AMCCVRC.LST or a user-defined name when more than one is to be submitted. List the one that goes with the netlist and AMCCSIMFMT output file. AMCCVRC is not required for minimum simulations, for sampled at-speed simulations, or for print-on-change simulations.

AMCCVRC SIGNAL ANALYSIS FILENAME The clock race-condition test requires a signal analysis file to specify clock-data relationships. A user-defined name.

SIMULATION DESCRIPTION FILE The text file, may be a commented copy of the AMCCSIMFMT output file, which describes the testing being performed.

EWS-SPECIFIC FILES

DAISY SPECIFIC FILES

- /AMCC/Qxxx_LIBS PROFILE FILE (REQUIRED FOR DAISY)

For reference, the DAISY PROFILE file must be included on the floppy disks. This file identifies the SIFT files used to perform the simulations. If more than one version was used, the individual simulations must reference the SIFT file used.

- DLS CONFIGURATION FILE (REQUIRED FOR DAISY)

For reference, the "/AMCC/CONFIG DLS_CONFIG" file must be included on the floppy disks. This file shows the DISPLAY_BUFFER_LENGTH xxx and the TIME_UPDATE_INTERVAL xxxx used during the simulation. If more than one version was used, the individual simulations must reference the configuration file used.

- DLS and DTV MODE FILES (REQUIRED FOR DAISY)

The MODE file used during each simulation must be documented on floppy disk, and the individual simulations must reference the MODE used (NOM, MIN, MAX or a range such as NOM/MAX or MIN/MAX).

AMCC DESIGN SUBMISSION CHECKLIST (809)

TEST SUBMISSION - ONE PER DESIGN SUBMISSION

= =

Date: ______________________________

Company Name: ______________________________

Designer: ______________________________

Phone Number: (________) - ______________________________

AMCC PRODUCT_NAME: (Code Name) ______________________________

AMCC DEVICE_NUMBER: ______________________________

= =

Fill in and submit with design submission package:

AMCC ARRAY SERIES: Q5000 _____ Q14000 _____ Q20000 _____ OTHER _______

AMCC ARRAY: ______________________________

MacroMatrix RELEASE VERSION: ______________________________

Macro Library RELEASE VERSION: ______________________________

EWS OPERATING SYSTEM AND SOFTWARE VERSIONS:

Daisy: Operating System Version: ______________

Aplication Software Version: ______________

Character graphics
DED ________
DED2 ________
Logic Simulator: DLSI ________

Bit-Mapped Graphics:
DED2 ________
ACE ________
DLSII ________

Valid: Operating System Version: ________

Validsim: ________

Validtime: ________

Mentor: Operating System Vertion: ________

Lasar 6: TBS

All users: Refer to Section 7 for required software levels for the system you are using

ANNOTATION LEVEL: ______ FRONT-ANNOTATION
(check one) ______ BACK-ANNOTATION

Maximum Operating Frequency: ________MHz

Power (Maximum Worst Case): ________W

Different from ERC? ____Yes ____No

MEDIA FILES REQUIRED IN SUBMISSION (check if included):

(simulation files are listed on the following pages)

[ ] Media Index file (READ.ME)
[ ] CIRCUIT.SDI
[ ] AMCCERC.LST
[ ] AMCCIO.LST
[ ] OUTPUT.DLY
[ ] AMCCPKG.LST

[ ] FNTMIN.ews*
[ ] FNTNOM.ews*
[ ] FNTCOM.ews*
[ ] FNTMIL.ews*
[ ] Schematic Drawing Pages

*ews = DSY. MEN. VAL, etc.

AMCC DESIGN SUBMISSION CHECKLIST (80

HARD COPY REQUIRED (check if included):

- [ ] Schematics (2 sets)
- [ ] AMCCERC.LST
- [ ] AMCCIO.LST
- [ ] AMCCVRC.LST
- [ ] AMCCPKG.LST
- [ ] Media Index file (READ.ME)
- [ ] Design Validation

_____ Number Submitted

OPTIONAL:

- [ ] Functional Description
- [ ] Block Diagram
- [ ] Pin-out Request
- [ ] AMCCXREF.LST
- [ ] Preplacement Request

WAIVERS (APPROVED PARS) INCLUDED IN SUBMISSION: _____

LIST PAR #S: _____

_____

_____

AMCC DESIGN SUBMISSION CHECKLIST (809)

EWS SPECIFIC

[ ] DAISY SPECIFIC FILES

- [ ] DAISY MODE FILES
  - [ ] MIN for MINIMUM SIMULATION, filename:_____
  - [ ] MAX for MAXIMUM SIMULATION, filename: _____
- [ ] PROFILE FILE
- [ ] CONFIGURATION FILE
- [ ] NESTED FILE (nested submissions)

[ ] VALID TIMING VERIFIER SUBMISSION

[ ] Verifier derectives file	(verifier.cmd)
[ ] Plottime directives file	(td.cmd)
[ ] Front annotation file	(delay.dat)
[ ] Case analysis file	(case.dat)
[ ] ASCII output file	(plotsig.dat)
[ ] Verifier execution files	(tvlog.dat; tvlst.dat)
[ ] Timing drawings	(GED polts of verifier results)
[ ] Compiler files	(cmp*.dat)

[ ] MENTOR DESIGN TREE COMPLETENESS CHECK

[ ] dlv <design name>
[ ] link file present ($cglb)
[ ] design.erel files (ERC and simulation database)
[ ] all sheetl.nrel, links, directories and .pic files
[ ] ERC output file
[ ] simulation transcript input file(s)
[ ] LIST file(s) with input signals, binary only option
[ ] LIST file(s) with output signals, binary only option
[ ] LIST file(s) with output signals, change only option (At-speed; path propagation)
[ ] output LIST file(s) - sampled (Functional)
[ ] input/output LIST files in binary format
[ ] design release document file

[ ] LASAR VERSION 6

TBS

AMCC DESIGN SUBMISSION CHECKLIST
ALL FUNCTIONAL, PARAMETRIC SIMULATIONS

(809)

Company Name: _____ Date: _____

Designer: _____ Phone Number: (_____) - _____

AMCC PRODUCT_NAME: _____ AMCC DEVICE_NUMBER: _____

PRODUCT_GRADE: ____ MIL ____ COM

FILE #	AMCCSIMFMT OUTPUT FILE NAME	MIN	MAX	SIMULATION CONTROL FILENAME	SIMULATION INPUT FILENAME	SIMULATION COMMAND FILENAME	AMCCVRC REPORT NAME	AMCCVRC SIG. ANALYSIS FILENAME	SIMULATION DESCRIPTION FILENAME
FUNCTIONAL SIMULATION SUBMISSION (SAMPLED ONLY): (1 MAXIMUM SIMULATION IS REQUIRED)									
PARAMETRIC SIMULATION SUBMISSION (SAMPLED ONLY): (1 MAXIMUM SIMULATION IS REQUIRED FOR PARAMETRICS)									

AMCC DESIGN SUBMISSION CHECKLIST (809)

AT SPEED SIMULATIONS

Company Name: _____ Date: _____

Designer: _____ Phone Number: (_____) - _____

AMCC PRODUCT_NAME: _____ AMCC DEVICE_NUMBER: _____

PRODUCT_GRADE: ____ MIL ____ COM

FILE #	AMCCSIMFMT OUTPUT FILE NAME	MIN	MAX	SIMULATION CONTROL FILENAME	SIMULATION INPUT FILENAME	SIMULATION COMMAND FILENAME	AMCCVRC REPORT NAME	AMCCVRC SIG. ANALYSIS FILENAME	SIMULATION DESCRIPTION FILENAME
AT-SPEED SIMULATION SUBMISSION (SAMPLED): (1 MAXIMUM AND 1 MINIMUM SIMULATION ARE REQUIRED)									
							N/A	N/A	
							N/A	N/A	
							N/A	N/A	
							N/A	N/A	
							N/A	N/A	
AT-SPEED SIMULATION SUBMISSION (PRINT-ON-CHANGE): (1 MAXIMUM AND 1 MINIMUM SIMULATION ARE REQUIRED)									
							N/A	N/A	
							N/A	N/A	
							N/A	N/A	
							N/A	N/A	

AMCC DESIGN SUBMISSION CHECKLIST (809)

AC TEST SUBMISSION - ONE PER AC SUBMISSION

Date: _____

Company Name: _____

Designer: _____

Phone Number: (_____) - _____

AMCC PRODUCT_NAME (CODE NAME): _____

AMCC DEVICE _NUMBER: _____

Fill in one of these sheets for each AC Test

AC Test Number: _____

AMCCSIMFMT Sampled Output Filename: _____

AMCCSIMFMT Print On Change Filename: _____

Test is: MAXIMUM _____

Concatenated Files: ____ Yes ____ No

Test Description: _____

_____

_____

_____

_____

_____

Test Start Address (If not Zero): _____

Vector Address of Transition: _____

Input Signal Name: _____ Transition : Rise ____ Fall ____

Output Signal Name: _____ Transition: Rise ____ Fall ____

For a MAXIMUM test: MAXIMUM DELAY SPECIFICATION: _____ ns

Annotated simulation measurement of this path: _____ ns

(from filename: _____)

Package pin capacitance used for this path: _____ pf

(from AMCCPKG.LST)

System load capacitance used for this path: _____ pf

(from AMCCPKG.LST)

AMCC DESIGN SUBMISSION CHECKLIST
AC TEST SIMULATION (OPTIONAL) SAMPLED

(809)

Company Name: _____ Date: _____

Designer: _____ Phone Number: (_____) - _____

AMCC PRODUCT_NAME: _____ AMCC DEVICE_NUMBER: _____

PRODUCT_GRADE: ____ MIL ____ COM

FILE #	AMCCSIMFMT OUTPUT FILE SAMPLED NAME	MIN	MAX	SIMULATION CONTROL FILENAME	SIMULATION INPUT FILENAME	SIMULATION COMMAND FILENAME	AMCCVRC* REPORT NAME	AMCCVRC SIG. ANALYSIS FILENAME	SIMULATION DESCRIPTION FILENAME
(1 MAXIMUM AND 1 MINIMUM SIMULATION ARE REQUIRED)									
1									
2									
3									
4									
5									
6									
7									
8									
9									
10									

*except toggle test

AMCC DESIGN SUBMISSION CHECKLIST (809)

AC TEST SIMULATION (OPTIONAL) SAMPLED

Company Name: _____ Date: _____

Designer: _____ Phone Number: (_____) - _____

AMCC PRODUCT_NAME: _____ AMCC DEVICE NUMBER: _____

PRODUCT_GRADE: ____ MIL ____ COM

FILE #	AMCCSIMFMT OUTPUT FILE SAMPLED NAME	MIN	MAX	SIMULATION CONTROL FILENAME	SIMULATION INPUT FILENAME	SIMULATION COMMAND FILENAME	AMCCVRC* REPORT NAME	AMCCVRC SIG. ANALYSIS FILENAME	SIMULATION DESCRIPTION FILENAME

(1 MAXIMUM AND 1 MINIMUM SIMULATION ARE REQUIRED)

11									
12									
13									
14									
15									
16									
17									
18									
19									
20									

*except toggle test

AMCC DESIGN SUBMISSION CHECKLIST (809)

AC TEST SIMULATION (OPTIONAL) - CHANGE FILE

Date: _____

Company Name: _____

Designer: _____

Phone Number: (_____) - _____

AMCC PRODUCT_NAME (CODE NAME): _____

AMCC DEVICE_NUMBER: _____

PRODUCT_GRADE: ____ MIL ____ COM

FILE #	AMCCSIMFMT OUTPUT CHANGE FILENAME	MIN	MAX	SIMULATION CONTROL FILENAME	SIMULATION INPUT FILENAME	SIMULATION COMMAND FILENAME	SIMULATION DESCRIPTION FILENAME
(1 MAXIMUM AND 1 MINIMUM SIMULATION ARE REQUIRED)							
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							

AMCC BIPOLAR, BICMOS LOGIC ARRAY

(809)

TIMING CORRELATION REPORT

Company Name: _____ Date: _____

Designer: _____ Phone Number: (_____) - _____

AMCC PRODUCT_NAME: _____ AMCC DEVICE_NUMBER: _____

PATH #	INPUT SIGNAL NAME (name)	INPUT SIGNAL OCCURS (ADR)	INPUT OF STIMULUS H-L or L-H	OBSERVABLE OUTPUT (name)	OUTPUT AVAILABLE/ OBSERVABLE (adr)	TRANSITION OF OUTPUT SIGNAL H-L or L-H	EXTERNAL NON-STANDARD LOAD (pF)	TARGET PERFORMANCE (ns)	FRONT ANNOTATION PERFORMANCE (ns)	BACK ANNOTATION PERFORMANCE (ns)
1										
2										
3										
4										
5										

(MAKE COPIES AS NEEDED)

AMCC PRODUCT_NAME:_____

P.O. # _____ AMCC DEVICE_NUMBER_____ CUSTOMER PART #_____

CIRCUIT DEVELOPMENT APPROVAL AND AUTHORIZATION TO PROCEED

Having reviewed the **FRONT ANNOTATED LOGIC SIMULATION** results provided, I hereby authorize AMCC to continue through back annotated logic simulation.

Signature_____

Title_____ Date _____

Having reviewed the **FAULT GRADING** results provided, I hereby authorize AMCC to continue with the circuit design.

Signature_____

Title_____ Date _____

Having reviewed the **BACK ANNOTATED LOGIC SIMULATION** results provided, I hereby authorize AMCC to continue through prototype manufacture.

Signature_____

Title_____ Date _____

PROTOTYPE APPROVAL

Having received and tested the devices provided, I hereby approve the above named **PROTOTYPES** as meeting all design and functional requirements.

Signature_____

Title_____ Date _____