# Section 4:

# Simulation Rules

## VECTOR SUBMISSION RULES ANDGUIDELINES

FIGURES

# AMCC VECTOR SUBMISSION RULES AND GUIDELINES

## INTRODUCTION

The following document has been designed to ensure you, the designer, of a successful transition from concept to finished part through a detailed examination of the simulations AMCC requires and the rules for their development and submission.

These are the critical information transfer areas which, if not correctly completed, may delay the implementation of your circuit.

This document supplements the specific EWS, LASAR 6 or AMCC Implemented Design Submission document.

- Functional and at-speed simulation and some means of timing verification are required prior to design submission.

- All simulation results submitted must have been created from annotated simulations. All simulations must use the same type of annotation (i.e., all are Front- or all are Back-Annotation).

- Timing checks must be turned on (be active) during all simulations.

- All timing errors flagged must be resolved prior to design submission.

A design cannot be processed without customer-generated simulation vectors. Functional, at-speed and the optional AC simulation vectors must be developed by the customer. While AMCC does not create the functional, at-speed or AC test simulation vectors for a design, we can assist in adding sufficient functional simulation vectors to obtain the recommended 90% or better fault coverage.

**FAULT GRADING SUPPORT:**

AMCC will perform fault grading, if desired, using TEGAS 5 or LASAR 6 software, the choice of which is at the discretion of AMCC.

## GENERAL INFORMATION

### AMCC ASSIGNED CIRCUIT NAME (REQUIRED IDENTIFICATION ON ALL DOCUMENTS AND MAGNETIC MEDIA LABELS)

When AMCC has received a purchase order for a circuit, AMCC assigns a code name to protect the proprietary nature of the customer's circuit. This code name MUST appear on the submission document, on all hardcopy documents and on all magnetic-media labels as a single point of reference, along with a date and a revision letter. The circuit name or code name is the value assigned to the PRODUCT_NAME chip macro parameter on the schematics.

### INDEX FILE FOR MEDIA (REQUIRED)

The machine-specific commands used to create the AMCC-readable magnetic-media files should be submitted as a means of indexing that magnetic-media. Clearly mark the location of a "read-me-first" text file that contains an index listing each file with a brief, meaningful description of the contents of each file. Submit the index file in media and hardcopy.

- All files must have meaningful file names.
- Descriptions must clearly identify functional and at-speed vectors and thier related files, and must be for both multipliers (maximum worst-case and minimum worst-case).
- If the optional AC test vectors are submitted, the AC vectors and their related files must be clearly identified.
- If the optional parametric vectors are submitted, the parametric vectors and their related files must be clearly identified.

I/O LIST (REQUIRED)
AMCCIO.LST; AMCCPKG.LST

A list of all signal I/O pads including I/O type (TTL standard, TTL open-collector, TTL 3-state, ECL 10K, ECL 100K) and clear identification of simultaneously switching outputs must be included in the hardcopy documentation. Also include thermal diode pads, VBxx macro pads and monitor points in the list.

Groups of simultaneously switching outputs and the maximum worst-case number of simultaneously switching TTL and ECL outputs must be clearly identified. The schematic macro parameter **SWGROUP** must be used. Standard power and ground pins and any identified extra power and ground pins must be listed.

An I/O list form is generated by the MacroMatrix ERC software and is called **AMCCIO.LST**. It will include fixed and added power and grounds, VBB and the thermal diode I/O signals.

Additional information (toggle frequency, ECL termination, package pin capacitance and system capacitive load) is entered using **AMCCANN** (AMCC annotation-interface software). **AMCCANN** will produce a second report, **AMCCPKG.LST** in addition to generating the complete annotation files.

**AMCCPKG.LST** will not be final until placement is complete and the file **CIRCUIT.PKG** has been downloaded to the EWS. Back-Annotation files are generated using CIRCUIT.PKG.

For Front-Annotation design submissions, submit **AMCCPKG.LST** as it is generated by the EWS.

For Back-Annotation design submissions, submit the final and complete **AMCCPKG.LST** report.

## CRITICAL PATH AND TIMING REQUIREMENTS (REQUIRED)

The maximum required frequency of operation for the circuit and the expected target performance for the critical paths should be clearly stated in the hardcopy documentation.

Paths which are within 10% of the maximum specifications, as defined by design or system constraints, are considered critical paths. The designer must supply a description of the critical paths and the maximum propagation delay allowable. The corresponding critical paths must be highlighted on one set of the schematics.

Note that target performance is not a part requirement, it is a goal. For critical paths that are to be treated as device specifications, an AC test may be required.

Use the attached form when the path is not to be part of an AC test. Fill out both halves of the form for each path. Use additional forms if necessary. Addresses requested are the vector time stamps in the at-speed print-on-change simulation output file.

## TIMING CORRELATION REPORT

Company Name: _____ Date: _____

Designer: _____ Phone Number: (_____) - _____

AMCC PRODUCT_NAME: _____ AMCC DEVICE_NUMBER: _____

4-1-10

| PATH # | INPUT SIGNAL NAME (name) | INPUT SIGNAL OCCURS (ADR) | INPUT OF STIMULUS H-L or L-H | OBSERVABLE OUTPUT (name) | OUTPUT AVAILABLE/ OBSERVABLE (adr) | TRANSITION OF OUTPUT SIGNAL H-L or L-H | EXTERNAL NON-STANDARD LOAD (pF) | TARGET PERFORMANCE (ns) | FRONT ANNOTATION PERFORMANCE (ns) | BACK ANNOTATION PERFORMANCE (ns) |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | | | | | | | | | |
| 2 | | | | | | | | | | |
| 3 | | | | | | | | | | |
| 4 | | | | | | | | | | |
| 5 | | | | | | | | | | |

(MAKE COPIES AS NEEDED)

## IDENTIFYING THE TIMING LIBRARY USED (REQUIRED)

Each simulation must clearly identify the library used to perform the simulations (MIN, COM (bipolar), COM4 (BiCMOS, -4.5V), COM5 (BiCMOS, -5.2V, +5V), MIL). (See the chart on the next page.) One set of functional, at-speed and AC test simulations must be performed using the maximum worst-case library. A second set of functional, at-speed and AC simulations must be performed using the minimum worst-case library.

The library identification should not be confused with the specification of the multipliers within the timing library. If the simulator allows MIN/MAX simulations (i.e., signal ambiguity or signal-tracking analysis), the mode used for each simulation must be identified.

## SIMULATION SYSTEM CONFIGURATION (REQUIRED)

Any unique settings made to a system during a simulation that could affect the simulation execution should be documented. Sufficient information must be included to allow the AMCC Implementation Engineer to duplicate the simulations submitted as a circuit design verification step. Consult the design submission section in Volume II, Section 6 of the Design Manual.

## ANNOTATION

Front-Annotation delay files can be generated for all AMCC-supported EWS systems. Back-Annotation delay files are partially generated on the AMCC VAX/VMS system and downloaded to an EWS for final processing by AMCCANN. Output load annotation is EWS resident.

- For customers submitting with Front-Annotation, all simulations must be done using the correct Front-Annotation delay files.
- For customers submitting with Back-Annotation, all simulations must be done using the correct Back-Annotation delay files.
- With this release, the user interface output load module will allow the specification of package pin capacitance and system capacitive load. All annotation files used in the simulations must include these delays.
- No Annotation delay files may be edited without a waiver from AMCC.

| TIMING LIBRARY | | ANNOTATION FILE | Power Supply |
|---|---|---|---|
| MILITARY | MIL | FNTMIL.ews, BCKMIL.ews | any |
| COMMERCIAL | COM | FNTCOM.ews, BCKCOM.ews | any (bipolar) |
| COMMERCIAL | COM4 | FNTCOM.ews, BCKCOM.ews | -4.5V BiCMOS |
| COMMERCIAL | COM5 | FNTCOM.ews, BCKCOM.ews | -5.2V; +5V BiCMOS |
| NOMINAL | NOM | FNTNOM.ews, BCKNOM.ews | any |
| MINIMUM | MIN | FNTMIN.ews, BCKMIN.ews | any |

ews = EWS extension or VAX extension

SIMULATION FORMAT (GENERAL)

The files documenting the signals and their order for the simulation output file for functional, at-speed and AC test simulations must be included in the documentation submitted. All simulation output files must use the same format (signals present and the order they are in). All simulation output files must be submitted as unedited AMCCSIMFMT output files.

All simulation output files must be submitted in BINARY format. Any simulations submitted in HEX, OCTAL or DECIMAL format are considered to be for reference only. The simulation output file MUST contain only the symbols 1, 0, X or Z for any one datapoint (single bit). Only 3-stated outputs can have a Z in their data column, to indicate a high-impedance state.

When using busses, refer to the EWS-specific MacroMatrix Installation in Volume II, Section 7 of the Design Manual.

AMCCSIMFMT

AMCCSIMFMT, the MacroMatrix AMCC Simulation Format package, is available on all AMCC-supported EWS systems. TEGAS display output is already in approved AMCC format.

- Only AMCCSIMFMT output simulation files may be submittted.

**SIMULATION MATRIX**

| REQUIRED SIMULATIONS | | | | | | | | OPTIONAL SIMULATIONS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FUNCTIONAL | | | | AT-SPEED | | | | AC TEST | | | | PARAMETRIC | | | |
| MIN | | MAX | | MIN | | MAX | | MIN | | MAX | | MIN | | MAX | |
| SAM | POC | SAM | POC | SAM | POC | SAM | POC | SAM | POC | SAM | POC | SAM | POC | SAM | POC |
| X | | X | | X | X | X | X | X | X | X | X | | | X | |

## FUNCTIONAL SIMULATION SUBMISSION (REQUIRED)

Functional simulation output vectors consist of all of the input and the expected output signals generated by the input file. These vectors provide a time independent, sequential state description of the circuit after any input change has propagated through the logic and all of the outputs have settled to their stable state. The functional simulation provided to AMCC should contain sufficient vectors to provide verification of the logic.

The functional simulation output vectors are the source for the actual test program that will be used to test the physical parts during production. The customer should supply all functional simulation vectors required for the recommended 90% or better fault coverage of the final circuit.

Functional simulation input vectors must be in a format compatible with AMCC-readable magnetic-media. If the design is submitted using DAISY, MENTOR, VALID, LASAR 6, etc., then the media format should be in compliance with that system's requirements.

An example functional simulation AMCCSIMFMT file is shown in Figure 4-2-1.

## FAULT GRADING - APPLIED TO THE FUNCTIONAL SIMULATION

Fault grading is a measure of the fault coverage - a "grade" on the quality of the fault detection provided by the submitted functional simulation vectors. A fault grading score of 100% means that if a SA1 or SA0 fault exists at any single node within the circuit it will be detected during the tester functional testing phase.

- Single fault detection, the detection of a stuck-at fault (SA1, SA0) at any single node in the circuit, requires that the node be "covered" by at least one simulation vector. A node is covered by the vector set when the state of at least one circuit primary output for at least one vector is different when the failure is present than when the failure is absent. A failure at a circuit node that is not covered by the functional simulation vector set will not be detected. (SA1 = stuck-at-1; SA0 = stuck-at-0. A stuck-at fault is a physical open or short circuit, i.e., a "hard" failure.)

- Redundancy in the circuit produces fault-masking and will reduce the obtainable fault-coverage since it reduces the observable nodes. The addition of test points when the redundancy is deliberate, and the minimization of the circuit when it is not, are recommended approaches to improve testability. The design methodology section of Volume I of the Design Manual contains a summary of designing-for-testability and designing-for-reliability recommendations.

- There are no requirements for fault location, i.e., the identification of the exact point of failure. Multiple-fault detection, a less-probable occurrence, is also not required although most single-fault minimal test sets and minimal test sequences will provide 100% fault coverage of all observable faults and will also detect the presence of some multiple faults.

## FUNCTIONAL SIMULATION RULES

- AMCC prefers that initialization be performed by a reset or set. If that is not possible, AMCC prefers that the number of vectors required for circuit initialization not exceed 25. If initialization in 25 steps is not possible, consult AMCC.

A circuit is initialized when the internal nodes and the primary inputs and primary outputs are in known states. [AMCCVRC unknown signal check]

Note: AMCCVRC currently checks for the 25 vector initialization limit. This will be relaxed to 100 vectors in the next MacroMatrix release due to the larger arrays.

- Initialization **MUST** occur at the beginning of each 4K page for arrays with 120 or less available (not used) signal pads; at the beginning of each 16K page for arrays with more than 120 available signal pads. [AMCCVRC size check]

- Initialization **MUST** also occur between functional test sets or sequences. "Home" the circuit to a known state before beginning the next test. Embedded initialization, if it violates the SSO limit, must be a complete initialization and must be documented with start and stop addresses. (Document the address at which functional test monitoring should resume.)

- All primary inputs, all primary outputs, all bidirectionals and then any 3-state or bidirectional enables, **IN THAT ORDER MUST** appear in the format for all simulations. A primary input is a signal coming into the array from the outside world. A primary output is a signal going from the array to the outside world. Interface macros (macros containing an input or an output PAD) **MUST** be used to connect to these signals. [AMCCVRC required signal check - existence of signal, not its order in the result file]

- All internal signals that are attached directly to bidirectional or 3-state enable pins **MUST** be listed in the simulation output, following the primary outputs. There are no exceptions. [AMCCVRC required signal check]

- The signal ordering as required by AMCC for all functional, at-speed and AC-test simulation output files is as follows:
  - All primary inputs
  - All primary outputs
  - All primary bidirectional I/O, if any
  - All 3-state or bidirectional enables, if any.

- No other internal signals may appear in the submitted simulation output files. [AMCCVRC required signal check]

• VBxx macro, thermal diode I/O macro and monitor point signals should not appear in the Functional vector format. If they are listed, they are ignored by AMCCVRC during the toggle test. These signals are not considered to be primary I/O signals.

• All primary outputs **MUST** toggle from 0 to 1 and from 1 to 0 within the vector set (first 4K vectors) to enable $V_{OH}$ and $V_{OL}$ testing. AMCC prefers that this occur in the first 1K vectors. [AMCCVRC toggle check]

• All primary inputs must toggle from 0 to 1 and from 1 to 0 within the functional vector set. AMCC prefers that all inputs toggle in the first 4K vectors. [AMCCVRC toggle check]

• All inputs and bidirectionals used as inputs **MUST** be initialized to a 1 or 0 state in the **first** simulation step whether or not they are active in the current test. [AMCCVRC unknown signal check]

• All inputs that are static for a given test **MUST** be forced to '1' or '0'. The "X" unknown state MUST not be used. [AMCCVRC unknown signal check]

• All sampled simulation output files submitted to AMCC **MUST** be in paged AMCC Simulation Format (AMCCSIMFMT). A simulation vector page is limited to 4K vectors (applies when the array has 120 or less I/O cells available) or 120K vectors (applies when the array has more than 120 I/O cells available).

• The output of the AMCCSIMFMT software program **MUST** not be altered in any way. It is an executable file.

• The simulation output file used as input to the AMCCSIMFMT program **MUST** be a **sampled** output (uniform step between vectors).

• Longer patterns **MUST** be built in independently initializable segments of length less than or equal to 4K (use multiple pages). Most designs can be tested in 4K vectors.

• **AMCC limits functional simulations to 16K vectors.** Consult your local AMCC Sales Representative if your vectors exceed 4K.

Note: The SENTRY tester adds control vectors as follows:

| | |
|---|---|
| bididirection change (I->O; O->I) | +2 |
| 3-state, Bidi UKN->KNOWN; KNOWN->UKN; | +1 |
| HiZ->output; output->HiZ | +1 |

Allowances must be made for these vectors on any page. [AMCCVRC length check]

• AMCC prefers that short input vector sets be concatenated (assembled) to produce a large (up to 4K) output vector set for submission. Submission consisting of multiple, small, independent output vector sets is not preferred. Simulate the concatenated input files.

• The transition control signal (normally a clock input) MUST occur within the same simulation output vector that the transition output change occurs. (The expected signal output pattern for a given input signal pattern is contained in the same simulation output vector.)

• The output is sampled just before the next input signal pattern arrives, normally one simulator time unit prior to the change.

• The active edge clock signal and the data signals affected by that clock MUST not change simultaneously. [AMCCVRC race check]

• If a clock is generated by two or more signals, at any point in time, only one clock signal can be changing and active while the other(s) MUST be held stable. Simultaneous changes of these signals is not allowed. Using both signals can produce glitches and false clocking due to race conditions.

• Heavily switching sequences (with more than 8 or 16 simultaneously switching outputs, depending on the I/O mode) MUST be placed at the end of the test pages (last one third of the vector set). [AMCCVRC SSO check]

| | |
|---|---|
| 100% TTL | 16 TTL outputs |
| 100% ECL | 16 ECL outputs |
| any mixed ECL/TTL | 8 TTL outputs; 8 ECL outputs, limits are independent |

Heavy switching includes 3-state and bidirectional enables and state changes. For wafer sort efficiency in the presence of heavy SSO switching, the first 2/3rds of the vector set should test the majority of the logic and toggle all I/O.

• Directional changes on large busses MUST be placed at the end of the test pages (last one third of the vector set). [AMCCVRC SSO check]

• Vectors should be written to cover as much of the circuit as possible prior to introducing 3-state and bidirectional enable switching or other heavy (multiple output) switching.

- To increase test efficiency, long sequences (as are necessary for large counters) SHOULD be placed at the end of the test pages. A long sequence is one exceeding 1K vectors. If possible, break up counters for testing.

- Input vectors MUST be uniformly applied in a fixed time interval of 100ns MINIMUM, no skewing of the input signals is allowed in a functional simulation.

- Each output sample MUST represent a uniform, fixed time interval of 100ns MINIMUM. For any array, the output sample interval should be equal to the MAXIMUM WORST-CASE propagation delay of the longest path plus 50ns, rounded up to the nearest 100ns increment (100, 200, 300, etc.). AMCC limits the Sentry tester to a maximum frequency of 5MHz.

- To satisfy AMCC design submission requirements, make a COPY of the AMCCSIMFMT output file and edit that file to add functional description comments as to the tests being performed at the location in which they occur within the file. As an alternative, the designer may submit some other, equally comprehensive description of the tests.

- All functional simulation files must be clearly listed and explicitly identified in a read me first index

- All maximum (MILITARY or COMMERCIAL), sampled functional simulation result files in AMCCSIMFMT must pass AMCCVRC prior to submission. Any errors left at submission time must be documented and must have a waiver from AMCC.

- Minimum sampled functional simulation result files are not run through AMCCVRC but must be compared for exact matches to their respective maximum result files.

- Minimum and maximum functional simulation files MUST exactly match.

The following AMCCVRC error does not need to be waivered:

- SSO check errors due to SET, RESET are to be clearly documented by the user as to what they are.

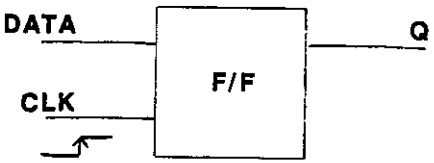
- Develop 3-state and bidirectional enable net to allow enable/disable in groups not exceeding eight outputs. NOTE: this may require additional I/O macros and their pads.

FIGURE 4-2-1 FUNCTIONAL AMCCSIMFMT SIMULATION FILE
TIME IN INTEGER FORMAT; SCALED FOR 100ns
(DAISY; VALID EWS)

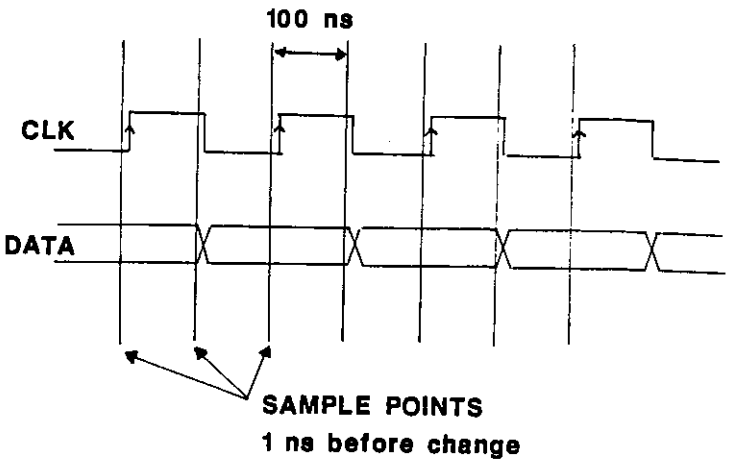
```
SAMPLE FILE: FUNCTIONAL SIMULATION
Q3500/Q5000/Q14000 SCALING: 10000 = 100ns
SAMPLE TAKEN 1 SIMULATION STEP PRIOR TO CHANGE
SAMPLE IS UNIFORM

1***CIRCUIT IDENTIFICATION =

                EESS SSDD DDDD DDDD DDDD DDY
                XXEE EEAA AAAA AAAA AAAA AAO
                TTLL LLTT TTTT TTTT TTTT TTU
                CRCC CC01 2345 6789 1111 11T
                LSTT TT              0123 45P
                KT32 10                   T

        TIME

9999            0100 0010 0101 1001 1010 010
19999           1100 0010 0101 1001 1010 010
29999           0000 0010 0101 1001 1010 010
39999           1000 0010 0101 1001 1010 011
49999           0000 0000 0101 1001 1010 011
59999           1000 0000 0101 1001 1010 010
69999           0000 0010 0101 1001 1010 010
79999           1000 0010 0101 1001 1010 011
89999           0001 0010 0101 1001 1010 011
99999           1001 0010 0101 1001 1010 010
109999          0001 0010 0111 1001 1010 010
119999          1001 0010 0111 1001 1010 011
129999          0001 0010 0101 1001 1010 011
139999          1001 0010 0101 1001 1010 010
149999          0011 0010 0101 1001 1010 010
159999          1011 0010 0101 1001 1010 011
169999          0011 0010 0101 1001 1000 011
179999          1011 0010 0101 1001 1000 010
189999          0011 0010 0101 1001 1010 010
199999          1011 0010 0101 1001 1010 011
209999          0010 0010 0101 1001 1010 011
219999          1010 0010 0101 1001 1010 010
229999          0010 0010 0101 1011 1010 010
239999          1010 0010 0101 1011 1010 011
249999          0010 0010 0101 1001 1010 011
259999          1010 0010 0101 1001 1010 010
269999          0010 0110 0101 1001 1010 010
                    • • •
```

FIGURE 4-2-1 FUNCTIONAL AMCCSIMFMT SIMULATION FILE
TIME IN INTEGER FORMAT; SCALED FOR 100ns
(DAISY; VALID EWS)

```
                 • • •
939999      1000 1010 0101 1001 1010 010
949999      0000 1010 1101 1001 1010 010
959999      1000 1010 1101 1001 1010 011
969999      0000 1010 0101 1001 1010 011
979999      1000 1010 0101 1001 1010 010
989999      0000 0010 0101 1001 1010 010
999999      1000 0010 0101 1001 1010 011
```




## ACTIVE ON RISING EDGE OF CLOCK




## CHANGE DATA ON INACTIVE EDGE

FIGURE 4-2-3 FUNCTIONAL AMCCSIMFMT SIMULATION FILE TIME IN MENTOR FORMAT

SAMPLE FILE: FUNCTIONAL SIMULATION
SAMPLE TAKEN 1 SIMULATION STEP PRIOR TO CHANGE
SAMPLE IS UNIFORM

1***CIRCUIT IDENTIFICATION =

| | | | | | |
|---|---|---|---|---|---|
| EESS | SSDD | DDDD | DDDD | DDDD | DDY |
| XXEE | EEAA | AAAA | AAAA | AAAA | AAO |
| TTLL | LLTT | TTTT | TTTT | TTTT | TTU |
| CRCC | CC01 | 2345 | 6789 | 1111 | 11T |
| LSTT | TT | | | 0123 | 45P |
| KT32 | 10 | | | | T |

| TIME | | | | | | |
|---|---|---|---|---|---|---|
| 99.99 | 0100 | 0010 | 0101 | 1001 | 1010 | 010 |
| 199.99 | 1100 | 0010 | 0101 | 1001 | 1010 | 010 |
| 299.99 | 0000 | 0010 | 0101 | 1001 | 1010 | 010 |
| 399.99 | 1000 | 0010 | 0101 | 1001 | 1010 | 011 |
| 499.99 | 0000 | 0000 | 0101 | 1001 | 1010 | 011 |
| 599.99 | 1000 | 0000 | 0101 | 1001 | 1010 | 010 |
| 699.99 | 0000 | 0010 | 0101 | 1001 | 1010 | 010 |
| 799.99 | 1000 | 0010 | 0101 | 1001 | 1010 | 011 |
| 899.99 | 0001 | 0010 | 0101 | 1001 | 1010 | 011 |
| 99.999 | 1001 | 0010 | 0101 | 1001 | 1010 | 010 |
| 1099.99 | 0001 | 0010 | 0111 | 1001 | 1010 | 010 |
| 1199.99 | 1001 | 0010 | 0111 | 1001 | 1010 | 011 |
| 1299.99 | 0001 | 0010 | 0101 | 1001 | 1010 | 011 |
| 1399.99 | 1001 | 0010 | 0101 | 1001 | 1010 | 010 |
| 1499.99 | 0011 | 0010 | 0101 | 1001 | 1010 | 010 |
| 1599.99 | 1011 | 0010 | 0101 | 1001 | 1010 | 011 |
| 1699.99 | 0011 | 0010 | 0101 | 1001 | 1000 | 011 |
| 1799.99 | 1011 | 0010 | 0101 | 1001 | 1000 | 010 |
| 1899.99 | 0011 | 0010 | 0101 | 1001 | 1010 | 010 |
| 199.999 | 1011 | 0010 | 0101 | 1001 | 1010 | 011 |
| 2099.99 | 0010 | 0010 | 0101 | 1001 | 1010 | 011 |
| 2199.99 | 1010 | 0010 | 0101 | 1001 | 1010 | 010 |
| 2299.99 | 0010 | 0010 | 0101 | 1011 | 1010 | 010 |
| 2399.99 | 1010 | 0010 | 0101 | 1011 | 1010 | 011 |
| 2499.99 | 0010 | 0010 | 0101 | 1001 | 1010 | 011 |
| 2599.99 | 1010 | 0010 | 0101 | 1001 | 1010 | 010 |
| 2699.99 | 0010 | 0110 | 0101 | 1001 | 1010 | 010 |

• • •

## FUNCTIONAL SIMULATION DOCUMENTATION REQUIREMENTS

Documentation included on AMCC-readable magnetic-media specifically for the functional simulation includes:

- the commented simulation control files;
- any referenced data input file;
- the timing library (MIN, COM, MIL) used;
- the worst-case multiplier(s) within that library that were used, if applicable (MIN, MAX);
- The sampled AMCCSIMFMT files produced (UNEDITED);
- either a text file version of the sampled AMCCSIMFMT file or some other document which clearly describes the testing being performed;
- the Front-Annotation file(s) used in the simulations;
- the command file used to generate the AMCCSIMFMT files;
- the timing error report with any remaining unresolved errors explained.
- the AMCCVRC signal analysis file used (clocked circuits)
- The AMCCVRC.LST report with errors documented and waivered as necessary.

The documentation should include all of the files necessary for AMCC to recreate all maximum worst case functional simulation executions and all minimum worst case functional simulation executions. Simulation stimuli, control and result files are required.

Both maximum and minimum simulations must be run. If the results of these are the same, only the maximum worst-case simulations need be submitted.

## MASTER RESET AND SSO VIOLATIONS

AMCCVRC will check for SSO violations at each vector. When an SSO violation is found due to a reset, the vectors should be changed and documented as follows:

1. The reset performed must reset the entire circuit.
2. The reset is followed by the re-initialization of macros not initialized by the reset.
3. The address of the next vector following the initialization is the restart address.

Document the reset by:

1. The address of the master reset.
2. The restart address.

Test will stop monitoring the outputs at the reset address and ignore outputs until the restart address.

Document the resets and restarts on the AMCCVRC.LST report for the vector set.

## PARTIAL RESETS

Resets of a partial circuit that do not violate the AMCCVRC SSO check do not need to follow these procedures.

## 3-STATE ENABLE AND BIDIRECTIONAL ENABLES

Any time that a 3-state output enable signal changing state causes an SSO violation the following changes must be made:

1. Redesign the circuit to add test-enable gates that allow 8 or 16 enables at a time and therefore meets the SSO requirement.

   - During normal operation the test enables are not used.

   - During test, they are used to de-gate the enable signals.

2. Write the vectors to use the test enable signals.

## AT-SPEED SIMULATION SUBMISSION (REQUIRED)
## NO HARDWARE TESTING IMPLIED - SIMULATION ONLY

An at-speed simulation is used to verify the actual timing performance of the circuit as implemented on the array against the target specification for the circuit.

- The at-speed simulation is run prior to layout using worst-case multipliers and Front-Annotation to spot potential problem areas in the circuit and to assist in defining the criteria for the layout. The Front-Annotation file makes a statistically-based estimate of the metal delay and adds the actual delay due to fan-out load and any wire-ORs present. All paths must be computed using worst-case timing multipliers and the Front-Annotation delay file. AMCC DOES NOT guarantee Front-Annotation simulation results.

The at-speed simulation is run after layout using the Back-Annotation file to verify the actual timing performance for the array. The Back-Annotation file provides the ACTUAL metal delays for the layout combined with the actual fan-out and wire-OR delays. AMCC DOES guarentee worst-case maximum Back-Annotation simulation results.

Note that the at-speed simulation outputs will be time-dependent (some results are not necessarily available within one sample step). The apparent "phase delay" of some outputs relative to others makes the evaluation of at-speed simulation results a non-trivial exercise. AMCC can assist the designer in interpreting and understanding the results of such simulations.

Note: at present, at-speed is optional for VALID EWS-based design submissions that have had the timing verifier used to verify circuit at-speed performance.

AT-SPEED SIMULATION RULES

- AMCC requires both a uniformly sampled output and a print-on-change output file for both a maximum worst case and minimum worst case at-speed simulation.

- The at-speed simulation output file format should be identical to that used for functional and AC test simulations.

- The output file format must be binary with the same symbol restrictions as for functional simulations (0, 1, X, Z).

- The print-on-change file should monitor the same primary inputs and primary outputs as monitored on the sampled output (i.e., use the same file format). The print-on-change output provides a picture of actual time-of-change for the monitored signals.

- The input signals can be skewed to emulate the actual circuit board environment.

- The at-speed simulation is to run at the specified maximum operating frequency of the actual part.

- The at-speed sampled and print-on-change simulation output files MUST exercise all paths of interest. AMCC cannot analyze paths without proper customer-generated at-speed vectors.

- AMCC limits the at-speed simulation vectors to 32K.

- The uniformly applied sample interval should be that of the period of the fastest input signal (once per period). Where there are many clocks or phases, or for high-frequency applications, consult AMCC for the preferred sample step size.

- The samples should be taken 1 simulator time unit before the fastest changing signal changes state.

- Sampled output files and print-on-change output files must be submitted in AMCCSIMFMT output format. Sampled at-speed simulation outputs will be used for comparison.

Example at-speed simulation AMCCSIMFMT files are shown in Figures 4-3-1 and 4-3-3. Figure 4-3-1 shows a sampled file. Figure 4-3-3 shows a print-on-change file. Both are required. Figure 4-3-2 is a diagram of phase-delay, where the result of the clock in one cycle appears at an output one or more clock cycles later.

FIGURE 4-3-1: SAMPLE FILE: AT SPEED SIMULATION
- SAMPLED

Q3500/Q5000/Q14000 SCALING: 10000 = 100ns (DAISY)
SAMPLE TAKEN 1 SIMULATION STEP PRIOR TO END OF
CLOCK CYCLE; AND PRIOR TO MIDPOINT OF CYCLE
RESULTS SHOW A PHASED DELAY

```
  TYPE SIMFMTAS.01
1***CIRCUIT IDENTIFICATION =

            EESSSSDDDDDDDDDDDDDDDD YP
            XXEEEEAAAAAAAAAAAAAAAA OA
            TTLLLLTTTTTTTTTTTTTTT UR
            CRCCCC01234567891111111 TA
            LSTTTT          012345 PM
            KT3210                 T

       TIME

499         0100001001011001101001 01
999         1100001001011001101001 01
1499        0000001001011001101001 01
1999        1000001001011001101001 01
2499        0000000001011001101001 11
2999        1000000001011001101001 01
3499        0000001001011001101001 01
3999        1000001001011001101001 01
4499        0001001001011001101001 11
4999        1001001001011001101001 01
5499        0001001001111001101001 01
5999        1001001001111001101001 01
6499        0001001001011001101001 11
6999        1001001001011001101001 01
7499        0011001001011001101001 01
7999        1011001001011001101001 01
8499        0011001001011001100001 11
8999        1011001001011001100001 01
9499        0011001001011001101001 01
9999        1011001001011001101001 01
10499       0010001001011001101001 11
10999       1010001001011001101001 01
11499       0010001001011011101001 01
11999       1010001001011011101001 01
12499       0010001001011001101001 11
12999       1010001001011001101001 01
13499       0010011001011001101001 01
13999       1010011001011001101001 01
14499       0010011001011000101001 11
14999       1010011001011000101001 01
15499       0010011001011001101001 01
                    • • •
```

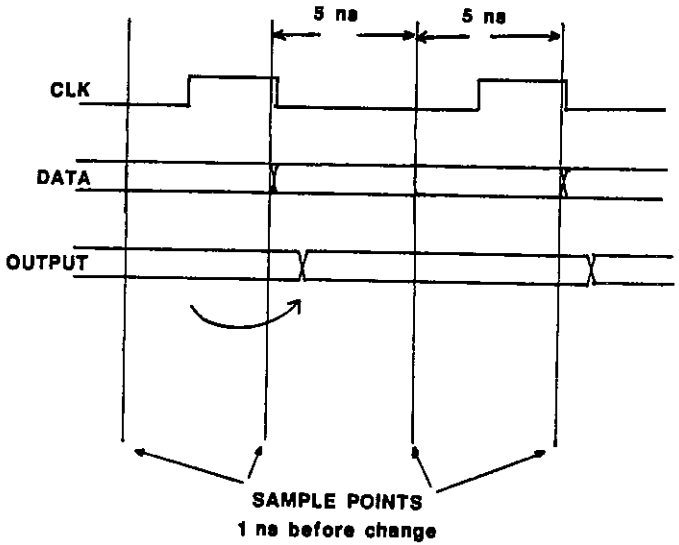
```
                    • • •
47999       10001010110110011010O1 01
48499       00001010010110011010O1 11
48999       10001010010110011010O1 01
49499       00000010010110011010O1 01
49999       10000010010110011010O1 01
```

FIGURE 4-3-2: EXAMPLE OF PHASE DELAY

**70/30 CLOCK**

**100 MHz SYSTEM SPECIFICATION**

**"PHASE DELAY"**




**CHANGE DATA ON INACTIVE EDGE**
**(could skew if needed)**

FIGURE 4-3-3: SAMPLE FILE: AT SPEED SIMULATION
- PRINT ON CHANGE
Q3500/Q5000/Q14000 SCALING: 10000 = 100ns (DAISY)
RESULTS SHOW A PHASED DELAY

```
 TYPE POCFMTAS.01
1***CIRCUIT IDENTIFICATION =

              EESSSSDDDDDDDDDDDDDDD YP
              XXEEEEAAAAAAAAAAAAAAA OA
              TTLLLLTTTTTTTTTTTTTTT UR
              CRCCCC012345678911111 TA
              LSTTTT          012345 PM
              KT3210                 T

       TIME

700           110000100101100110100 1 01
1000          000000100101100110100 1 01
1700          100000100101100110100 1 01
2000          000000000101100110100 1 01
2063          000000000101100110100 1 11
2700          100000000101100110100 1 11
3000          000000100101100110100 1 11
3018          000000100101100110100 1 01
3700          100000100101100110100 1 01
4000          000100100101100110100 1 01
4063          000100100101100110100 1 11
4700          100100100101100110100 1 11
5000          000100100111100110100 1 11
5018          000100100111100110100 1 01
5700          100100100111100110100 1 01
6000          000100100101100110100 1 01
6063          000100100101100110100 1 11
6700          100100100101100110100 1 11
7000          001100100101100110100 1 11
7018          001100100101100110100 1 01
7700          101100100101100110100 1 01
8000          001100100101100110000 1 01
8063          001100100101100110000 1 11
8700          101100100101100110000 1 11
9000          001100100101100110100 1 11
9018          001100100101100110100 1 01
9700          101100100101100110100 1 01
10000         001000100101100110100 1 01
10063         001000100101100110100 1 11
10700         101000100101100110100 1 11
11000         001000100101101110100 1 11
11018         001000100101101110100 1 01
11700         101000100101101110100 1 01
                        • • •
```

## AT-SPEED SIMULATION DOCUMENTATION REQUIREMENTS

Documentation required on AMCC-readable magnetic-media specifically for the at-speed vector simulation includes:

- the commented simulation control file;
- any referenced data input file;
- the timing library used (MIN, COM, MIL, etc.)
- the worst-case multiplier(s) within that libary that were used, if applicable (MIN, MAX).
- the sampled AMCCSIMFMT files produced (UNEDITED);
- a text file version of the AMCCSIMFMT file or some other document which clearly describes the testing performed;
- the Front-Annotation file(s) used in the simulations
- the command files used to generate the sampled AMCCSIMFMT files.
- The print-on-change AMCCSIMFMT files
- the timing error report with any remaining unresolved errors explained.

Due to reconvergent fan-out, MIN/MAX simulations may have erroneous results. These false errors will need to be identifed if MIN/MAX simulations are to be used, since reconvergent fan-out is not handled by most simulators.

The documentation should include all necessary files to recreate both the maximum worst case at-speed simulation and the minimum worst case at-speed simulation. Both inputs and results are required. Both simulations (maximum and minimum) are required. Outputs must be submitted in both sampled and print-on-change format.

## AC TESTS:
## PROPAGATION PATH DELAY VECTOR SUBMISSION (OPTIONAL)
## PACKAGED PARTS ONLY

A maximum of 10 measurements (small arrays; < 2000 gates) and 20 measurements (large arrays; > 2000 gates) are allowed for logic array testing. Mesuring the rising and falling edges for one output signal counts as TWO measurements. Each test is from one input to one output.

These are propagation path tests only.

Measurements are made at +1.5V threshold for TTL and at 1.3V below reference for ECL.

Figure 4-4-1 shows a sampled and Figure 4-4-2 shows a print-on-change AC test simulation AMCCSIMFMT file for a propagation path delay. The example uses DAISY results. (VALID outputs would be identical in appearance. MENTOR output shows a decimal point in the time step (vector address).) The data signal SELCT3 is falling and the observed output is YOUTPT.

Both sampled and print-on-change AC Test simulation output files are required for design submission.

## CONCATENATED AC TESTS

As an option, all AC vector sets may be concatenated into one simulation input file and submitted as one sampled and one print-on-change output file for each operating condition simulated. The concatenated file may not exceed 4K vectors.

Each test must begin with an initialization routine to bring the circuit from the power-up unknown state to a known state, then supply the correct biasing and stimuli for the individual tests. The start address of the AC test in this case would be zero for the first test, a different address for the next test and so on.

## SHARED VECTORS

When more than one test can use the same identical set of vectors, only one version of the set needs to be supplied. This occurs when a bus has more than one member tested or in parallel interrelated operations. Each measurement (one input to one output) counts as a separate test.

FIGURE 4-4-1 AC TEST AMCCSIMFMT SIMULATION FILES
PROPAGATION DELAY; SAMPLED AND PRINT ON CHANGE
- individual simulation
SAMPLE FILE: AC TEST FOR SELCT3 RISING - SAMPLED
100ns scaling - DAISY

```
1***CIRCUIT IDENTIFICATION =

            SS SSDD DDDD DDDD DDDD DDY
            EE EEAA AAAA AAAA AAAA AAO
            LL LLTT TTTT TTTT TTTT TTU
            CC CC01 2345 6789 1111 11T
            TT TT              0123 45P
            32 10                    T

      TIME

9999        00000000000000000000000000
19999       00000000001000000000000000   initialize
29999       10000000001000000000000001   transition
            ^                        ^    and result
```

FIGURE 4-4-2 AC TEST AMCCSIMFMT SIMULATION FILES
SAMPLE FILE: AC TEST FOR SELCT3 RISING
- PRINT ON CHANGE (DAISY)

```
1***CIRCUIT IDENTIFICATION =

            SS SSDD DDDD DDDD DDDD DDY
            EE EEAA AAAA AAAA AAAA AAO
            LL LLTT TTTT TTTT TTTT TTU
            CC CC01 2345 6789 1111 11T
            TT TT              0123 45P
            32 10                    T

      TIME

10000       00000000001000000000000000   initialize
20000       10000000001000000000000000   transition
21494       10000000001000000000000001   result
                                     ^
```

FIGURE 4-4-3 AC TEST AMCCSIMFMT SIMULATION FILES
PROPAGATION DELAY; SAMPLED AND PRINT ON CHANGE
- concatenated simulation
SAMPLE FILE: AC TEST FOR SELCT3 RISING;
DATA12 FALLING

```
1***CIRCUIT IDENTIFICATION =

            SS SSDD DDDD DDDD DDDD DDY
            EE EEAA AAAA AAAA AAAA AAO
            LL LLTT TTTT TTTT TTTT TTU
            CC CC01 2345 6789 1111 11T
            TT TT              0123 45P
            32 10                    T

      TIME

9999        00000000000000000000000000
19999       00000000001000000000000000   initialize
29999       10000000001000000000000001   trans; result
            ^                          ^
39999       00000000000000000000000000
49999       11000000000000000000100001   re-initialize
59999       11000000000000000000000000   trans; result
                                  ^    ^
```

Whether or not the tests are independently developed, they are constructed to run independently. Each test has its own initialize step(s), then a transition-result step. A circuit may require several steps to set-up the propagation path for measurement (called "biasing" the circuit). The tests should be written so that they could be looped by the tester by themselves - i.e., they rely on no other vectors.

For the above, the start address of the first test is "9999" and the last address is "29999". For the second test, the start address is "39999" and the last address is "59999".

## AC TEST SIMULATION RULES

- A set of vectors must be supplied for each path (each group of outputs tested) and each data direction to be tested. Data may be measured for both rising and falling edge inputs for each path. A separate vector set is required for each edge direction measured.

- All vector sets can be concatenated into one simulation.

- The vector set should be sufficient to initialize the path(s) required to set-up the intended measurement. The vectors must initialize the array and then stimulate the path(s) to be measured. For each path, the input, output and relevant input bias conditions must be specified.

- If a group of outputs is switched simultaneously (such as with a bus) then those outputs may be covered by a single vector set. The vector set will be used repeatedly for each path. The outputs will be measured one at a time. Clearly specify the input to be paired with each output to be measured.

- The last vector in each vector set will be the one which causes the output to change to the state desired for the measurement to be made. The last vector in a vector set is the only point at which a measurement will be made for that set. For different AC test measurements, consult AMCC.

- Both the input control signal transition (normally a clock input) and the output transition change **MUST** appear in the same output vector.

- The signals included and the order of the signals in the AC simulations **MUST** be the same and in the same order as for the functional simulation(s) (same output format), i.e., all primary inputs, all primary outputs and then all 3-state and bidirectional enables, if any.

- The simulation output format must be binary with the same signal state symbol restrictions as for functional simulations (1, 0, X, Z).

- All paths **MUST** be clearly identified on one set of the schematics. Notes are recommended for the EWS schematics.

- Each path **MUST** have the input (stimulus) pin and the output (response) pin clearly identified on one set of the schematics.

- Test limits **MUST** be clearly defined for each path.

- A print-on-change file, in addition to the sampled simulation output file, **MUST** accompany all AC test simulation vector submissions. Note that the submission must include simulations made using the worst-case maximum (MILITARY or COMMERCIAL) timing multiplier and the worst-case MINIMUM timing multiplier.

- All AC sampled and print on change simulation output files submitted to AMCC **MUST** have been run through the AMCCSIMFMT simulation output file processor.

- The AC test simulation vector sets are simulated and documented as for functional simulation.

- No test can accept input from a pin that is then made into an output during the test and is used to provide the result (i.e., bidirectionals).

- ECL bidirectional and 3-state macros involved in the test may have only a logic "1" or a logic "0" output. Tests are made to measure 1->0 or 0->1 transition delays. ECL output loading is 50 ohms.

- TTL bidirectional and 3-state macros have three true states: 1, 0 and Z.

Tests for 1->Z, Z->1, 0->Z or Z->0 may be made available: Consult with AMCC if you require these tests.

A differential pair can provide input for any test. The measurement is made from the crosspoint.

A differential pair used as output can appear on any AC test. The measurement will be made to only one output. Clearly specify which output is to be used in the test. If both outputs are to be measured, this counts as two measurements.

Actual tester limits are computed using Back-Annotation simulation results and the system capacitive load and package pin capacitance. The package pin capacitance is that supplied in the CIRCUIT.PKG file after placement and routing have been completed. The system load is that supplied in the OUTPUT.DLY file as a result of the AMCCANN user-interface execution. Both values are read from the AMCCPKG.LST report file.

## DOCUMENTING AC TEST SIMULATION

Documentation required on AMCC-readable magnetic-media specifically for the AC test vector simulation includes:

- the commented simulation control file(s);
- any referenced simulation input file(s);
- the timing library used (MIN, COM, MIL);
- the worst-case muiltiplier(s) within that library that were used, if applicable (MIN, MAX);
- the sampled AMCCSIMFMT files (UNEDITED); two per test (worst-case maximum; minimum);
- the print-on-change AMCCSIMFMT files; two per test (worst-case maximum; minimum);
- a text file version of the AMCCSIMFMT file(s) or some other document which clearly describes the testing performed;
- the Front-Annotation files used in the simulations;
- the command file(s) used to generate the simulation results in sampled AMCCSIMFMT format.
- the timing error reports for the simulations with any remaining unresolved errors explained.
- the AMCCVRC signal analysis file used (clocked circuits);
- the AMCCVRC.LST report for the sampled worst-case maximum simulation. Note: The simultaneously switching output check does apply to AC tests.

The documentation should include all necessary files to recreate both the maximum worst case AC test simulation and the minimum worst case AC test simulation. Both inputs and results are required. Both simulations (maximum and minimum) are required. Outputs must be submitted in both sampled and print on change format.

## GUIDELINES FOR PARAMETRIC VECTORS
(OPTIONAL VECTORS)

Quality Assurance departments will generally require that the DC parametric tests for VIH and VIL be performed. Should this option be selected, there are three approaches to submitting a design to AMCC:

1) combinatorial circuits with no added gate tree;
2) sequential circuits with no added gate tree; and
3) combinatorial or sequential circuits with an added gate tree.

There are several types of inputs that cannot be tested in any of these approaches. They are: thermal diodes, AC monitors, VBxx macros, added power and ground macros, and unbuffered ECL or TTL inputs. Unbuffered TTL and ECL inputs are covered by their paired buffered inputs. Unbuffered ECL which drives BIxx macros are not covered.

In addition to these, a gate tree implementation will not be able to test external 3-state enable-drivers.

Differential inputs always operate as a pair and each pair should be considered as a single entity when reading the following test methodology descriptions.

If the output is not as expected for any vector, error is detected.

COMBINATORIAL CIRCUITS - NO GATE TREE ADDED

This approach is for non-clocked circuits and circuits with no SET or RESET, i.e., combinational or combinatorial-only circuits.

- All inputs must be tested, with the exceptions only those previously listed.

- Within the vector set, each input must vary from 0-1 and from 1-0.

- One or more than one input may vary in any given vector.

- None, one or more than one output may switch in a given vector.

- The number of outputs switching in a vector must pass the AMCCVRC SSO Check. (Refer to the AMCCVRC SSO check for a description of the limits, Volume II, Section 8, Appendix B.)

- Perform AMCCVRC checks: Parametric Toggle Test *
  (Checks Inputs Only)
  SSO Check
  Length Check
  Differential Input Check
  Required Signals Check
  Unknown Signals Check

* These AMCCVRC checks are not yet implemented (809).

SEQUENTIAL CIRCUITS - NO GATE TREE ADDED

This approach is for clocked circuits, circuits with latches, flip/flops or MSI macros containing these elements.

- All inputs must be tested, with the exceptions only those previously listed.

- Within the vector set, each input must vary from 0-1 and from 1-0.

- One or more than one input may vary in any given vector.

- Only one output may switch in a given vector (except in the case of a differential).

- Perform AMCCVRC checks:
  - Parametric Toggle Test * (Checks Inputs Only)
  - Length Check
  - Differential Input Check
  - Required Signals Check
  - Unknown Signals Check
  - Sequential Toggle Test * (Checks for one output)

* These AMCCVRC checks are not yet implemented (809).

GATE TREE - ANY CIRCUIT (RECOMMENDED)

This approach for parametric testing is the best for any circuit, any I/O mode. This procedure is the one AMCC prefers and recommends. It requires internal logic cells, internal routing, and possibly one additional I/O cell.

- Enable the TEST mode in the first vector if the design requires it. Set all bidirectional macros to the input mode, set up gating, etc.

- Gate all inputs (except those already identified as exclusions) together (use an AND tree, a NOR tree, etc. as required).

- Bring the result of the GATE tree out to a primary output which must be listed in the simulation vector format. (Note: It will be listed in ALL simulations performed on this circuit.)

- The results may be passed through a multiplexer to allow use of an existing primary output only if the circuit is I/O limited.

- One input may switch per vector in the following manner.
    - Start with all inputs at logical "1"
    - Switch one input to zero
    - Switch that one input back to one
    - Switch the next input in sequence to zero.
    - Continue until all inputs have been toggled

A sample gate tree is shown in Figure 4-5-1. The inputs are from the unused inverted outputs of the circuit input macros, adding to the power consumption but not to time delays in the main circuit.

- Perform AMCCVRC checks: Parametric Toggle Test *
  (Checks Inputs Only)
  SSO Check
  Differential Input Check
  Required Signals Check
  Unknown Signals Check
  Parametric Output Test *
  (Gate output must toggle
  in each vector)

- The race check is not required.

* These AMCCVRC checks are not yet implemented (809).

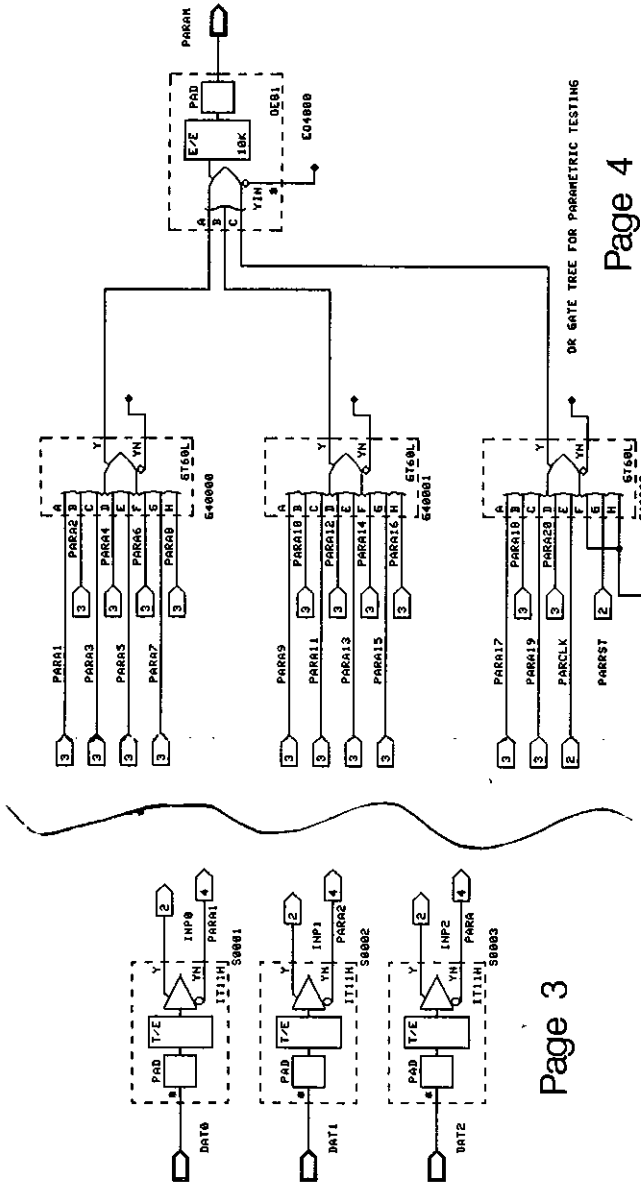



**FIGURE 4-5-1 Parametric Test Logic**
(partial circuit)

FIGURE 4-5-2: GATE-TREE PARAMETRIC TEST SAMPLE PATTERN:

```
                    Gated
                    tree
...input....        result
111111111111        1
011111111111        0
111111111111        1
101111111111        0
111111111111        1
110111111111        0
111111111111        1   toggle the
111011111111        0   output
111111111111        1
111101111111        0
111111111111        1
111110111111        0
111111111111        1
111111011111        0
111111111111        1
111111101111        0
111111111111        1
111111110111        0
111111111111        1
111111111011        0
111111111111        1
111111111101        0
111111111111        1
111111111110        0
111111111111        1
```

Figure 4-5-3 shows the AMCCSIMFMT output file for the parametric vector set for the gate structure of Figure 4-5-1.

**DOCUMENTING PARAMETRIC VECTORS**

Parametric vector sets are to be documented the same as for functional vectors, with a sampled simulation output.

Include a written description of the test if the GATE version (option 3) was used and include: address at which the circuit is initialized; and name of the primary output signal for the gate.

AMCC reserves the right to judge the validity of vectors for these tests and may require changes. AMCC will make recommendations if changes are required.

```
1***CIRCUIT IDENTIFICATION =
            EESSSSDDDDDDDDDDDDDDD YP
            XXEEEEAAAAAAAAAAAAAAA OA
            TTLLLLTTTTTTTTTTTTTTT UR
            CRCCCC01234567891111111 TA
            LSTTTT          012345 PM
            KT3210                 T
-----------------------------------------
9999        111111111111111111111 00
19999       111111011111111111111 01
29999       111111111111111111111 00
39999       111111101111111111111 01
49999       111111111111111111111 00
59999       111111110111111111111 01
69999       111111111111111111111 00
79999       111111111011111111111 01
89999       111111111111111111111 00
99999       111111111101111111111 01
109999      111111111111111111111 00
119999      111111111110111111111 01
129999      111111111111111111111 00
139999      111111111111011111111 01
149999      111111111111111111111 00
159999      111111111111110111111 01
169999      111111111111111111111 00
179999      111111111111111011111 01
189999      111111111111111111111 00
199999      111111111111111101111 01
209999      111111111111111111111 00
219999      111111111111111110111 01
229999      111111111111111111111 00
239999      111111111111111111011 01
249999      111111111111111111111 00
259999      111111111111111111101 01
269999      111111111111111111111 00
279999      111111111111111111011 01
289999      111111111111111111111 00
299999      111111111111111111101 01
309999      111111111111111111111 00
319999      111111111111111111110 01
329999      111111111111111111111 00
339999      011111111111111111111 01
349999      111111111111111111111 00
359999      101111111111111111111 01
369999      111111111111111111111 00
379999      111110111111111111111 01
389999      111111111111111111111 00
399999      111101111111111111111 01
409999      111111111111111111111 00
419999      111011111111111111111 01
429999      111111111111111111111 00
439999      110111111111111111111 01
449999      111111111111111111111 00
```

FIGURE 4-5-3 PARAMETRIC VECTORS (16:1 MUX EXAMPLE)

## REQUESTING HARDWARE TESTING (OPTIONAL)

### BENCH TESTING

These are characterization-only tests, performed on a limited quantity basis.

For speeds up to 25MHz, an automated test utilizing HP test equipment can be arranged (64 inputs maximum).

### CRITICAL PATH TESTING

Critical paths (typically 1 to 5 maximum) testing, for propagation delay and set-up and hold time, on the bench can be performed without a special test fixture provided the following information is supplied:

- the critical input pin and the critical output pin are defined;
- the vectors used are a subset of the AC Test Vectors defined in the previous section;
- a stand-alone set of AC vectors is provided to establish the test condition on only those pins which are necessary to bias and set-up the critical path;
- the AC test vector set must be simulated and verified prior to release to test;
- the AC vector set must be repeatable therefore initialization vectors must be included in the set. The length of the set is restricted to 50 vectors in length in order to view to critical path with a normal oscilloscope.

## MAXIMUM FREQUENCY TEST

The maximum frequency test is limited to 350MHz (bipolar) or 50MHz (BiCMOS) and must be performed on a mutually agreed upon custom test fixture.

A clock frequency of up to $f_{MAX}$ = 350MHz (bipolar) or 50MHz (BiCMOS), is used with a maximum of four (4) dynamic signals and a maximum of five (5) critical paths.

# APPENDIX

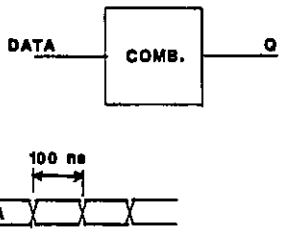
FUNCTIONAL SIMULATION DATA, CLOCK, SAMPLE POINT DIAGRAMS

If the propagation delay maximum worst-case plus 50ns is equal to or greater than 100ns, then the vectors are written for a 150 or 200ns time interval and this must be clearly documented in the design submission.

There is no limit on how many inputs may change at once. Since the objective is to find an error, one input per logic module maximum should be the norm.

CASE 1: COMBINATIONAL CIRCUIT - NO "CLOCK"

The vectors are written to change something every 100ns. The sample is taken one simulator time step prior to the next vector.

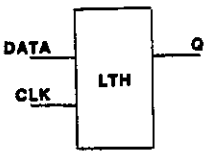



**CHANGE DATA EVERY STEP**

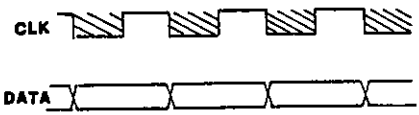
## FUNCTIONAL SIMULATION

CASE 2: TRANSPARENT-LOW LATCH

The vectors are written so that the data changes within the vector that also changes the clock from high to low (falling edge). The vector that changes the clock from low to high must change no other inputs. No vectors are written to change data between the clock edge changes. The sample is taken one simulator time step prior to the next vector.




TRANSPARENT LOW LATCH

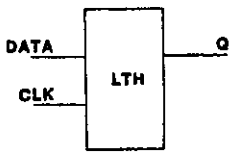



CHANGE DATA ON FALLING EDGE

## FUNCTIONAL SIMULATION

CASE 3: TRANSPARENT-HIGH LATCH

The vectors are written so that the data changes within the vector that also changes the clock from low to high (rising edge). The vector that changes the clock from high to low must change no other inputs. No vectors are written to change data between the clock edge changes. The sample is taken one simulator time step prior to the next vector.



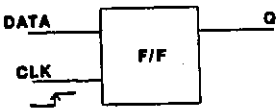

TRANSPARENT HIGH LATCH


CHANGE DATA ON RISING EDGE

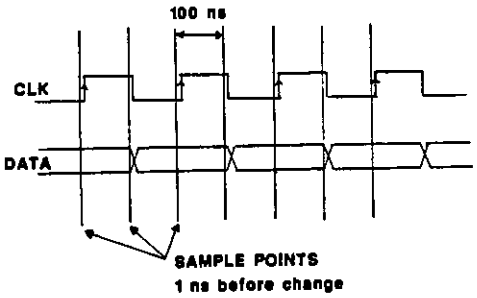
## FUNCTIONAL SIMULATION

CASE 4: RISING EDGE ACTIVE FLIP/FLOP

The vectors are written so that the data changes within the vector that also changes the clock from high to low (falling edge). The vector that changes the clock from low to high must change no other inputs. No vectors are written to change data between the clock edge changes. The sample is taken one simulator time step prior to the next vector.




ACTIVE ON RISING EDGE OF CLOCK

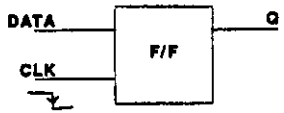



CHANGE DATA ON INACTIVE EDGE

## FUNCTIONAL SIMULATION

CASE 5: FALLING EDGE ACTIVE FLOP/FLOP

The vectors are written so that the data changes within the vector that also changes the clock from low to high (rising edge). The vector that changes the clock from high to low must change no other inputs. No vectors are written to change data between the clock edge changes. The sample is taken one simulator time step prior to the next vector.



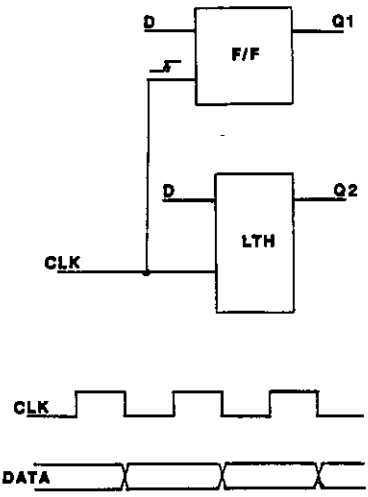

ACTIVE ON FALLING EDGE OF CLOCK


CHANGE DATA ON INACTIVE EDGE

## FUNCTIONAL SIMULATION

CASE 6: COMBINATION OF A TRANSPARENT LOW LATCH
AND A RISING-EDGE FLIP/FLOP

The vectors are written so that the data changes within the vector that also changes the clock from high to low (falling edge). The vector that changes the clock from low to high must change no other inputs. No vectors are written to change data between the clock edge changes. The sample is taken one simulator time step prior to the next vector.




**TRANSPARENT LOW LATCH**

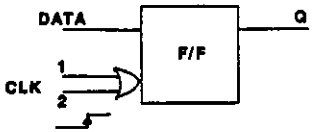
**AND**

**RISING EDGE F/F**

## FUNCTIONAL SIMULATION

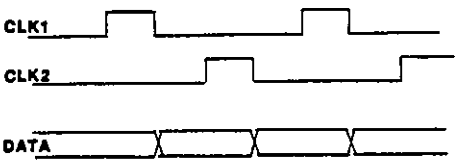
CASE 7: DUAL CLOCK SIGNALS
- RISING EDGE ACTIVE FLIP/FLOP

The vectors are written so that only one clock signal is changing at any time. The data may change in any vecto that is also changing a clock signal from high to low (falling edge). The diagram shows one possiblility. The vector that changes the clock from low to high must change no other inputs. No vectors are written to change data between the clock edge changes. The sample is taken one simulator time step prior to the next vector.




RISING EDGE ACTIVE

- DUAL CLOCK

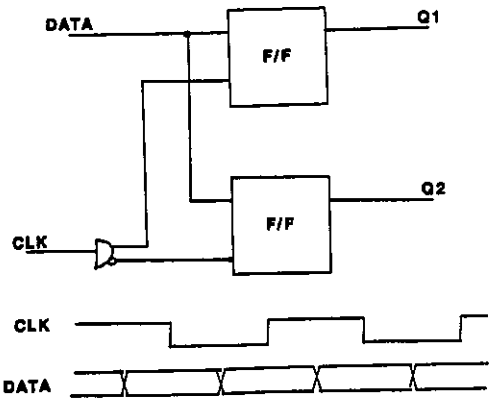



CHANGE DATA ON INACTIVE EDGES

## FUNCTIONAL SIMULATION

CASE 8: BOTH CLOCK EDGES ACTIVE
SAME DATA

In this case, the vectors that change the clock in either direction cannot change any other input (DATA in the diagram). The vectors that change the data cannot change any clock. The sample is taken one simulator time step prior to the next vector.




**BOTH EDGES ACTIVE**

**- ON SAME DATA**

## FUNCTIONAL SIMULATION